Power Loss Investigation in Low Power Current Source Inverters Using Wideband Gap Devices for Solar Energy Applications

by

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Abstract

With the steady expansion of renewable energy comes the need to develop next-generation power converters focusing on high power density, efficiency, and reliability with lowered costs, simple structure, and the ability to meet strict grid codes. Currently, Voltage Source Inverter (VSI) based solutions dominate the solar inverter market, however, the Current Source Inverter (CSI) introduces some interesting advantages making the topology a valued research area. These advantages include inherent short circuit protection, natural voltage boosting capabilities, increased reliability, and increased power density. However, CSIs suffer from significant conduction losses due to the need for reverse voltage blocking or "reverse blocking" (RB) semiconductors and a large DC-link inductor with high losses. It is speculated that Wide Bandgap (WBG) devices will push power converters to the "next generation". Although, the magnitude of WBG device advantages will depend on the ability of commercially available devices to harness the benefits of WBG material, as well as the converter configuration. With the roll-out of commercially available WBG devices, their advantages should be able to naturally improve the base CSI's efficiency through a reduction in the RB switch's conduction and switching losses. Also, by enabling higher switching frequency operation, passive components can be downsized. This alleviates the DC-link inductor size, cost, and power loss technical challenges seen in the CSI topology by a factor to be studied. Therefore, this research analyzes and compares the efficiency of numerous switch configurations applied to a 10kW string CSI using Powersim (PSIM) thermal module simulations. This provides context to the theoretical efficiency limits of the base CSI with enhanced next generation switches. This research studies in-depth the required size of the DC-link inductor and filer components at various switching frequencies and applied modulation schemes in order to accurately estimate their associated losses. Loss values are derived and used in the overall CSI efficiency comparison. The CSI efficiency is characterized at various switching frequencies, power ratings, operating temperatures, and modulation schemes.

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Publications

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List of Abbreviations

Abbreviation	Description
2L, 3L	Two level, Three level
AC	Alternating Current
ANPC	Active Neutral Point Clamped
AWG	American Wire Gauge
BD	Bidirectional
CL	Capacitor-Inductor (Filter Configuration)
CMV	Common Mode Voltage
CSI	Current Source Inverter
DC	Direct Current
DC-AC	DC to AC
DMV	Differential Mode Voltage
ESR	Equivalent Series Resistance
GaN	Gallium Nitride
GCT	Gate Commutated Thyristors
HEMT	High Electron Mobility Transistor
HF	High Frequency
IEA	International Energy Agency
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LC	Leakage Current
LF	Low Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

MPPT	Maximum Power Point Tracking
NS-SVM	Natural Sampling Space Vector Modulation
PECS	Photovoltaic Energy Conversion Systems
PF	Power Factor
PSIM	PowerSim
PU	Per Unit
PV	Photovoltaic
PWM	Pulse Width Modulation
R.E	Relative Error
RB	Reverse Blocking
RB-IGBT	Reverse Blocking Insulated Gate Bipolar Transistor
SBD	Schottky Barrier Diode
SHE	Selective Harmonic Elimination
Si	Silicon
SiC	Silicon Carbide
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TPWM	Trapezoidal Pulse Width Modulation
VSI	Voltage Source Inverter
WBG	Wide Bandgap
XFMR	Transformer

List of Symbols

Symbol	Description
a,b,c,d	Core Loss Curve Fitting Variables
A_e	Core Effective Area
α	Resistor Temperature Coefficient
B_{pk}	Peak AC Flux Density
C_f	Filter Capacitor
C_{gd}	Gate-to-drain Capacitance
D	Duty Cycle
d	Cable Diameter
ΔT	Time Duration
dv/dt	Voltage Rate of Change
$E_{on/off}$	Turn On or Turn Off Energy
$E_{on/off,n}$	Turn On or Turn Off Energy at Switching Instant n
E_{RMS}	RMS Voltage Across DC-link Inductor
$f_{fund.}$	Fundamental Frequency
f_{res}	Resonant Frequency
f_s	Sampling Frequency
f_{sw}	Switching Frequency
H	Magnetizing Force
$I_{c,1}$	Fundamental Filter Capacitor Current
I_{CE}	Collector-Emitter Current
I_{DC}	DC-link Current
ΔI_{DC}	DC-link Current Ripple

I_{ds}	Drain-Source Current
$I_{F,datasheet}$	Datasheet Test Forward Current
I_n	Current Sample SVM Switch State Vector
I_{n+1}	Future Sample SVM Switch State Vector
I_{ref}	SVM Reference Vector
i_s	CSI Grid Current
$I_s(n)$	n^{th} Harmonic Component of the CSI Grid Current
i_w	CSI PWM Current
$I_w(n)$	n^{th} Harmonic Component of the CSI PWM Current
k	SVM Sector Number
K	Slope of MOSFET Transfer Characteristics
L_{dc}	DC-link Inductance
L_e	Effective Core Length
L_f	Filter Inductance
L_g	Grid Inductance
L_T	Mean Length Per Turn
m_a	Modulation Index
m_f	Frequency Modulation Index
n	Sample/Switching Instant
N	Number of Samples Per SVM Sector
η_{CEC}	California Energy Commission Efficiency
η_{Euro}	European Efficiency
N_p	Number of Pulses
N_T	Number of Turns
ρ	Conductivity
P_{loss,C_f}	Filter Capacitor Power Loss
$P_{D,Cond,lower}$	Body Diode Conduction Loss of Case E's Lower Switch

P_{DC}	Inductor DC Winding Loss
P_{dc}	CSI Input Power
$P_{f_{sw},Si}$	Si MOSFET Switching Loss
$P_{Q,Cond,Lower}$	3^{rd} Quadrant Conduction Loss of Case E's Lower Switch
P_{sw}	Switching Loss
$P_{sw,D}$	Diode Switching Loss
Q	Quality Factor
Q_{rr}	Reverse Recovery Charge
R_{AC}	Inductor AC Resistance
$R_{ds(on)}$	MOSFET On-State Resistance
R_G	Gate Resistance
R_g	Grid Line Resistance
r_L	Resistance Per Unit Length
R_{on}	Semiconductor On Resistance
$S_1 - S_6$	CSI Switch Number, Switch One ... Switch Six
$SQ1 - SQ6$	SVM Sequence One ... Sequence Six
T_0, T_1, T_2	SVM Dwell Time Vectors
$tan(\delta)$	Capacitor Loss Tangent
t_d	Delay Time
$t_{fu,n}$	Voltage Fall Time at Sample n
θ	Grid Voltage Angle
θ'	Modified SVM Reference Vector Angle
θ_{start}	SVM Reference Vector Angle at the Start of a Given Sector
θ_{ref}	Reference angle, synthesized by the difference between the SVM reference angle and the grid angle.

T_j	Junction Temperature
$t_{ru,n}$	Voltage Rise Time at Sample n
T_s	Sampling Period
v_c	TPWM Carrier
V_F	Forward Voltage Drop
V_g	Grid Voltage (RMS)
V_{GS}	Gate-to-Source Voltage
V_{in}	CSI Input Voltage
V_L	Inductor Voltage
$V_{LL,rms}$	RMS Line-to-line Voltage
v_m	TPWM Modulating Signal
$V_{plat.}$	MOSFET Miller Plateau Voltage
$V_{S,datasheet}$	Datasheet Test Voltage Applied Across the Switch
$V_{Son/off}$	Turn On or Off Voltage Across the Switch
V_{TH}	MOSFET Threshold Voltage
Z_c	Capacitor Impedance
Z_{grid}	Grid Impedance

1 Introduction

1.1 The Global State of Photovoltaic Energy

Renewable energy is a clear solution to greenhouse gas emissions and the climate crisis. However, political and economic factors come into play when discussing the rollout of renewable energy sources. Such topics are discussed in the International Energy Agency's (IEA) "Renewable Energy Market Update" [1] and summarized in the coming text. To begin with, since 2021, solar photovoltaic (PV) system costs have increased and will continue to increase into 2023. Specifically, the cost of polysilicon, steel, copper, aluminum, and freight caused an increase in PV plant costs by 15% in 2022 compared to 2020. Logically, this would be considered a roadblock in the development of PV energy; however, the competitiveness with natural gas and coal has increased.

This is due to a more dramatic increase seen in the price of coal and natural gas themselves. The market update also discusses the fact that the cost of power in countries belonging to the European Union (Germany, France, Italy, and Spain) have seen historic highs, especially since natural gas sets the price of hourly power rates. In these countries, the wholesale cost of electricity is still greater than long-term PV development contracts. Due to these facts, as well as the invasion of Ukraine, these countries have expedited distributed solar PV energy to reduce their dependence on Russia's natural gas and reduce their electricity bills through self-consumption. As a result, Europe has seen an increase in solar energy of 23 gigawatts (GW), 26 GW, and 29 GW in 2021, 2022, and projected for 2023 respectively. China accounts for most of the increase in the PV energy forecast for 2022-2023, with plans of 140 GW of solar energy in 2023 through an investment of 60 billion USD. The driving forces for such plans are the large population, the cost comparison of PV energy to the cost of coal in all provinces, and the goal of reaching 1200 GW of renewable energy by 2030. In the US, new tariffs, PV module availability, and lack of government investments have slowed development, decreasing the PV forecast from 17% to 9% in 2023. However, this still corresponds to an increase of about 25 GW, and an increase in the coming years is still projected. India forecasts an expansion of 15 GW of solar energy in both 2022 and 2023 due to delayed approved commissions not being completed in 2020 due to the pandemic. The Middle East, Africa, and Latin America will also see an increase in energy produced by PV (8.172 GW and 6.633 GW respectively). The driving forces here are generous net metering schemes and favorable economic conditions. On the other hand, ASEAN nations are seeing a decrease in solar energy power additions when compared to the large increase in 2020 due to contract details. The trends in solar energy at a global scale are presented in Fig. 1.1. Each color represents a different country and the amount of solar energy added in the given year in GW. The red line represents the percentage of solar energy to all renewable energies added in that

year. As the line shows, solar energy is one of the largest growing renewable energy sources, accounting for at least 50% of renewable energy growth in 2019-2022 and projected for 2023.

Canada's energy production details are highlighted in a separate report by the IEA called "Canada 2022 Energy Policy Review" [2] as well as "Energy Fact Book" [3] produced by Natural Resources Canada. In recent years, Canada has been in the top 10 countries in terms of primary energy production. Primary energy is defined as energy sources found in nature before any conversion is applied. The breakdown of Canada's total primary energy supply (TPES) in 2019 is as follows: 38% natural gas, 33% oil, 11% hydro, 9% nuclear, 4% coal, 4% biofuels and waste, and 1% renewables (wind, solar, and geothermal). Overall, 76% of TPES is fossil fuels, while 16.2% is renewable. However, in 2020, oil and coal-based power saw a decrease of 9% and 24%, respectively, while solar saw an increase of 4%. Solar energy is reported to be the fastest growing renewable energy source in Canada. Solar energy has increased from 0.3 TWh to 4.3 TWh from 2010 to 2020 and accounts for 0.7% of renewable energy generated and 0.2% of the total final energy consumption in Canada. Growth has slowed in the last 2 years due to weak load growth, electricity surpluses without storage solutions, corporate power purchase agreements, regulated electricity markets, issues with variable renewables and grid integration, policies such as net metering rules, and development and implementation of smart grid technologies. It is also worth noting that Canada already has one of the cleanest electricity generation systems in the world with 83% of electricity coming from clean sources in 2020. The breakdown is 60% hydro, 15% nuclear, and 8% renewable energy (wind, solar,

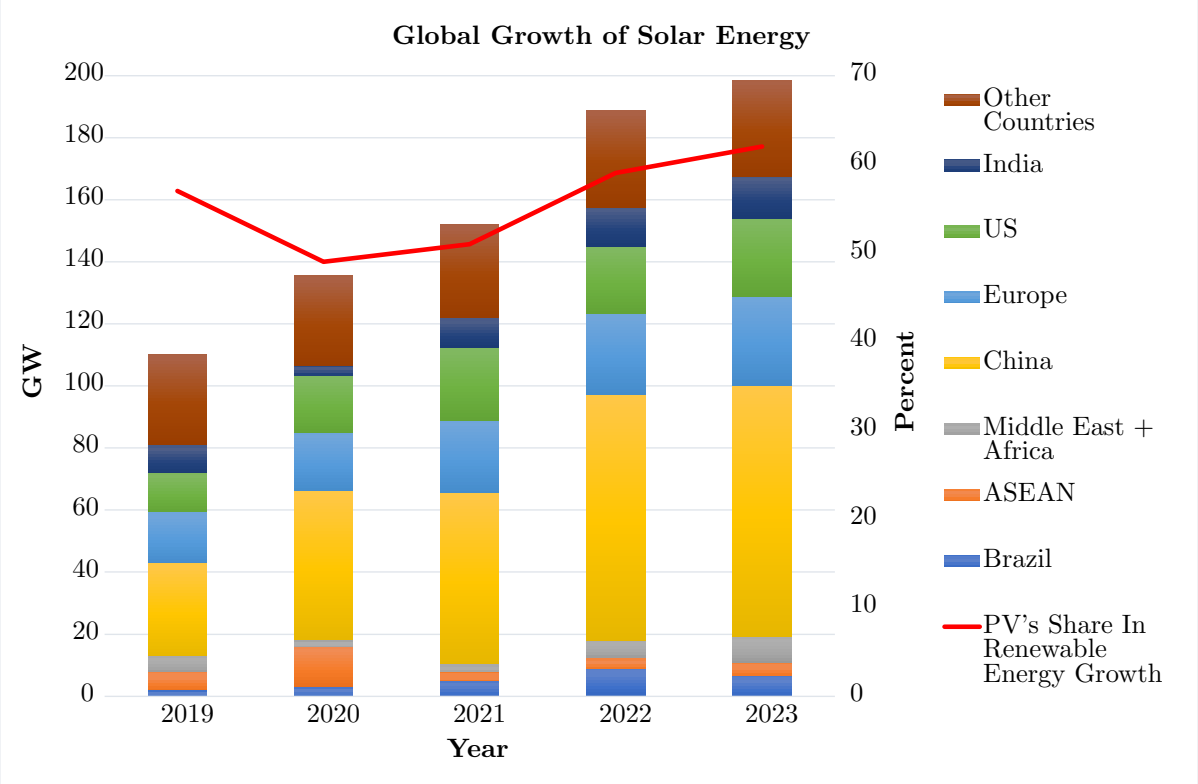


Figure 1.1: Solar energy trends from 2019-2023 based on the data presented in [1].

and bioenergy). The remaining is accounted for by natural gas and combustibles (coal and oil). A driving force behind the investment and growth in renewable energies in Canada is the goal of net zero emissions and decarbonizing their electricity systems by the year 2050. Another factor is emission regulations put in place for industrial consumers. Also, the dominance of hydroelectric power will mitigate risks towards investing in the growth of variable power generation methods, like solar. On the other hand, rooftop solar energy has not seen a lot of use in Canada as electricity rates are affordable based on the average income. There are continued investments in solar energy in Canada with much funding going out. In 2020 19% of the energy-related public budget went toward solar energy and 15% toward R&D of storage and transmission solutions, huge challenges solar energy faces. Another good trend in investments into solar energy is the number of projects and capital invested grows each year. In 2019, 5 projects were funded with $0.7B, in 2020, 7 projects were funded with $0.9B, and in 2021, 20 projects were funded with $3.2B. In Fig. 1.1, Canada will fall under the "other countries" data based on the lower amounts of solar energy generated compared to other countries.

Overall, at a global scale, PV energy production has increased from 110 GW to 150 GW from 2019 to 2021 [1]. Solar energy will continue to see variable amounts of growth, but complete stops in the expansion will not occur. Behind this fact are driving political and economical forces such as regulations, tax incentives, costs (cost per kW, plant costs, and comparisons to other available power generation methods), renewable energy and emission reduction goals, and new technologies (smart grid components or other new developments).

1.2 Photovoltaic Energy Conversion Systems: Components, Topologies, & Commercialized Solutions

To understand where this thesis fits into the solar energy research area, it is important to understand the structure of typical Photovoltaic energy conversion systems (PECS) and typical power ratings, voltage ratings, and common switching frequencies. Since the string inverter topology is the focus of this thesis, extra effort is put into explaining existing "building block" topologies to lay the groundwork for where the CSI fits in. A summary of the following paragraphs can be found in Table 1. Although, one important note from Table 1 is the relationship between power rating and switching frequency. The two have an inverse relationship meaning that at high power, the switching frequency is low and vice versa. This is due to the switching loss generated. At high power, the current and voltage stress the semiconductors see can be very large (thousand volts and hundreds of amps range) making high switching frequency operation impossible due to large switching losses that will deteriorate the efficiency.

In general, PECS consists of several components as seen in Fig. 1.2. First, the PV generator creates a DC current and voltage. From there, a large capacitor controls the voltage ripple [4]. After the filter

capacitor, a DC-DC stage is usually deployed. Its roles are to boost the input voltage provided by the PV generator based on the needs of the inverter stage, perform maximum power point tracking (MPPT), and in some cases, provide isolation depending on the selected topology and grid codes [4]. Typically, another capacitor is used at the output of the DC-DC and input of the inverter to limit ripple [4]. The next stage is the solar inverter that carries out the DC-AC conversion and must do so efficiently. The DC-AC converter also acts as the interface between the system and the grid. Therefore, alongside control, it must perform certain tasks such as grid synchronization, power factor control, and protection schemes [4]. After the DC-AC conversion, a filter is used on the grid side to ensure grid codes are met [4], [5]. Depending on the output voltage level, a low-frequency (LF) transformer may be used to increase the voltage, however, this is a costly and bulky component that has been eliminated in many inverter topologies. PECS can range from low to high power configurations [4], [6], [7], [8]. In [6], Infineon defines residential applications in the range of 1-10kW, commercial applications in the range of 10kW-5MW, and utility-scale applications as anything greater than 5MW. Examples of residential applications include a homeowner using a set of solar panels, commercial applications include PV generators installed at offices or factories to supply additional power to the grid, and utility-scale refers to large-scale solar farms. PECS are classified based on their power rating and application. The four categories include centralized, string, multi-string, and micro-inverter configurations and are shown in Fig. 1.3 [4], [6].

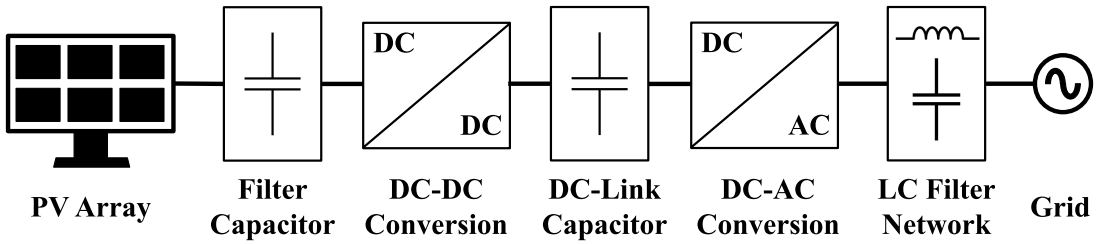


Figure 1.2: Typical photovoltaic conversion system.

The central configuration is the most used, and it utilizes a single inverter to convert the DC voltage generated by several parallel-connected PV strings [4], [6]. On top of converting the DC power to AC, the central inverter is responsible for grid synchronization, reactive power control, and performing MPPT on the entire array of PV modules [4]. An (LF) transformer is used at the output of the inverter for the purpose of elevating the voltage. This configuration requires a bypass diode for each module and a series-connected blocking diode for each string in case of partial shading, module power generation mismatch, and to prevent load behavior in weaker modules [4], [8]. Overall, the benefits of central inverter configurations are the low cost per kW, simple control, and simple structure [4], [6]. On the other hand, some disadvantages are large conduction losses in the blocking and bypass diodes, large DC cable loss due to modules located far away from the inverter, and the MPPT algorithm is not optimized for each PV module [4] [8]. For central inverters, the two-level voltage source inverter (2L-VSI) is the

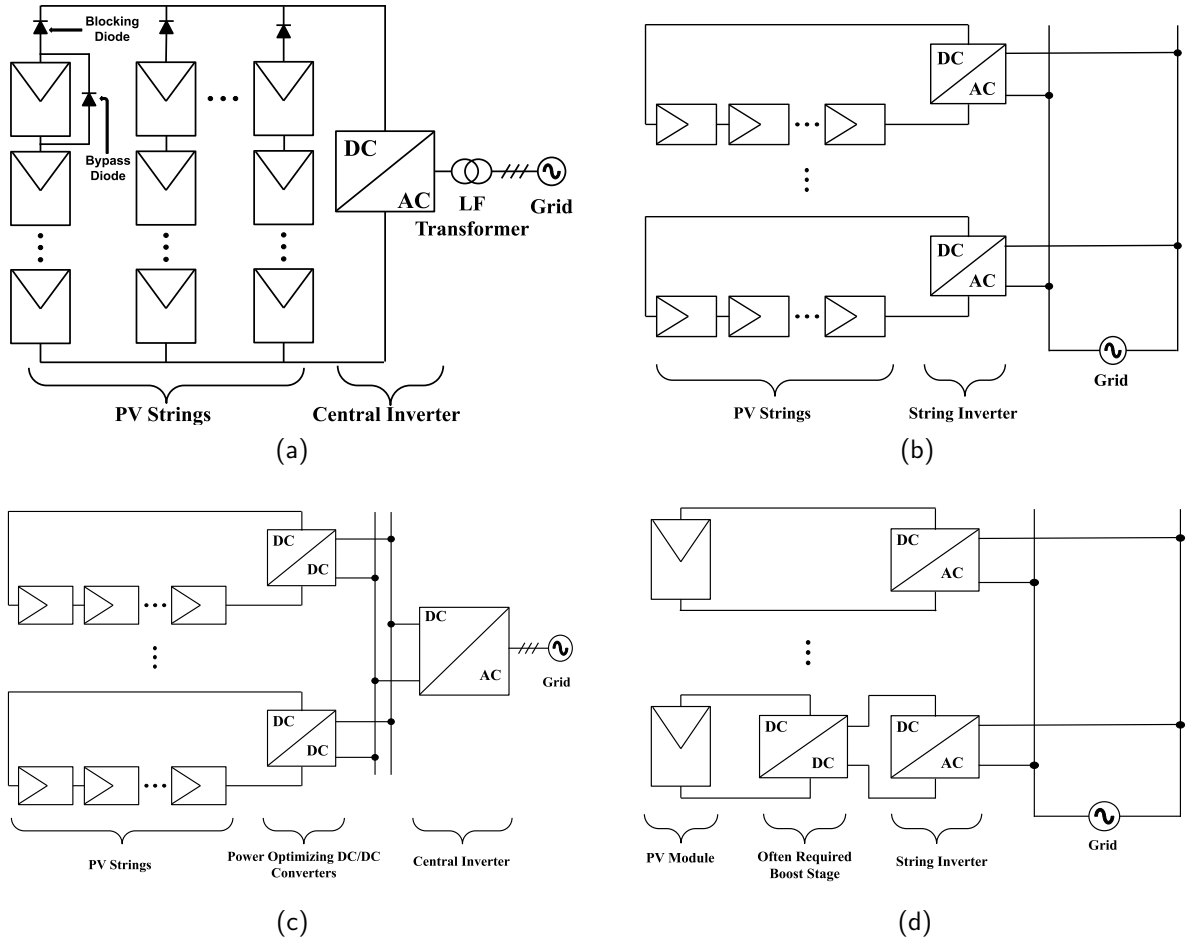


Figure 1.3: The four main configurations for solar energy harvesting: a) Central inverter, b) String inverter, c) Multi-string, d) Mirco-inverter.

most used topology [4]. However, the three-level neutral point clamped (3L-NPC) inverter, and the 3L-T type inverter have been developed to improve efficiency, reduce filter size, and more easily meet strict grid codes [4], [5]. Other configurations include the flying capacitor (FC) inverter and active neutral point clamped (ANPC) inverter shown in Fig.1.4. The typical power rating for central inverters is 600-1.2kW [6].

The string configuration, shown in Fig. 1.3 (b), uses an inverter per PV string [4], [6]. In this case, each PV string has its own MPPT that increases energy collection and minimizes mismatch loss compared to the central inverter configuration [4], [8]. String configurations allow for flexibility when providing galvanic isolation [4]. For instance, isolation can be achieved with an LF transformer interfacing the inverter and grid or if a DC-DC stage is used, a high frequency (HF) transformer can be used [4]. These options are shown in Fig. 1.5. No isolation (transformer-less) configurations are possible, but it depends on isolation standards and the inverter's performance [4]. Removing the LF transformer is desirable as it increases efficiency (the transformer accounts for 2-3% of losses [4]) and power density while decreasing cost. However, some issues can arise when doing this. For example, some inverter configurations can provide leakage current (LC) in grid-tied PV applications [9]. LC is formed by common

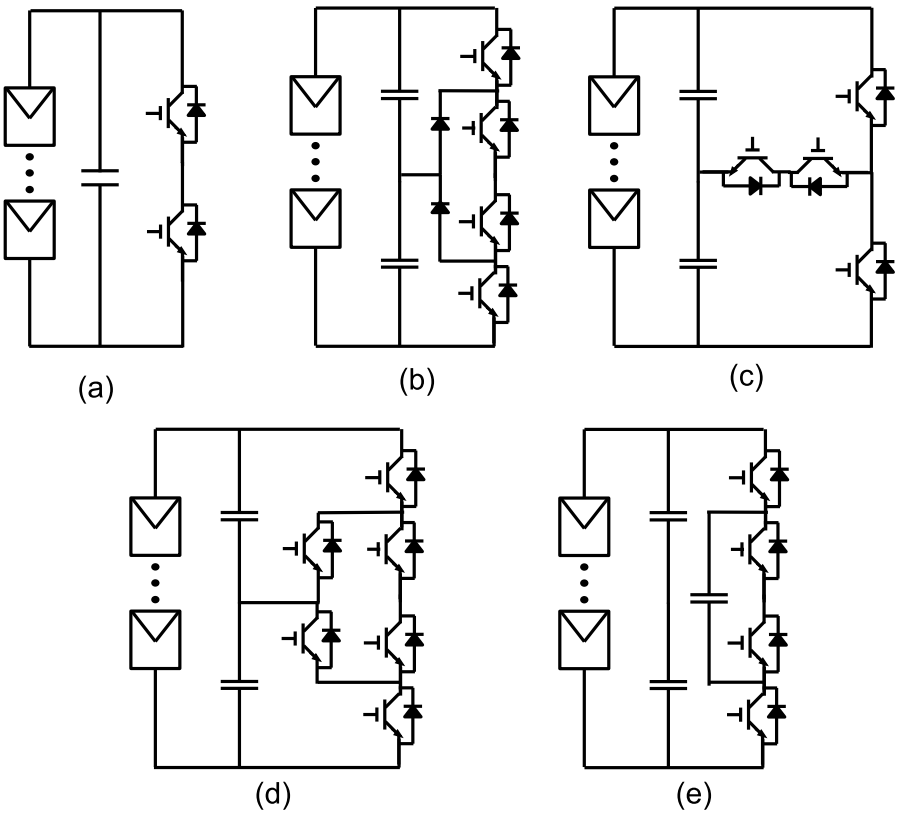


Figure 1.4: Per phase circuit of commercialized central inverter topologies: (a) 2L-VSI, (b) 3L-NPC, (c) 3L-NPC2 (T-type), (d) ANPC, (e) Flying Capacitor (FC).

mode voltage (CMV) that induces current flow between the parasitic capacitance of the PV module and the grid ground [4], [9], [10]. The parasitic capacitance is the result of the PV's grounded metallic frame overlapping with the surface of PV cells [4], [9]. LC affects the grid current quality and converter efficiency [10]. It is desirable to keep CMV constant to eliminate LC, this is typically done by careful design of the modulation scheme or by adding additional components to the configuration (i.e. more semiconductors or filter components) [10]. For string inverters, initially, the most commonly used topology was the H-bridge for single phase and 2L-VSI for three-phase [4], [6], [8]. For these topologies, an LF transformer interfacing with the grid is used for the purpose of LC suppression, without it, the inverter would not be allowed to connect to the grid corresponding to various global standards discussed in [4], [8], [10]. If using bipolar SPWM, a constant CMV is produced. Still, there is also a differential mode voltage (DMV) that decreases the efficiency due to reactive current flow between the DC-link capacitor and grid during free-wheeling periods [4], [8], [10]. In practice split symmetric filters have been implemented to eliminate the CMV in transformer-less configurations (Fig. 1.5) [4], [8]. However, the low-efficiency yields room for improvement. If unipolar SPWM is used, the DMV does not affect the efficiency but now the CMV is not constant, this causes leakage current that makes the topology unusable in transformer-less configurations [10]. The flexibility of isolation is shown in Fig. 1.5. Using a HF transformer increases the power density and decreases the size but since there are multiple power

conversions, and as a result the efficiency is decreased [8].

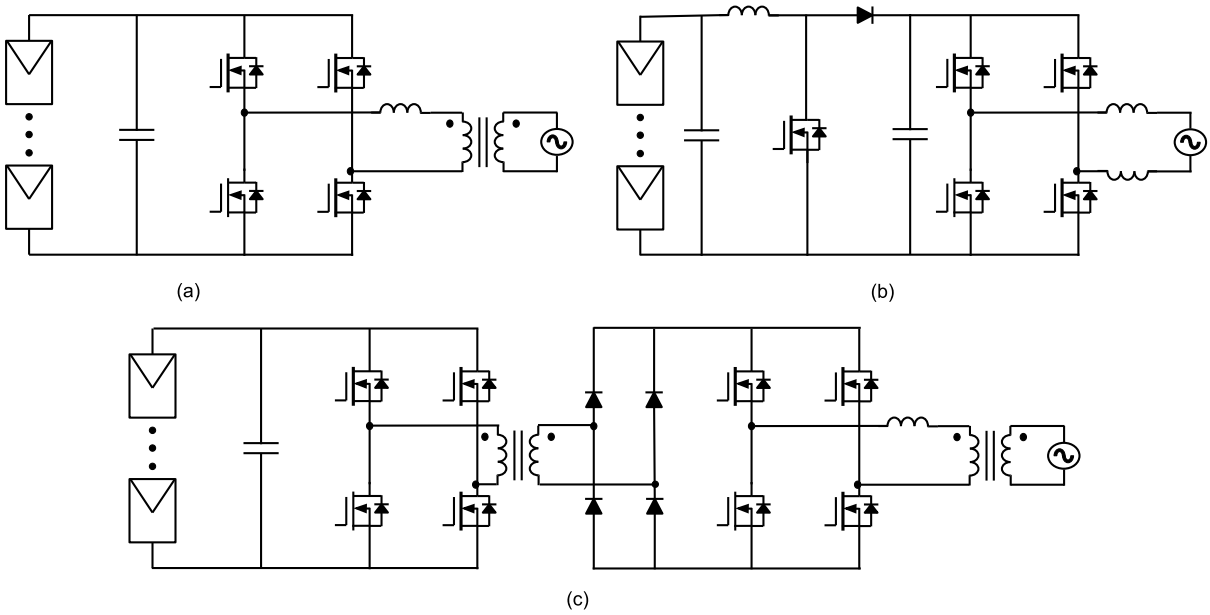


Figure 1.5: Galvanic isolation options for string inverter configurations (single-phase cases are shown for simplicity).

In an attempt to eliminate CMV and improve efficiency, the H5 and highly efficient and reliable inverter concept (HERIC) configurations were created [4], [10]. Both configurations create "decoupling" during freewheeling periods [4], [10]. The H5 achieves DC-decoupling while the HERIC achieves AC-decoupling [8], [10]. This overcomes the problem of reactive current flow between the grid and DC-link and significantly reduces common mode voltage [4], [7], [8]. It is also worth noting that decoupling the DC voltage generated by the PV modules from the inverter rail voltage is a desirable characteristic for the operation of the inverter, it enables a wide range of input voltages and improves the grid control performance [4]. It also allows for the use of different PV module technologies and placements [4]. One downfall to these configurations is uneven loss distribution resulting in a more complex cooling system design [8]. Further methods of decoupling were studied and resulted in the H6D1 configuration [4], [7], [8], [10]. By introducing a switch on the negative DC bus bar and adding a diode across the DC bus to enable different modulation schemes, DC-decoupling is achieved. However, this time even loss distribution among the switches is achieved [4]. A downside to this topology is the efficiency due to four switches conducting at certain instances [4], [8]. In turn, the H6D2 configuration was created to lessen losses through clamping at half of the DC-link voltage [4]. Many additional topologies based on the decoupling idea in full-bridge converters have been proposed and are highlighted in [7], [8], and [10].

With the LC issue having many solutions and the fact that CMV is naturally suppressed in half-bridge configurations, a new focus on increasing the power quality was considered. This resulted in neutral point clamped inverters like the NPC and ANPC also shown in Fig. 1.4 [4], [7], [10]. As mentioned, these topologies have seen use in PV transformer-less applications due to the removal of

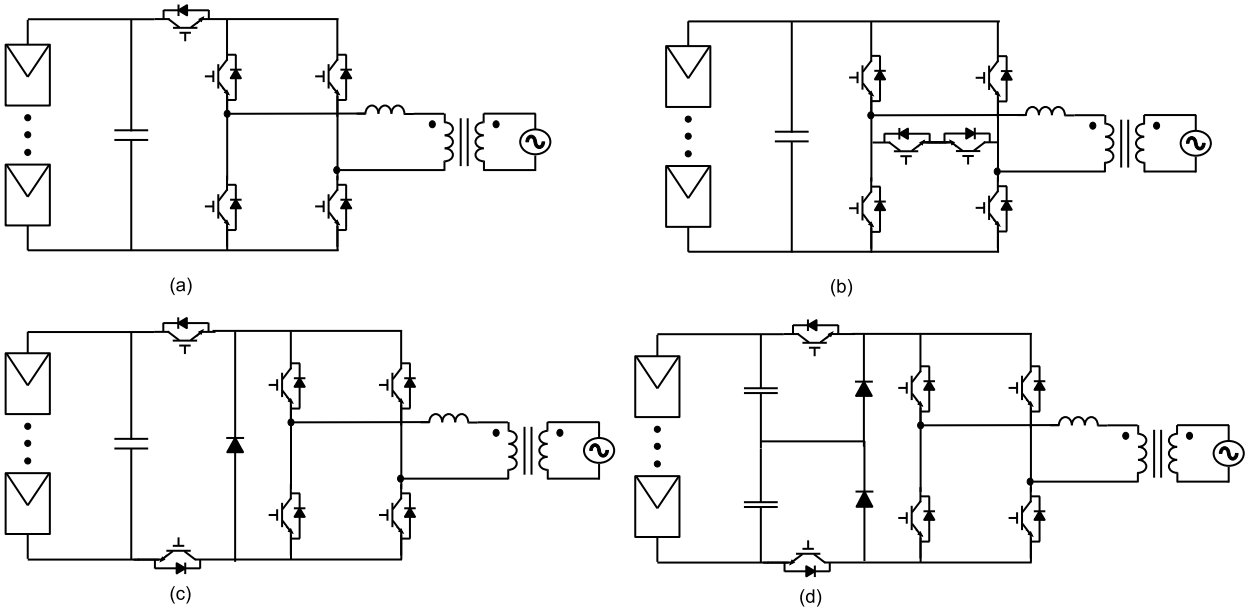


Figure 1.6: Decoupling type inverter solutions: (a) H5, (b) HERIC, (c) H6D1, (d) H6D2.

leakage currents through a naturally occurring constant common-mode voltage [4]. Constant CMV is also caused by the fact that the neutral point of the grid is tied to the neutral of the DC-link for these specific topologies [4]. Other advantages of this topology include three voltage levels resulting in higher power quality and downsizing of the filter capacitor, reduced voltage stress, and reduced dv/dt [4], [10]. The disadvantages include uneven loss distribution and low reliability through high short-circuit risk [10]. Due to these issues, the T-type converter was proposed [4], [10]. This configuration reduces the amount of conducting switches, produces three voltage levels, and corrects the uneven loss distribution further but doubles the voltage stress of the switches [10]. Again, many additional inverters based on half-bridge configurations are highlighted in [10].

Realizing the potential of multilevel inverters to improve power quality, increase efficiency through lowering the switching frequency, and reduce the filter size requirements in PV interfacing yielded the creation of the 5L-HNPC [4]. The main advantage of course was the additional voltage levels, but this configuration requires specific modulation and symmetrical filtering to eliminate CMV [4]. Another example of a commercialized multilevel inverter for PV applications is the cascaded H-bridge (CHB) [4], [7]. This converter creates thirteen voltage levels by using asymmetric voltage sources and has the mentioned benefits of a multilevel inverter [4]. However, additional bypass switches are required to reduce CMV, due to asymmetric voltage sources, the loss distribution is uneven, and the generation and control of the independent voltage sources raise some technical challenges [4]. Currently, multilevel inverters are seeing a lot of research interest. While not a new topic by any means, new topologies are derived from NPC, CHB, and flying capacitor (FC) configurations [4]. Some new topologies are highlighted in [5], [7], [8], and [10].

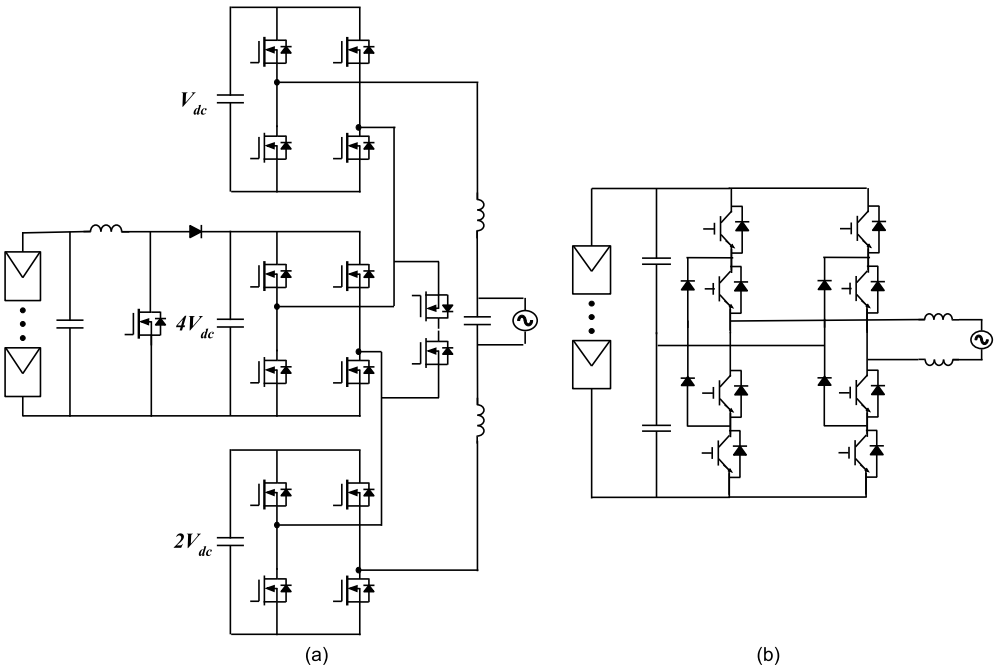


Figure 1.7: Multilevel inverter solutions: (a) Asymmetric CHB, (b) 5L-HNPC.

The multi-string configuration adds a DC/DC converter per PV string for power optimization and uses a single inverter [6]. Essentially, this is the combination of the string and the central inverter configuration [4], [8]. This configuration minimizes the effects of module mismatch and partial shading and decouples the PV side from the inverter DC-link [4], [8]. The same inverter topologies discussed for the string configuration can be used for multi-string as well [4], [7]. A simple boost converter or HF-isolated DC-DC converter (see Fig. 1.5) is typically used for the DC-DC conversion stage based on the PV technology and isolation requirements [4]. Although multi-string configurations have more converters, the installation and maintenance are reported to be quite simple making them used frequently in residential and commercial applications [8].

Moving on, the micro-inverter configuration uses one DC/AC inverter per PV module (each individual solar panel) [4], [6]. Mismatch losses are eliminated, and a higher energy yield is achieved [8]. It also often needs a DC/DC conversion stage due to the low output voltage of individual PV generators (typically <50V) [4], [8]. Again, the DC-DC stage will also be responsible for MPPT and in most commercialized cases, provide isolation [4]. The most used DC-DC converter is the flyback converter [4]. One main drawback of this configuration is the multiple voltage conversions. As a result, multiple DC-DC converters are often used in parallel to lessen the current through the boost stage semiconductors and downsize passive components [4]. However, micro-inverter configurations as a whole have not seen much use mainly due to the high cost per kW due to the high component count of semiconductors and control equipment like sensors and gate drivers [4], [8].

Table 1: PECS typical power, voltage, switching frequency, and topologies used. As well as pros/cons and applications [4], [6], [7], [8], [10].

Configuration	***Ratings***	***Topologies***	***Pros/Cons***
Centralized	PV Voltage: 550V, 850V, 1000V,1500V Power: 600-1250kW Grid Voltage: 320-690V f_{sw}: 2-4kHz	2L-VSI ANPC 3L-NPC1 NPC2 (T-type) FC	• Structure: Simple, low number of components, single LF XFMR. • Control Complexity: Low (one controller). • Power Optimization: Low (MPPT applied to PV string). • Efficiency Drawbacks: Diode conduction loss, mismatch losses, DC cable loss. • Cost/kW: Low.
String	PV Voltage: 600, 1000, & 1500V Power: 1-200kW Grid Voltage: 360-800V f_{sw}: 20-35kHz	DC/DC: Boost (Single or Dual). DC/AC Single Phase: H-bridge, H5, H6, and HERIC. DC/AC Three Phase: 2L-VSI, NPC1, NPC2 (T-type), ANPC, H6D1, H6D2, multilevel NPC, 5L-HNPC, and CHB.	• Structure: Module, high component count, multiple XFMRs if isolation is required, isolation is flexible. • Control Complexity: High (Each inverter requires its own grid control system). • Power Optimization: Medium (MPPT applied to each PV string). • Efficiency Drawbacks: Multiple XFMRs. • Cost/kW: Medium.
Multi-string			• Structure: Module, medium component count, isolation is achievable through each DC-DC stage, meaning an LF XFMR may not be required. • Control Complexity: Low (A single grid-side control system). • Power Optimization: Medium (MPPT applied to each PV string). • Efficiency Drawbacks: High DC power transmission loss. • Cost/kW: Medium.
Micro-inverter	PV Voltage: 40-80V Power: 200-1500W Grid Voltage: 110/230V f_{sw}: 40-80kHz	DC/DC: LLC and Flyback DC/AC: 2L-VSI Cyclo-inverter	• Structure: Module, highest component count, isolation is achievable through each DC-DC stage, meaning an LF XFMR may not be required. • Control Complexity: High (Each inverter requires its own grid control system). • Power Optimization: Best MPPT performance. • Efficiency Drawbacks: Multiple power conversions. • Cost/kW: High.

1.3 Introduction to Wide Bandgap Devices

The purpose of this section is to provide context to the material level properties that enable improved performance of wide bandgap devices. On top of that, applications, operation range (power and switching frequency), manufacturers and their commercially available products are reviewed. In the final section, the selected semiconductor devices' key loss parameter performance are compared.

1.3.1 Wide Bandgap Device Characteristics

While established silicon (Si) semiconductors (MOSFET, IGBT, GTO, etc) have dominated the power electronics industry for many years based on their functionality, reliability, and adequate efficiency, constant development in semiconductor technology has enabled further improvements. Wide bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN) have superior physical properties that can lead to efficiency, size, and cost improvements [11], [12]. At the same time, Si material has

reached its maximum potential in terms of voltage rating, temperature limitation, switching speed, and other loss-related parameters [13], [14], [15]. Specifically, the highest voltage rating, current rating, and junction temperature for any Si device have been at 6.5kV, 2000A, and 175°C respectively [13].

The main advantages of SiC devices include lower on-state resistance, high frequency operation, and reliable high temperature operation [14], [15], [16], [17]. As a result of implementing SiC devices in a power converter, the system will see advantages. For instance, by enabling high frequency and temperature operation, the power conversion system will see downsizing of passive components and cooling system components [14]. It is important to discuss the material-level properties that enable such advantages seen in SiC devices. First, two polytypes of SiC are available in the market, that is, 4H-SiC and 6H-SiC [15], [16]. The prefixes refer to the stacking sequence and bond shapes which greatly effect the electrical and thermal characteristics of the material [18], [19]. The characteristics of 4H and 6H SiC structures are the most suitable for power conversion applications due to the coming properties and the fact large wafers can be made from these crystal structures [15], [17]. This is a key feature that will drive the availability of SiC up and costs down [12]. In terms of physical properties, SiC has a bandgap energy about 3 times that of Si (Si = 1.12eV, SiC = 3.26eV), this is why SiC devices are known as "wide bandgap" devices [13], [19], [20]. Also, the intrinsic carrier concentration is reduced when transitioning from Si to SiC [16], [18]. These characteristics relate to SiC's ability to operate at high temperature and reduce leakage currents [16], [18], [20]. This can be understood with basic semiconductor physics. To begin with, semiconductors only operate in temperature ranges where the intrinsic carrier concentration is low [18], [21]. Also, as temperature increases, the energy of electrons increases, and they can move to the conduction band causing unexpected/unwanted conduction in the device [14]. Therefore, by observing (1), the expression for the intrinsic carrier concentration, n_i, [18], [21], the larger the bandgap energy, the higher the temperature value can go before the carrier concentration becomes too large and electrons move to the conduction band. As a result, SiC has low intrinsic carrier concentration for junction temperatures up to 900°C compared to Si where the maximum temperature is 150°C [14], [16]. Since the leakage current is directly related to n_i, as seen in (2), the reduction in leakage current is verified.

$$n_i = \sqrt{N_c \times N_v} \times e^{\left(\frac{E_g}{2kT_j}\right)} \tag{1}$$

$$J_s = q{n_i}^2 \left(\frac{1}{N_D}\sqrt{\frac{D_p}{\tau_p}}\right) \tag{2}$$

Next, the electron saturation velocity is doubled in SiC material [15], [16], [19], [20]. This parameter is a measure of how quickly a charge carrier can move through the device at a worst-case situation (a high electric field) and is directly related to the switching speed of the device [15], [21]. Therefore, since this velocity is greater in SiC, there is a reduction in switching loss and higher frequency operation is enabled [15], [16]. This characteristic also enables quicker depletion region discharge times, greatly

decreasing the reverse recovery time and current in WBG diodes [15]. Continuing, the critical electric field seen in Si is 10 times less than that of SiC [12], [13], [15], [19], [20]. It is known that the critical electric field is directly proportional to the breakdown voltage of the device [15], [18], [21]. This makes devices with higher breakdown voltages achievable [15], [17]. As of 2023, the highest value commercially available is 1700V but MOSFETs rated for 3300V are being tested as seen in [22]. One advantage of this will be the elimination of series-connected switches commonly seen in power electronic topologies [5]. In turn, this will ease some design challenges that arise with series connected switches such as gating signal timing and improved efficiency. Another benefit of the higher critical electric field is a decrease in on-state resistance. This relationship can be seen in (3) [15], [16], [19], [21]. Further, (4) and (5) are derived in [15] and show the relationship between the breakdown voltage and the on-state resistance, R_{on}. The results show that for the same breakdown voltage, the on-state resistance has the potential to be decreased by a factor of 61.1 that of Si. Due to the increase in the electric field value, higher doping levels and thinner layers can be achieved [15]. This implies the size of SiC devices can be smaller than its Si counterpart. On top of that, these characteristics also contribute to the reduction of on-state resistance [15]. R_{on} is decreased due to the decrease in drift layer resistance [14]- [16]. R_{on} is decreased due to the decrease in drift layer resistance [15], [19]. Specifically, the drift layer area, thickness, and capacitance are decreased by a factor of 626, 11, and 46 respectively at room temperature [16].

$$R_{on} = \frac{4V_R}{\varepsilon_s \mu_n {E_C}^3} \tag{3}$$

$$R_{on,\ \ Si}\left(\Omega.cm^2\right) = 5.93 \times 10^{-9} {V_R}^5 \tag{4}$$

$$R_{on,\ \ SiC}\left(\Omega.cm^2\right) = 97 \times 10^{-12} {V_R}^5 \tag{5}$$

Lastly, the thermal conductivity of Si is $1.31\frac{W}{cm}K$ while for SiC it is about $5\frac{W}{cm}K$ [15], [16], [19], [20]. Equation (6) shows the inverse relationship between thermal conductivity and the thermal resistance (junction to case) of a given device [15]. As a result, since thermal resistance will be reduced in SiC, the temperature produced by the junction can be easily passed to air and a simpler cooling system can be used. Thermal conductivity is a measure of how quickly a device increases in temperature, meaning SiC devices' junction temperature will increase slower than Si devices when producing loss [15]. Table 2 shows the discussed properties of Si and SiC material along with the related advantage.

$$R_{th,jc} = \frac{d}{\lambda A} \tag{6}$$

Table 2 also shows the properties of GaN. It should be noted that the same advantages apply. However, GaN has a slightly higher bandgap energy, critical electric field, and saturation electron velocity [15], [16], [19]. This implies that GaN material allows for further reduction in switching loss, lower on-

state resistance, and higher voltage ratings. However, GaN has poor thermal conductivity, meaning the on-state resistance will increase significantly with temperature increases. As a result, cooling system design is crucial when working with GaN devices.

Table 2: Physical properties of Si, SiC, and GaN along with their advantages [15], [16], [18], [19], [20].

Parameter	***Si***	***4H-SiC***	***GaN***	***Advantages***
E_g- Bandgap Energy (eV)	1.12	3.26	3.4	Higher temperature operation and reduced leakage current.
V_s- Saturated Electron Velocity ($\frac{cm}{s}$)	1×10^7	2×10^7	2.7×10^7	Reduced switching loss enabling higher switching frequency operation
E_c- Critical Electric Field ($\frac{V}{cm}$)	3×10^5	2.5×10^6	3×10^6	Lower on-state resistance and higher voltage rating.
k- Thermal Conductivity ($\frac{w}{cm}K$)	1.31	4.9	1.2	Better ability to sink heat causing reduced cooling system requirements.

1.3.2 Applications, Manufacturers, & Commercially Available Wide Bandgap Devices

Fig. 1.8, shows the capable power and switching frequency range of each technology compiled from data presented in [13], [23], [24], [25], [26]. Please note that this data is based on the theoretical limitations/potential of the technology, not necessarily what is available in the market. The figure shows that Si technology can be used in the range of 1-10 MW applications, with the switching frequency range being from tens of hertz to a maximum of 100 kHz for low power applications.

Currently, there are many manufacturers of WBG based devices. Infineon, ROHM, STMicroelectronics, Onsemi, Toshiba, Wolfspeed (Cree), Allegro Microsystems, TT Electronics, Mitsubishi Electric, GeneSiC Semiconductor, GaN systems, and Littlefuse Inc are some examples. The following tables will highlight the products commercially available which will shed some light on the current applications of SiC and GaN. Table 3 shows a breakdown of five manufacturers' discrete SiC MOSFET products. It should be noted that the maximum voltage rating currently is 2000 V achieved by Infineon. The maximum operating junction temperature across all manufacturers is currently 175°C. The minimum on-state resistance achieved at room temperature and 1200 V is 12 $m\Omega$ achieved by Onsemi but the other manufacturers presented are very close. The typical output capacitance is shown since it is a dominant factor in switching loss. The values range from tens to low twenties of pF. Comparing this to fast-switching Si devices that have a minimum value of 55 pF. These manufacturers also offer module SiC configurations. The configurations include boost, parallel boost, series connected SiC MOSFETs, full bridge, H-bridge, half-bridge rectifier, ANPC, and T-type. Since manufacturers have made these configurations, it is an indicator that they are widely used in industry.

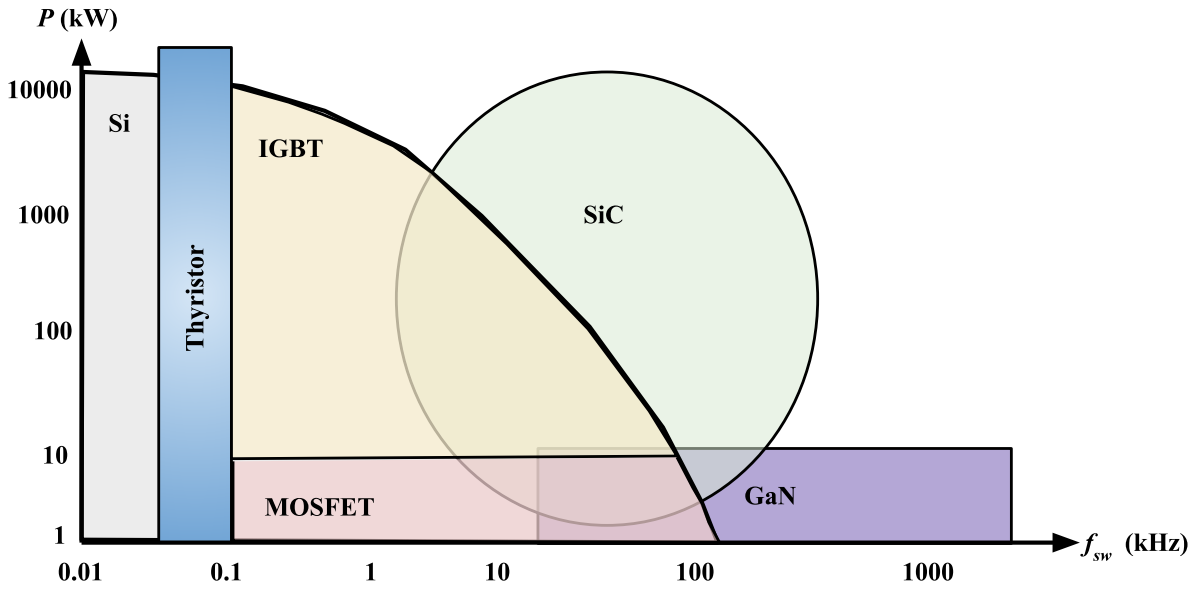


Figure 1.8: Typical power and switching frequency range of operation for various semiconductor technologies [13], [23] - [26].

Table 3: Commercially available discrete SiC MOSFETs [27], [28], [29], [30], [31].

Manufacturer	***Voltage Ratings (V)***	***Max. Operating Temperature (°C)***	***Typ. On-Resistance (mΩ) @ $T_j = 25°C$, $V_R = 1200V$***	***Output Capacitance (pF)***
Infineon	650, 1200, 1700, 2000	175	14	23
Rohm	650, 750, 1200, 1700	175	18	27
STM	650, 750, 900, 1200, 1700	175	13	11.3
Onsemi	650, 750, 900, 1200	175	12	11
Wolfspeed	650, 900, 1000, 1200, 1700	175	16	20

Table 4: Commercially available discrete SiC diodes [27], [28], [29], [30], [31].

Manufacturer	***Voltage Ratings (V)***	***Max. Operating Temperature (°C)***	***Typ. Forward Voltage (V) @ $T_j = 25°C$, $V_R = 1200V$***	***Total Capacitive Charge (nC)***
Infineon	600, 650, 1200	175	1.4	14
Rohm	650, 1200	175	1.4	17
STM	600, 650, 1200	175	1.45	12
Onsemi	650, 1200, 1700	175	1.45	15
Wolfspeed	600, 650 1200, 1700	175	1.4	11

Table 5: Commercially available discrete GaN devices [32], [33].

Manufacturer	***Voltage Ratings (V)***	***Max. Operating Temperature (°C)***	***Typ. Forward Voltage (V) @ $T_j = 25°C$, $V_R = 1200V$***	***Total Capacitive Charge (nC)***
GaN Systems	100, 650	175	1.4	14
Infineon	400, 600	175	1.4	17

1.3.3 Performance Comparison of New and Conventional Semiconductors

The following figures (Fig. 1.9-Fig. 1.13) show comparisons between key datasheet parameters of the IKW30N65ES5 IGBT by Infineon, STY112N65M5 fast-switching Si MOSFET by STMicroelectronics, C3M0025065K SiC MOSFET by Cree, and GS66516 GaN high electron mobility transistor (HEMT) by GaN systems. More detail on why these devices were selected is provided in Chapter 2. Fig. 1.9 (a) shows the variation of the normalized on-state resistance with temperature for the Si, SiC, and GaN MOSFETs. It can be noted that the SiC MOSFET's on-state resistance has a negative temperature coefficient for low temperatures. This is the result of a resistive channel with a negative temperature coefficient and a drift layer region with a positive temperature coefficient [23]. However, across the entire temperature range, the SiC devices' on resistance stays relatively constant at around a normalized value of 1-1.2. In contrast the Si MOSFET has a positive temperature coefficient throughout the whole temperature range. At high temperatures, the on-state resistance at least doubles. Similarly, the GaN HEMT is quite sensitive to changes in temperature. It has very comparable performance to that of the Si MOSFET. The advantage of the GaN device can be seen in Fig. 1.9 (b). At room temperature, the GaN device's on-state resistance is resilient to changes in drain current over its entire operating range. The on-state resistance when varying the current of the Si and SiC MOSFET are very comparable at room temperature. The advantage of SiC comes when the temperature is increased which is common in all applications.

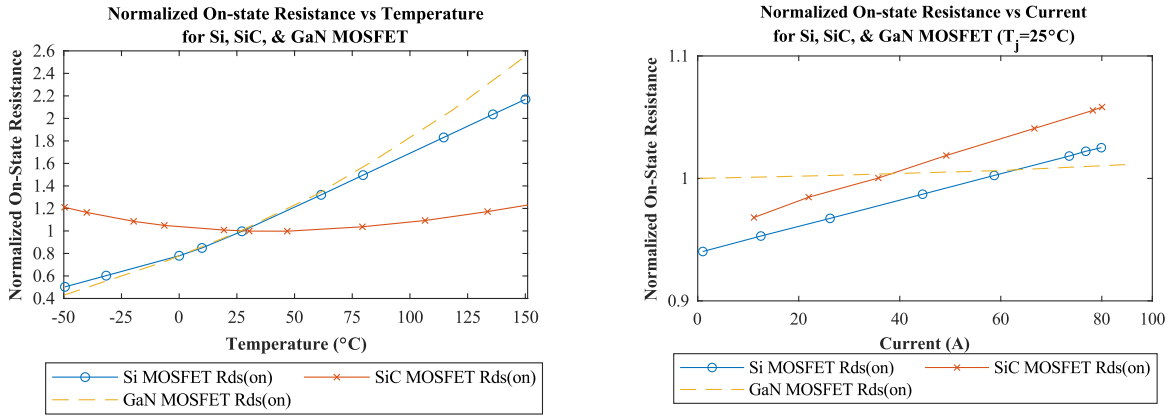


Figure 1.9: On-state resistance characteristics of the STY112N65M5 Si MOSFET, C3M0025065K SiC MOSFET, and GS66516 GaN HEMT with V_{gs} = 10 V, 15 V, and 6 V respectively. (a) With varying temperature (I_{ds} = 40 A), (b) With varying I_{ds} ($T_j = 25^{\circ}C$).

Fig. 1.10 (a)-(d) show the switching energy versus drain current at room temperature and maximum device operating temperature for each device (with other parameters defined in the figure footing). It should be noted that the switching energy of the GaN, IGBT, and Si devices are scaled linearly with

the gate resistance value provided in the datasheet and the required gate resistance of 2.5 Ω for a fair comparison. This method will be discussed in more detail in Chapter 3. The results show that the IGBT has the worst switching loss performance across all current values, followed closely by the Si MOSFET. On the other hand the WBG devices remain below 200 µJ. Having a closer look at the WBG devices' switching energy performance (Fig. 1.10 (b)) shows that the turn-on energy of the SiC MOSFET and GaN HEMT have a linear relationship with the current while the turn-off energies have a more parabolic reaction. The overall reduction in switching loss between the Si devices (MOSFET and IGBT) and WBG devices is due to the absence of tail current caused by the accumulation of minority carriers (WBG material is unipolar and a majority carrier) [20], [23].

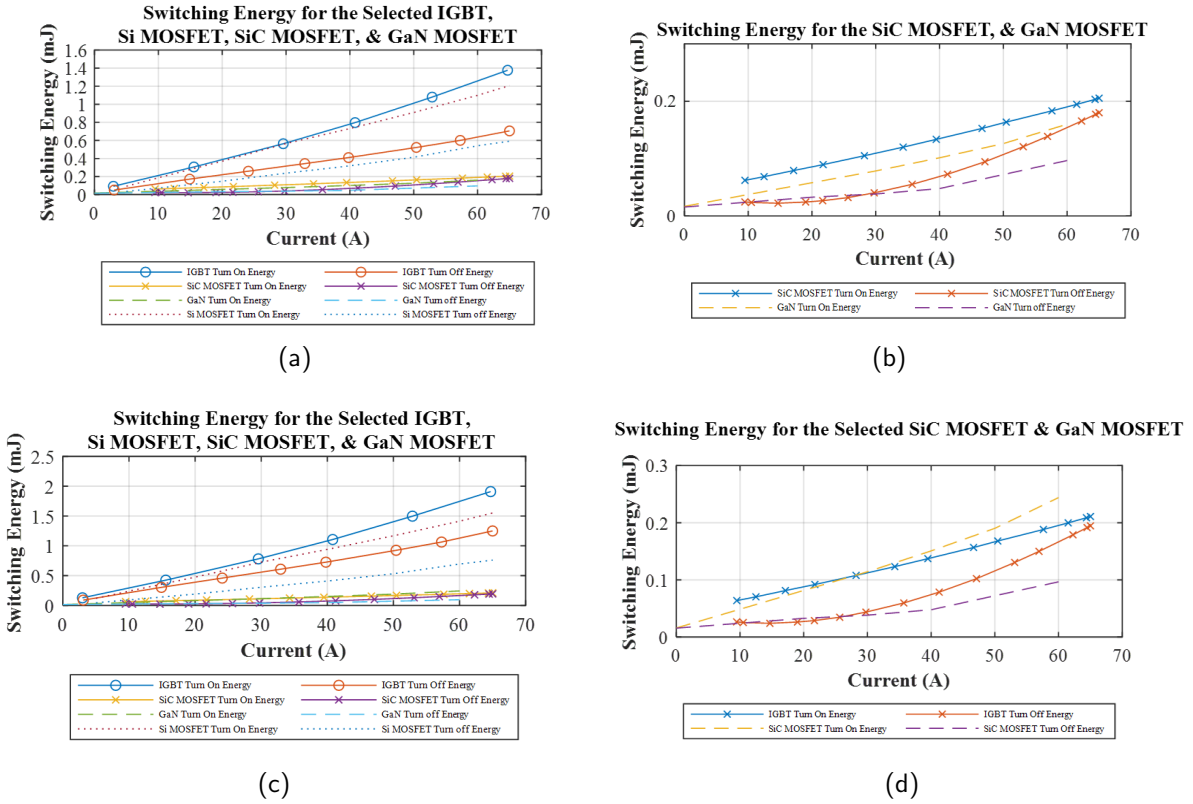


Figure 1.10: Switching energy versus drain current for the STY112N65M5 Si MOSFET, C3M0025065K SiC MOSFET, IKW30N65ES5 IGBT, and GS66516 GaN HEMT with V_{gs} = 10 V, 15 V, 15 V and 6 V respectively, $V_{dd} = 400V, R_G = 2.5\Omega$. (a) $T = 25°C$, (b) Zoomed in version of the WBG devices in (a), (c) $T = max.$, (d) Zoomed in version of the WBG devices in (c).

When the temperature is increased to the device's maximum operating temperatures (150° or 175° correspondingly), the Si MOSFET and IGBT turn-on energies increase by approximately 35% while the turn-off energy increases by 30% and 78% respectively. Conversely, the WBG devices maintain values below 250 µJ, a negligible increase in loss. Fig. 1.10 (d) shows the switching energies of the WBG device at their maximum junction temperatures, swept over their operating currents. Fig. 1.11 shows an overview of the switching energies swept across various temperature values. From this, already discussed points can be reinforced.

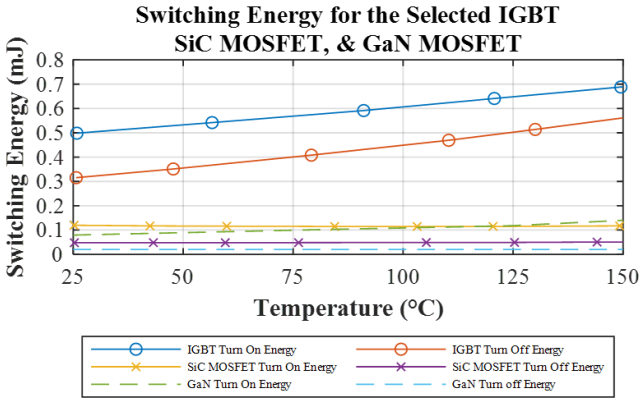


Figure 1.11: Switching energy versus temperature for the IKW30N65ES5 (IGBT), C3M0025065K (SiC MOSFET), and GS66516T (GaN MOSFET) with V_{gs} = 15 V, 15 V, and 6 V respectively, I_d = 30 A, and R_G = 2.5 Ω.

As to be discussed, the mechanism for loss of the IGBT is not defined by on-state resistance, rather the forward voltage drop. Therefore, Fig. 1.12 shows these values for the selected GaN, SiC and IGBT device at room and maximum temperatures in order to compare the technologies. At room temperature the WBG devices have very similar performance and can handle much higher currents while producing a lower voltage drop than the IGBT. Notice, the linear nature of the WBG devices is more desirable than the characterisitic curve produced by the IGBT. At maximum temperature the performance in the SiC device dips a small amount, meaning, a higher forward voltage is produced for lower current operation than that at room temperature. This characteristic is exaggerated further in the GaN device, meaning, it is very sensitive to temperature. A very high voltage drop is created at lower currents for the GaN device at maximum temperature. The IGBT surprisingly performs better at room temperature for currents greater than 75 A but creates a much higher voltage drop in all other regions. When the temperature is increased, the IGBT forward voltage sees an increase more dramatic than the SiC device, but less dramatic than the GaN device. Again, the IGBT would be more efficient at the maximum junction temperature for currents greater than 70 A. However, the fact that the SiC device can operate at a higher temeprature value should be considered.

A method for decreasing the conduction loss used later in this report is the using anti-series connected switches. In this configuration, the '3rd quadrant channel' or 'reverse conduction channel' of the lower switch is used to conduct the DC-link current. The following figure shows a comparison of the 3rd quadrant voltage drop caused by the selected SiC MOSFET. It will be compared to the other lower switch solutions. This includes the IGBT body diode, Si diode, SiC schottky barrier diode (SBD), and the GaN HEMT reverse conduction channel voltage drop. The first to note in Fig. 1.13 (a) is that the GaN reverse conduction channel produces a high voltage drop, much higher than other solutions presented. It is also very sensitive to temperature changes. Increasing the temperature creates a much higher voltage drop for the GaN reverse channel. Observing 1.13 (b), the IGBT body diode, Si diode, SiC

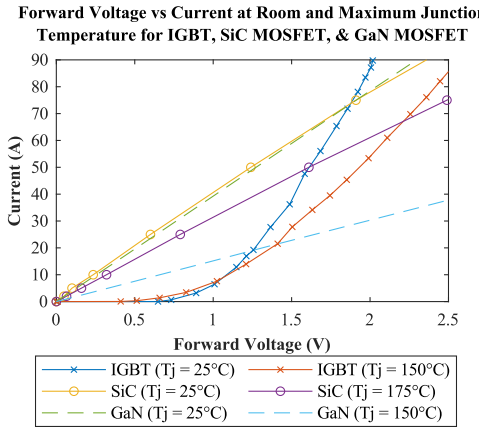


Figure 1.12: Forward voltage of the IKW30N65ES5 (IGBT), C3M0025065K (SiC MOSFET), and GS66516T (GaN MOSFET) at room and maximum operating temperature.

SBD voltage drop is inversely related to the temperature (negative temperature coefficient). So as the temperature increases, the forward voltage drop produced by the respective channels decreases. For the IGBT, the performance of the body diode voltage drop does not really change from its room temperature to maximum temperature operation, making it very resilient to temperature changes. The Si diode has the worst performance in the range of 0-70 A at room temperature. However, it has better performance than the SBD and IGBT body diode at maximum temperature. It should be mentioned at this time that while operating at higher temperature may result in lower voltage drops and hence lower losses, there are negative connotations to operating at high temperature. Such as lower reliability/lifetime of the device and more expensive and bulky cooling systems. The SBD performs in a very similar manner to the IGBT body diode but has a lower maximum current value. Finally, the SiC MOSFET's third quadrant channel has a more linear response to increasing current. This results a much lower voltage drop from 0-50 A than the other solutions. The voltage drop produced also has a positive temperature coefficient (see Fig. 1.13).

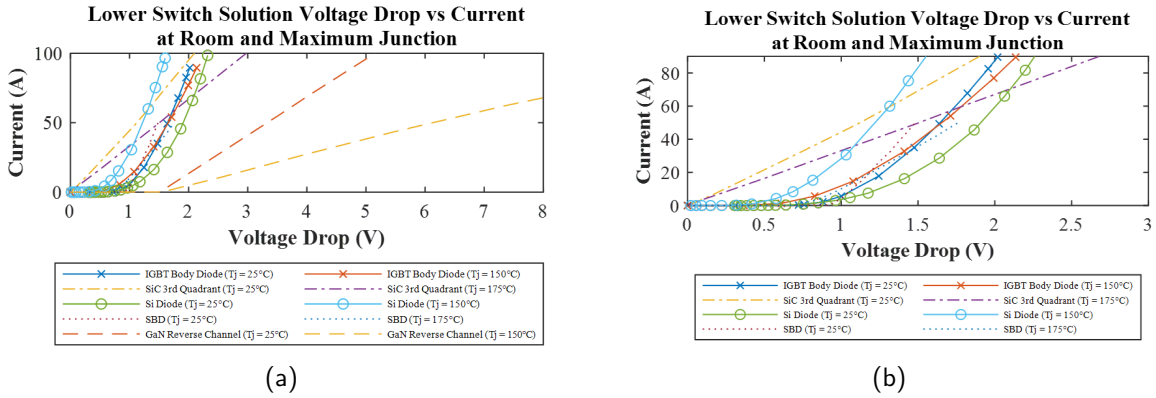


Figure 1.13: Voltage drop characteristics of the RFS60TZ6S Si Diode, FFSH5065A SiC Schottky Barrier Diode, IKW30N65ES5 IGBT Body Diode, C3M0025065K SiC MOSFET 3rd Quadrant Channel (V_{gs} = 15 V), and GS66516 GaN HEMT (V_{gs} = 0 V). (a) All devices, (b) GaN device removed for easier viewing.

2 Introduction to Current Source Inverters

2.1 Introduction to CSI Components

The CSI topology converts DC current to AC current. Instead of producing a defined output voltage like the commonly used VSI, a defined AC current is created at the output. In turn, the voltage is defined by the load (grid, load impedance, etc). That is why it is referred to as a "current first, voltage second" converter. The output of the CSI requires a three-phase capacitor (C_f) that plays two roles in the CSI's operation [5]. One is to filter harmonics in the PWM current (i_w), so they are not seen in the load current (i_s) [5]. The second purpose is to assist in the commutation of the switches [5]. Since the PWM current changes rapidly, the capacitor in each phase provides a path for energy stored in the load inductance [5]. This avoids damage to the switching devices due to overvoltage [5]. On the DC side, a large inductor (L_{dc}) with a voltage source (V_{in}) (rectifier, battery, etc) is used to generate the DC-link current (I_{dc}) and make it continuous, as well as limit the ripple [5]. For switching frequencies around 500 Hz, the DC-link inductor is very large, usually around 0.5 to 0.8 per unit (pu) [5]. Some general advantages of CSIs should be mentioned. First, CSIs are a simple structure containing few components and do not need to use freewheeling diodes [5]. Second, since CSIs produce PWM current, the output produced is free from dv/dt issues seen in VSIs [5]. Third, the DC-link inductor provides reliable short-circuit protection by limiting the rate of change of current which provides more time for protection schemes to begin [5]. The CSI configuration connected to the grid is shown in Fig. 2.1, where L_g and R_g are the line inductance and resistance.

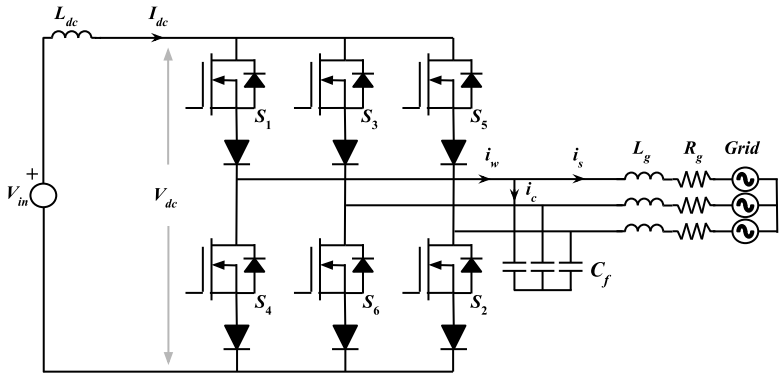


Figure 2.1: Grid-tied Current Source Inverter.

2.2 Review of Reverse Blocking Semiconductors

The semiconductor devices (S_1-S_6) shown in Fig. 2.1 can be any switch capable of reverse voltage

blocking or "reverse blocking" (RB) to avoid interphase short circuits and reverse power flow [5], [34]. More detail on this is provided in the next section. Thyristors are an example of a device with RB capabilities [5]. Examples include silicon-controlled rectifiers (SCRs), gate turn-off thyristors (GTOs), gate-commutated thyristors (GCTs), and integrated gate-commutated thyristors (IGCT). However, these devices are limited to low switching frequencies (as shown in Fig. 1.8), making the CSI bulky [5]. Thyristor-based CSIs are mainly used in high-power motor drives [5]. The circuit symbols for the mentioned thyristors are shown in Fig. 2.2.

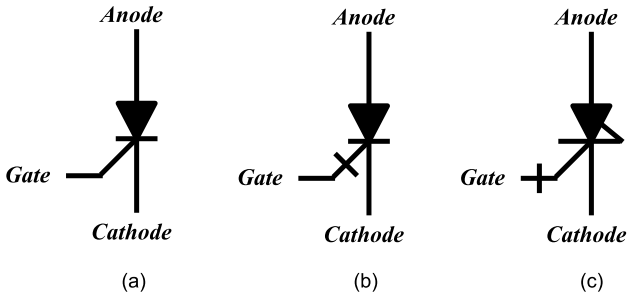


Figure 2.2: Circuit symbols for thyristors: a) SCR, b) GTO, c) GCT/IGCT.

Bidirectional (BD) switches can be used in series with a diode to achieve RB. Combinations of discrete components are commonly classified as hybrid switches [35]. Examples include insulated gate bipolar transistors (IGBTs) with series-connected diodes and MOSFETs with series-connected diodes as shown in Fig. 2.3 (a) and (b) respectively [5], [35]. This can enable switching frequencies in the range of tens of kilohertz [36]. On the downside, adding the diode can add large amounts of conduction loss [35]. As discussed, with further development of WBG devices, SiC MOSFETs and GaN-HEMTs can also be used in series with a diode [35]. Other hybrid configurations are presented in [35], [37], and [38]. The first one to be discussed is common-source (anti-series) MOSFETs [35], [37], [38]. Two options are available based on this configuration. One is to control the upper switch and short the gate and source of the lower switch (Fig. 2.3 (d)) [35]. This uses the lower switch's body diode to achieve reverse blocking. Generally speaking, the body diode of BD switches usually have worse loss characteristics when compared to discrete diodes. However, IGBTs with SiC body diodes are commercially available and can provide value in such a configuration [39]. This will be discussed in more detail throughout the report. The second option is to control both the upper and lower switch, shown in Fig. 2.3 (e). The control must work in such a way that the lower switch behaves as a diode during transient states to achieve RB, and the lower device conducts during steady state to reduce conduction losses. Such a modulation scheme is discussed in detail in [40], where the lower switch is provided with a delayed gating signal relative to the upper switch. This will be discussed in more detail in the coming section on modulation schemes. The next option presented in [35] is the common drain configuration shown in Fig. 2.3 (f). This works in a similar fashion to the common source cell and will not be explained again. The choice between a

common source and drain cell configuration really depends on the connection convenience of the overall circuit as the switching performance is the same [41]. Please note that the MOSFETs in Fig. 2.3 (d)-(f) can be interchanged with other switch options such as IGBTs, GaN-HEMTs, etc [35], [37], [38]. GaN devices do not have a body diode but rather, they are naturally capable of reverse conduction [42]. The reverse conduction channel has similar characteristic curves to that of a diode with no reverse recovery losses (only switching loss is caused by the output capacitance of the device) [42].

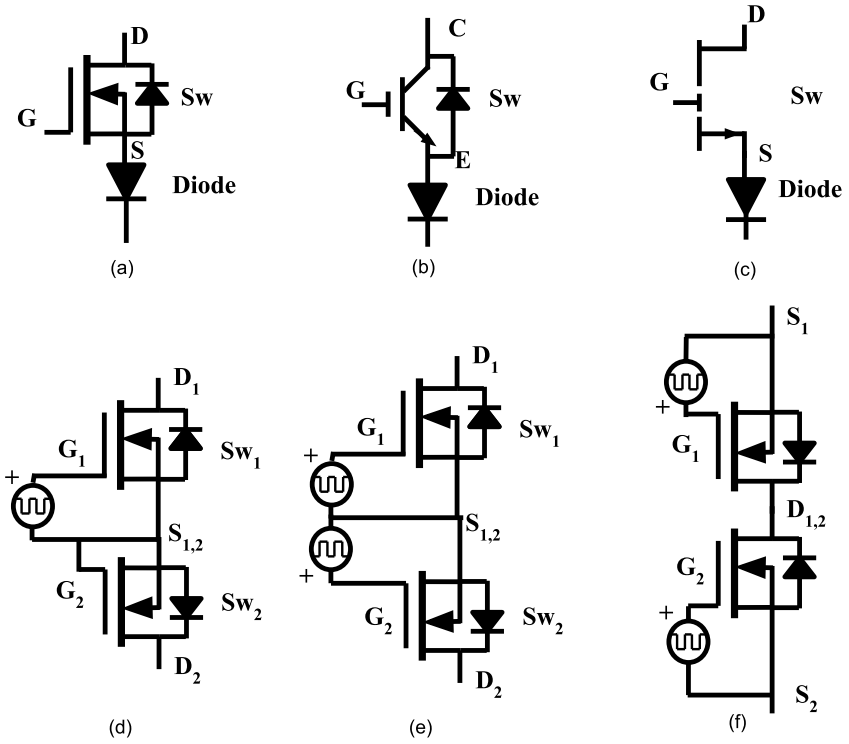


Figure 2.3: Circuit symbols for hybrid RB solutions: a) Si/SiC MOSFET+Diode, b) IGBT+Diode, c) GaN-Hemt+Diode d) Common source, single controller e) Common source, two controllers, d) Common drain.

Single technologies that can handle reverse-blocking have been discussed in theory and are referred to as monolithic switches [35]. An example is reverse blocking IGBTs (RB-IGBT) that have been reported in [43] and [44]. However, higher conduction loss than a single IGBT, less than desirable switching performance, and limited commercial availability has capped their use [35], [44], [45]. Another example of a monolithic switch is seen in [40] and [46]. It is a bidirectional dual-gate GaN device. It is constructed by adding an additional gate structure while sharing the drift region, this way the on-state resistance sees no increase to that of a single switch [46]. High switching frequency operation is achievable since it uses WBG technology. Since there are two gates, based on biasing, different operations can be achieved [40]. By biasing both gates on, bidirectional operation is achieved [40]. When both gates are off, the device acts as anti-series diodes with the ability to block up to 1340V [40]. Finally, when one gate is biased on, and the other is off, the device acts as a diode achieving RB and forward conduction [40]. Monolithic circuit symbols are shown in Fig. 2.4.

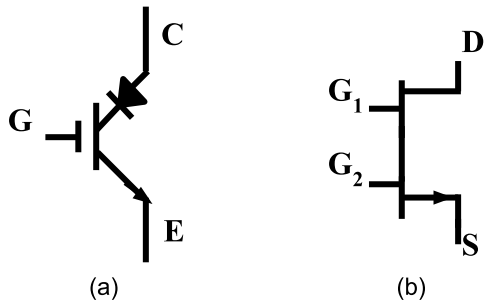


Figure 2.4: Circuit symbols for monolithic solutions: a) RB-IGBT, b) Bidirectional dual-gate GaN device.

2.3 Modulation Schemes

Modulation schemes used for the CSI include trapezoidal pulse width modulation (TPWM), selective harmonic elimination (SHE), and space vector modulation (SVM) [5]. They will be discussed in the coming sections. These modulation schemes are derived from two rules. First, there must always be a path for the DC-link current, this means that at least one upper and lower switch must conduct at any instant [5]. If this is not achieved, high overvoltage will appear on the DC-link inductor and the semiconductors will be destroyed [5]. Second, only two switches can conduct during steady state to achieve the expected operation [5]. If this condition is not met, the DC-link current will be divided among phases causing unpredictable output currents. Fig. 2.5 shows fault conditions. With that in mind, Table 6 shows the only nine valid switching states for proper operation of the CSI. Different switch states are classified as active states or zero states [5]. The difference in the classifications is that an active state provides current to the grid, while a zero vector bypasses the grid, supplying the grid with no current. Therefore, there are six active states and three zero states. For the remaining four switches that are off, the voltage across them (the switch + reverse blocking device) will be equal to the given line-to-line voltage. Fig. 2.7 (a)-(i) shows the equivalent circuit under each switching state along with the voltage stress across non-conducting switches and DC-link voltage.

Table 6: Valid switching states for the CSI with the corresponding current supplied to the load.

Type	***On Switches***	***PWM Phase Current***		
		Phase A	***Phase B***	***Phase C***
Active	S_1,S_6	I_{dc}	$-I_{dc}$	0
Active	S_1,S_2	I_{dc}	0	$-I_{dc}$
Active	S_2,S_3	0	I_{dc}	$-I_{dc}$
Active	S_3,S_4	$-I_{dc}$	I_{dc}	0
Active	S_4,S_5	$-I_{dc}$	0	I_{dc}
Active	S_5,S_6	0	$-I_{dc}$	I_{dc}
Zero	S_1,S_4	0	0	0
Zero	S_3,S_6	0	0	0
Zero	S_2,S_5	0	0	0

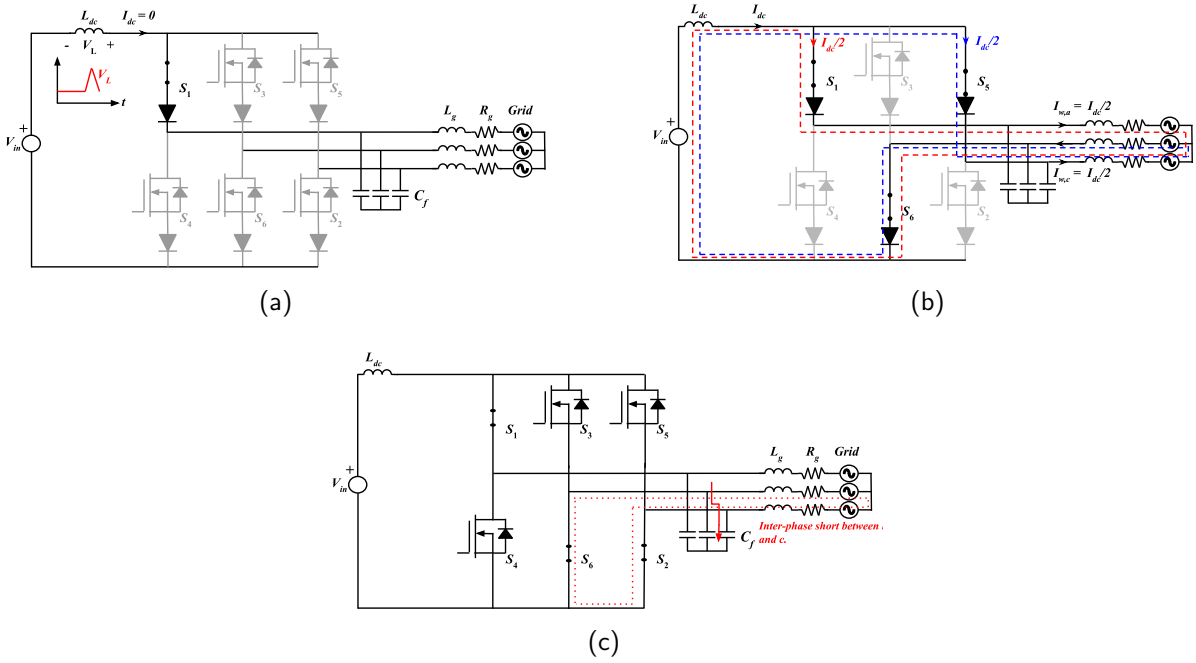


Figure 2.5: CSI faults: (a) One switch on, (b) Two switches on during steady state, (c) No RB switches used, causing inter-phase short during switch transition.

Practically, an overlap between sequential gating signals is implemented in order to ensure a path for the DC-link current is always available [34]. When transitioning from S_1 and S_6 being on to S_1 and S_2, S_6 remains on until S_2 is fully on. The series-connected diodes prevent interphase short circuits between phase B and C. It should be noted that this process is very fast so no current division occurs between the phases. If overlap is not implemented, S_6 may turn off prior to S_2 turning on fully, resulting in no lower switch on, and no path for the DC-link current (Fig. 2.5 (a)). The overlap process is summarized in Fig. 2.6.

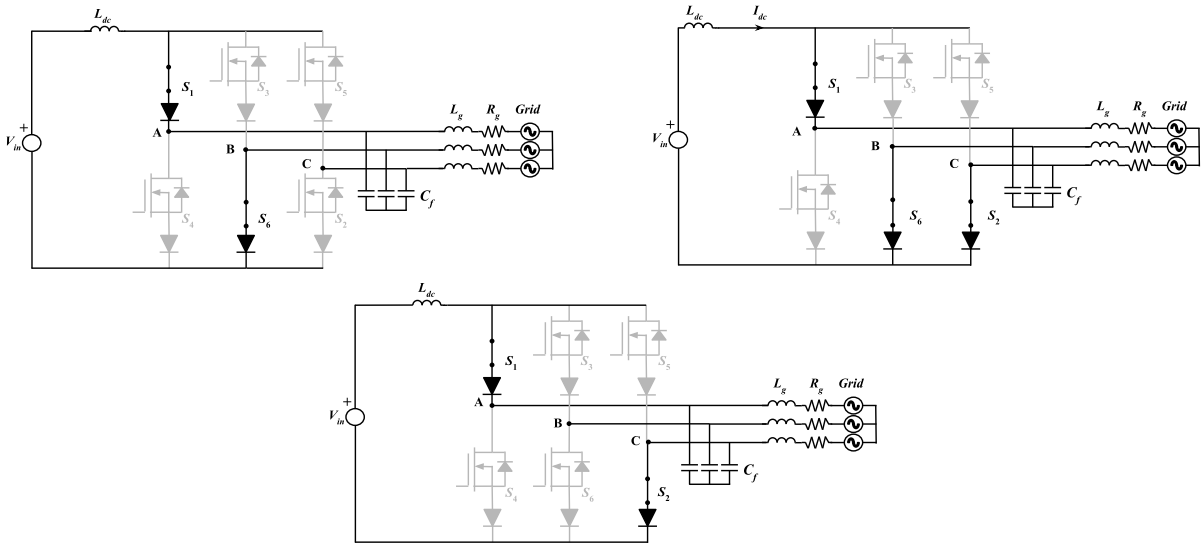


Figure 2.6: Overlap implementation during commutation from S_1,S_6 to S_1,S_2.

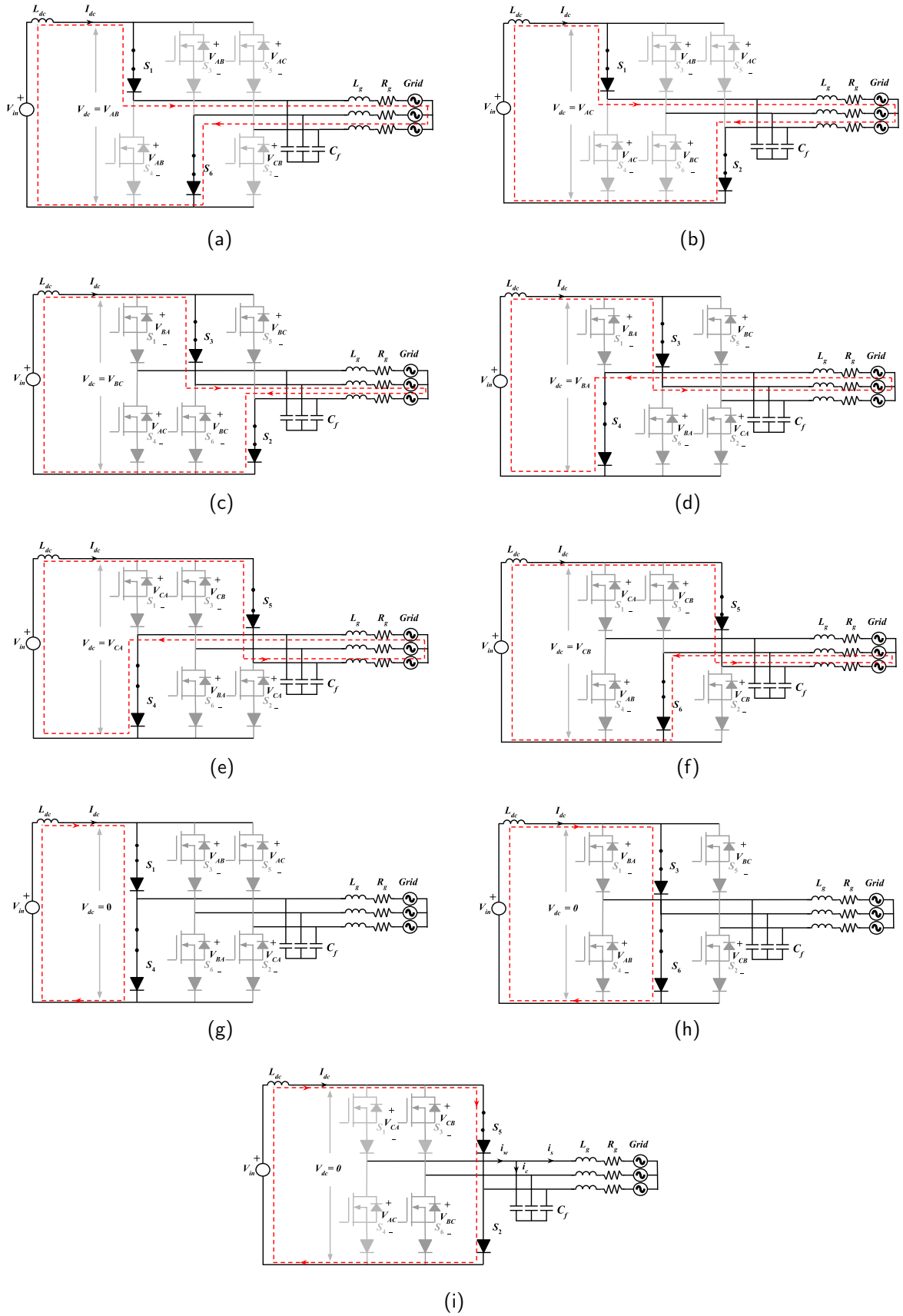


Figure 2.7: Valid switching states for CSI operation with voltage stress and DC-link voltage shown: (a) S_1,S_6, (b) S_1,S_2, (c) S_2,S_3, (d) S_3,S_4, (e) S_4,S_5, (f) S_5,S_6, (g) S_1,S_4, (h) S_3,S_6, (i) S_2,S_5.

2.3.1 Space Vector Modulation

SVM assigns vectors to the switching states as shown in Fig. 2.8. The vector locations can be visualized in the α-β axis as shown in 2.8. The active and zero vectors are stationary while the reference vector, $\vec{I}_{ref.}$, rotates in space at an angular velocity proportional to the fundamental frequency of the inverter [5]. The corresponding switch state is selected based on the location of $\vec{I}_{ref.}$. The duty cycle of a given switching state is known as the 'dwell time'. It can be computed using (7)-(9), where m_a is the modulation index, $\theta^{'}$ is the modified reference vector angle, and T_s is the sampling period. The modified reference vector angle can be computed using (10), where k is the sector number. The range of m_a is from 0 to 1 [5]. It should be noted that only natural sampling SVM (NS-SVM) is considered throughout the report [47]. Conventional SVM is widely discussed in literature and, therefore, not reviewed here [47], [48].

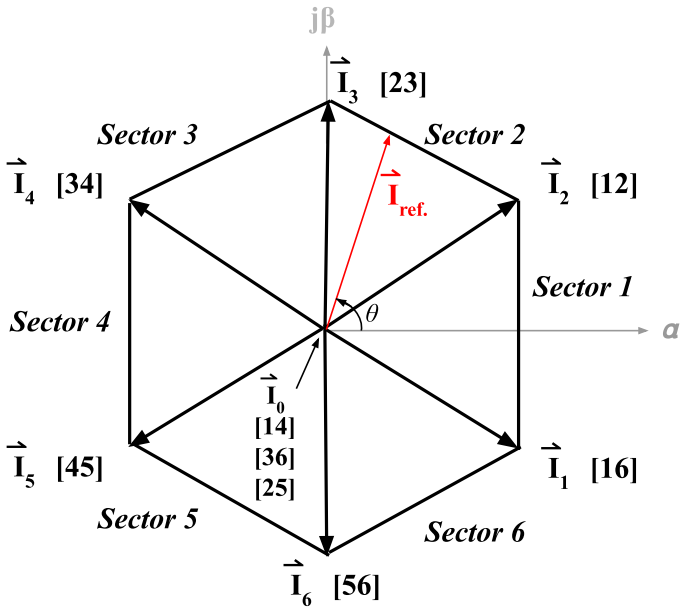


Figure 2.8: Visualization of space vector modulation for CSIs.

$$T_1 = m_a sin(\frac{\pi}{6} - \theta^{'})T_s \tag{7}$$

$$T_2 = m_a sin(\frac{\pi}{6} + \theta^{'})T_s \tag{8}$$

$$T_0 = T_s - T_1 - T_2 \tag{9}$$

$$\theta^{'} = \theta - (k-1)\frac{\pi}{3} \tag{10}$$

Another design aspect to consider for SVM is the vector switching pattern. Typically, the sequence is selected to minimize the switching frequency and minimize switching losses [5]. However, the vector pattern also affects the harmonic performance, DC-link current ripple, and as a result, the filter and DC-link inductor size [47], [48], [49], [50], [51]. [47] and [51] present six sequences. Sequence one (SQ1) SVM

uses two active vectors that supply I_{dc} and $-I_{dc}$ respectively, followed by a zero vector [5], [47], [51]. The specific vectors are selected based on the current sector location of the reference vector. This is shown in Fig. 2.9. The sampling to switching frequency ratio is 2:1 [47]. To understand the relationship between the switching frequency, f_{sw}, and sampling frequency, f_s, the following thought process can be followed. If the switching sequence is considered with one sampling period per sector, each switch will conduct three times per cycle of the fundamental (60 Hz). As a result, the switching frequency is 3×60=180Hz. Since there is one sampling period per sector, the sampling frequency will be $1 \times 6 \times 60$=360 Hz. If the amount of sampling periods per sector is increased to two (the sampling frequency is $2 \times 6 \times 60$=720 Hz), each switch will conduct six times per 60 Hz cycle. This makes the switching frequency 6×60=360 Hz. Continuing this thought process to the required switching frequency yields the required sampling frequency. Fig. 2.10 shows how SVM is implemented on a processor (using the NS assumption), with the f_{sw} set to 540 Hz and f_s set to 1080 Hz. Half of the fundamental period is shown. A counter is used and represents each sampling period [48], [51]. It counts to a value equal to T_S. The dwell times T_1 and $T_1 + T_2$ are used as "modulating signals" and are compared with the counter to generate the corresponding gating signals. It should be noted the time duration of $\vec{I}_n$, $\vec{I}_{n+1}$, and $\vec{I}_0$ are equal to T_1, T_2, and T_0 respectively.

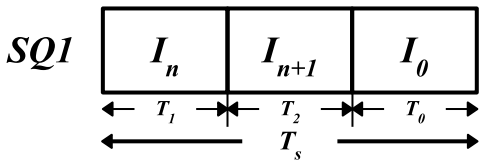


Figure 2.9: Vector Sequence for SQ1 SVM.

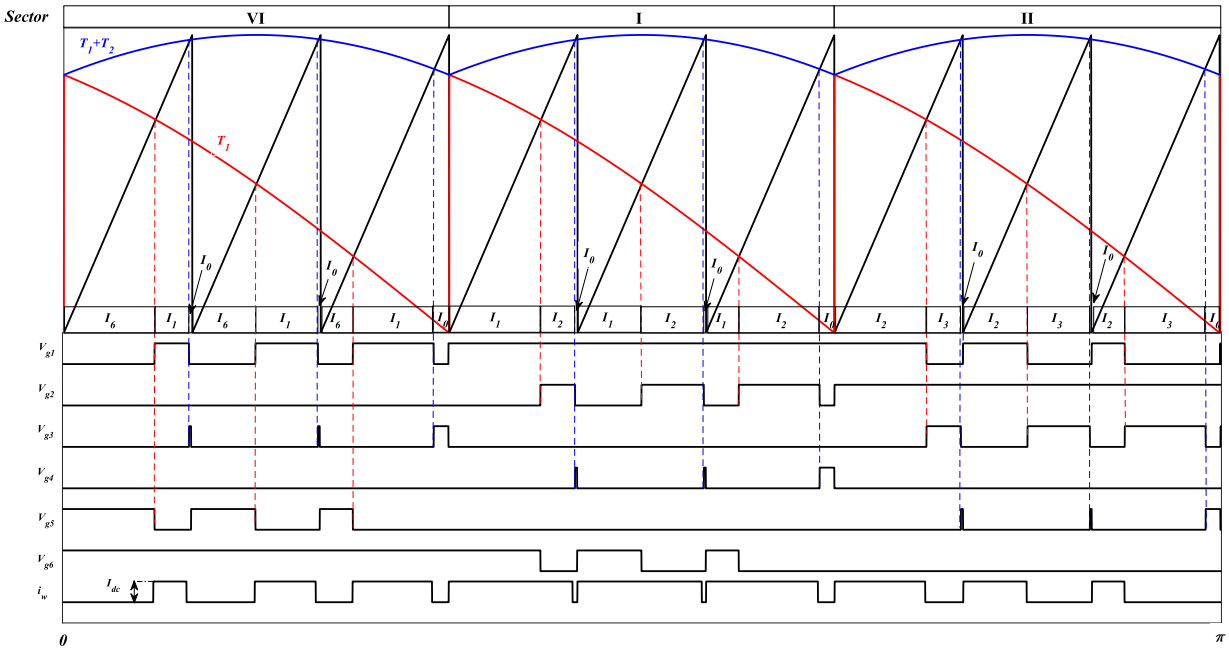


Figure 2.10: SQ1 SVM ($m_a = 1$, $f_{sw} = 540$ Hz, $f_s = 1080$ Hz).

Sequence two (SQ2) SVM divides the zero vector in a given sampling period by two and inserts it at the beginning and end of the pattern [47]. Now, the duration of either zero vector is $T_0/2$. This is shown in Fig. 2.11. The switching and sampling frequency relationship remains the same as that of SQ1 SVM [47]. Again, a sawtooth carrier/counter is used [47], [51]. However, the dwell times used to carry out the comparison action are $T_0/2$, $T_1 + T_0/2$, and $T_1 + T_2 + T_0/2$. To minimize switching frequency, the zero vector at the end of a sampling period is the same as the starting zero vector of the next sampling period within the same sector [51]. Also, when transitioning between sectors, the last zero vector is the first zero vector of the future sector [51]. A half period of the fundamental is shown in Fig. 2.12.

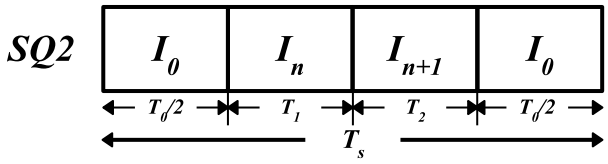


Figure 2.11: Vector Sequence for SQ2 SVM.

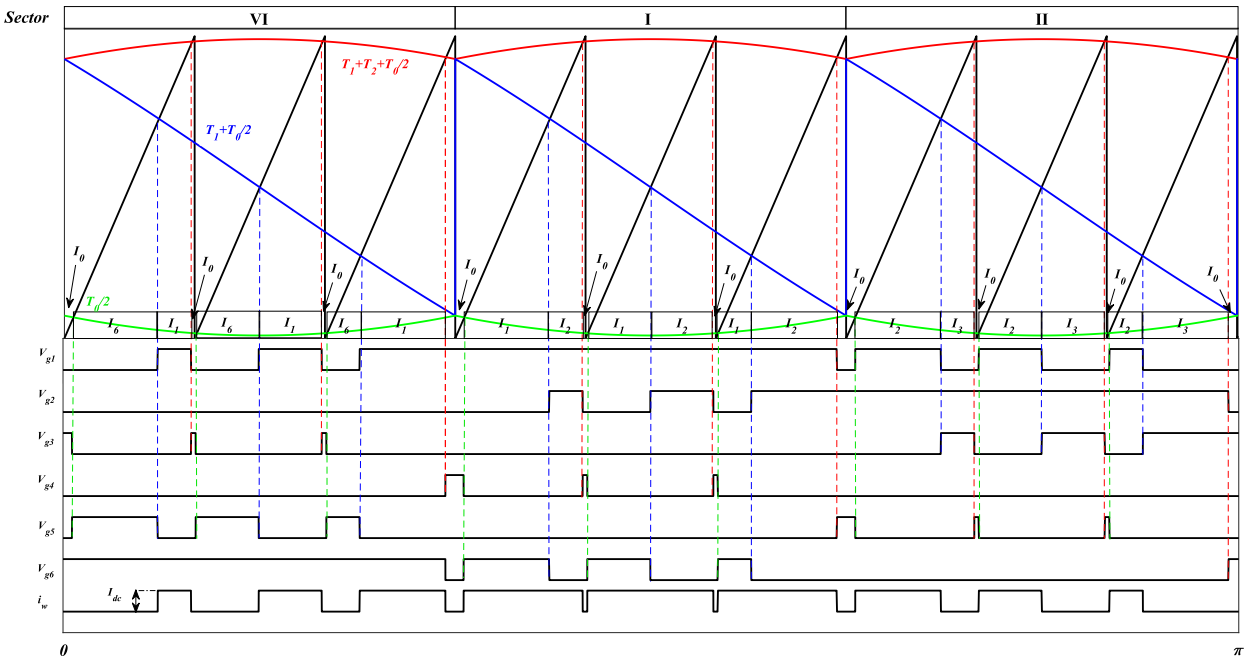


Figure 2.12: SQ2 SVM ($m_a = 1$, $f_{sw} = 540$ Hz, $f_s = 1080$ Hz).

Sequence three (SQ3) inserts the zero vector between the two active vectors of SQ1 SVM [47]. This along with the time durations are shown in Fig. 2.13. Naturally, the last active vector of any given sector is equal to the first active vector of the following sector [51]. This reduces the switching frequency. As shown in Fig. 2.14, when using a sampling frequency of 1080 Hz, the equivalent switching frequency is 480 Hz [47], [51]. To implement this sequence, a sawtooth carrier is used once again and the dwell time vectors include T_1 and $T_1 + T_0$ [47], [51].

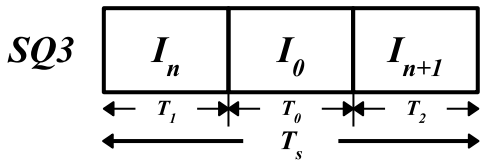


Figure 2.13: Vector Sequence for SQ3 SVM.

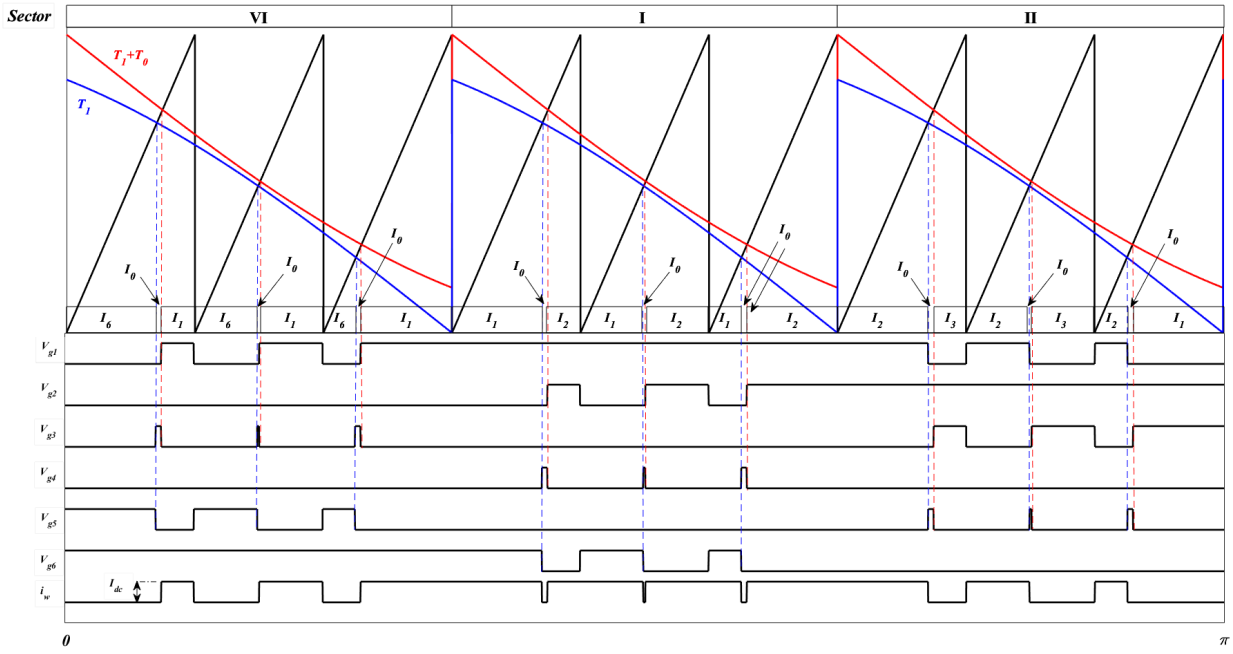


Figure 2.14: SQ3 SVM ($m_a = 1$, $f_{sw} = 480Hz$, $f_s = 1080Hz$).

Sequence four (SQ4), similar to SQ2 splits the zero vector and puts it on either end of the pattern during a given sampling period. However, in order to maintain symmetry in i_w, the pattern is reversed for alternating sampling periods [51]. In order to implement this, a triangular carrier is utilized. The dwell time vectors utilized include $T_1 + T_2 + T_0/2$, $T_1 + T_0/2$, during even sectors $T_1 + T_0/2$, and during odd-numbered sectors $T_2 + T_0/2$ [47]. To minimize the switching loss the last zero vector of a sector is set to be the first zero vector of the following sector [51]. As a result, the sampling to switching frequency ratio is 2:1 just like SQ1 and SQ2 [47], [51]. Sequence five (SQ5) SVM puts the zero vector first followed by the two active vectors that are interchangeable [47], [51]. Similar to SQ4, an asymmetric pattern is used, meaning, the pattern is reversed in subsequent sampling periods (see Fig. 2.17) [51]. This is to keep waveform symmetry. To achieve this, a triangular carrier is used and a sampling frequency of 1440 Hz is used for a switching frequency of 480 Hz [47], [51]. The dwell time vectors used include $T_2 + T_0$ and T_0. Of course, to limit the switching frequency, the zero vector to end a sector is equal to the first zero vector of the next sector. The principle of SQ5 SVM gating signal generation is shown in Fig. 2.17 and Fig. 2.18.

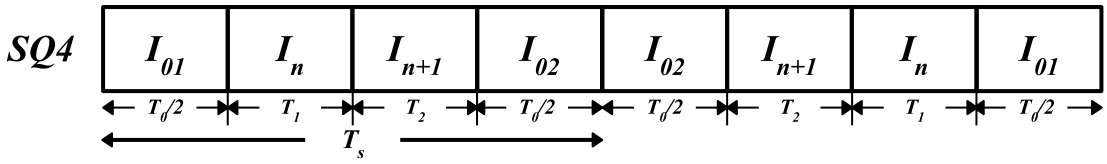


Figure 2.15: Vector Sequence for SQ4 SVM.

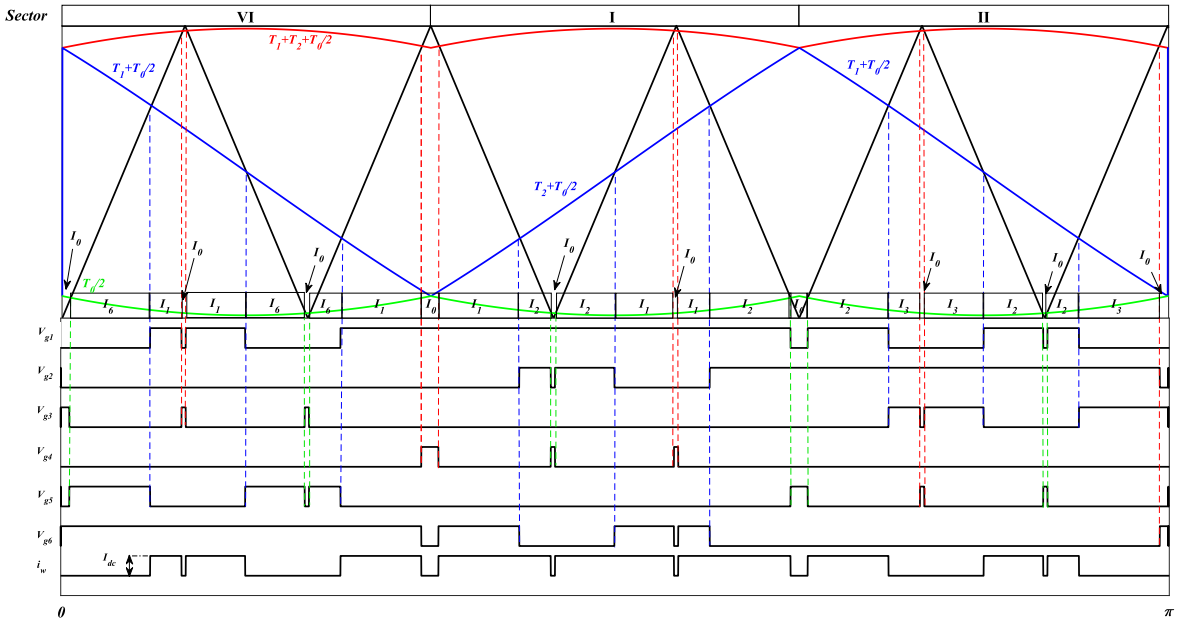


Figure 2.16: SQ4 SVM ($m_a = 1$, $f_{sw} = 540$ Hz, $f_s = 1080$ Hz).

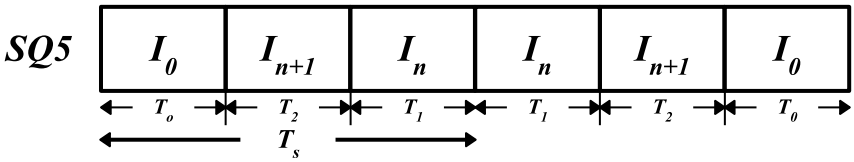


Figure 2.17: Vector Sequence for SQ5 SVM.

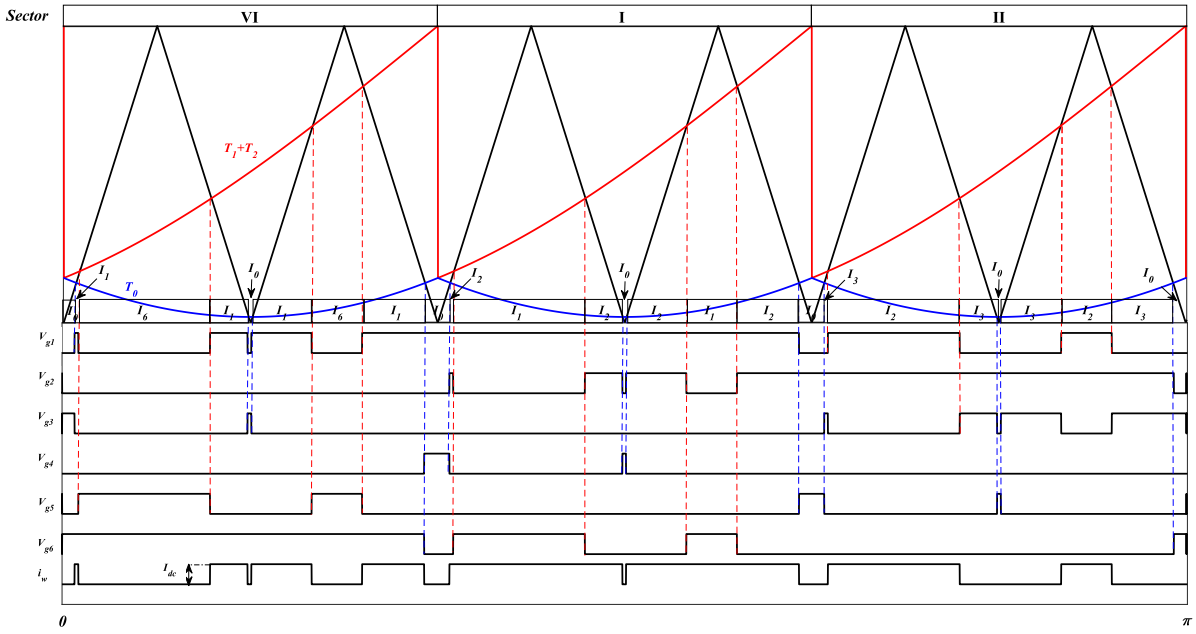


Figure 2.18: SQ5 SVM ($m_a = 1$, $f_{sw} = 480$ Hz, $f_s = 1440$ Hz).

Sequence six (SQ6) SVM is a non-symmetrical pattern that consists of two active vectors followed by a zero vector in the first sampling period [47]. The following sampling period begins with a zero vector and is followed by two active vectors in the same order as the first sampling period. Again, a triangular carrier is used. The modulating signals include $T_1 + T_2$, T_1, and T_2 [47]. The switching frequency is minimized due to the fact that a sector will end on the first active vector of the proceeding sector [51]. Similar to SQ4, a sampling frequency of 1440 Hz needs to be used to maintain symmetry in the PWM current [47], [51]. However, in this case, the equivalent switching frequency is 540 Hz.

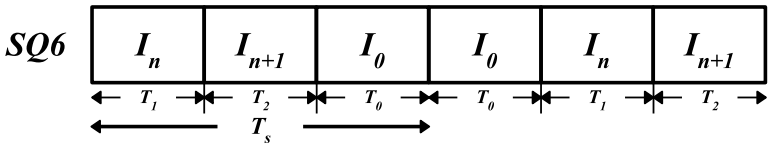


Figure 2.19: Vector Sequence for SQ6 SVM.

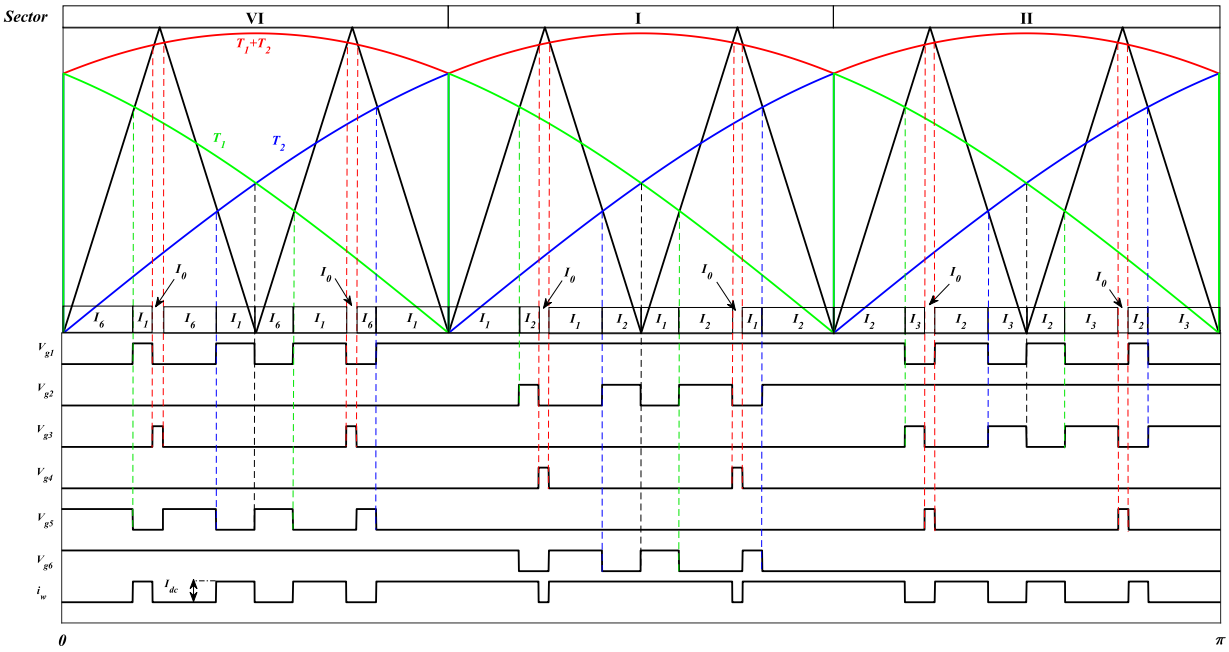


Figure 2.20: SQ6 SVM ($m_a = 1$, $f_{sw} = 540$ Hz, $f_s = 1440$ Hz).

It is worth noting that the equivalent switching frequency of the converter can be computed using (11) for any modulation scheme [5]. Where N_p is the number of pulses in one fundamental period and f_{fund} is the fundamental frequency of the converter (60 Hz).

$$f_{sw} = f_{fund} \times N_p \tag{11}$$

2.3.2 Trapezoidal Pulse Width Modulation

Conventional PWM used in VSIs cannot be used in CSIs because it violates the two mentioned

switching state restrictions. As a result, TPWM was developed [5]. This modulation scheme uses a discontinuous triangular carrier (v_c) and trapezoidal modulating signal (v_m). From $\pi/3$ to $2\pi/3$, no change in the gating signals occur to avoid invalid switching states [5]. These facts are illustrated in Fig. 2.21. As a result, of the discontinuous carrier and flat portion v_m, there is no bypass operation and the magnitude of the PWM currents fundamental harmonic can only be adjusted within a limited range [5]. Specifically, from 0.85 to 1 of the rated fundamental when m_a is varied across its entire range [5]. For TPWM, m_a is defined by (12)

$$m_a = \frac{v_m}{v_{cr}} \tag{12}$$

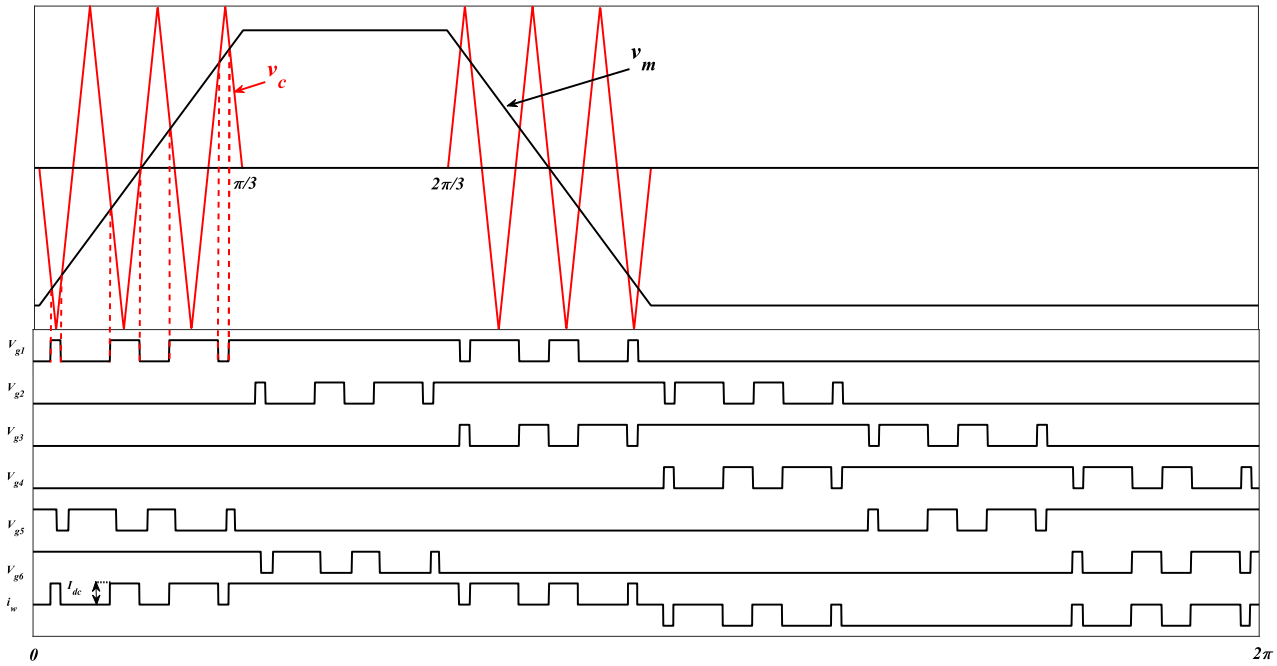


Figure 2.21: TPWM ($m_a = 0.85$, $N_p = 7$, $f_{sw} = 420$ Hz).

2.3.3 Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a modulation scheme where the switching angles are pre-calculated to eliminate low-order, high magnitude harmonics in low frequency applications [5]. These angles are pre-loaded onto the processor and therefore, SHE is considered an off-line modulation scheme [5]. The switching angles are derived based on the Fourier series of the desired PWM current waveform [5], [52]. The analysis simplifies further due to the fact that the PWM current is kept to have half-wave or quarter-wave symmetry, eliminating even order harmonics [52]. The number of equations to be solved is given by (13). This equation also implies the number of independent switching angles. For the case of $Np = 5$, there are three independent angles. The number of independent angles determines the number

of harmonics that can be eliminated [5], [52]. The PWM current waveform for the case of $Np = 5$ is shown in Fig. 2.22. The expressions in (14) can be written and the angles can be solved using non-linear methods such as the Newton-Raphson method [5]. The resulting angles when solving (14) for θ_1, θ_2, and θ_3 are 2.25°, 5.6°, and 21.26° respectively [5]. This enables the elimination of the 5^{th}, 7^{th}, and 11^{th} harmonics but (14) can be tailored to eliminate any three desired harmonics.

$$N_p = 2k + 1 \tag{13}$$

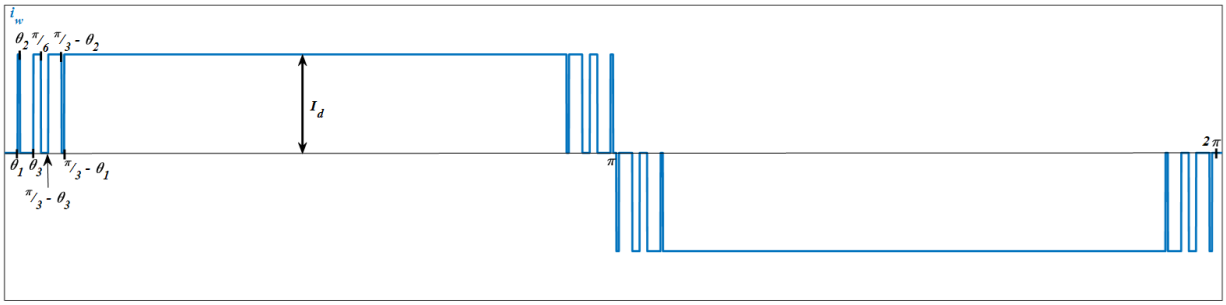


Figure 2.22: PWM current generated by SHE with N_p=7.

$$\begin{cases} F_1 = \cos(5\theta_1) + \cos(5(\pi/3 - \theta_1)) - \cos(5\theta_2) - \cos(5(\pi/3 - \theta_2)) + \cos(5\theta_3) \\ \qquad + \cos(5(\pi/3 - \theta_3)) - \cos(5\pi/6) = 0 \\ F_2 = \cos(7\theta_1) + \cos(7(\pi/3 - \theta_1)) - \cos(7\theta_2) - \cos(7(\pi/3 - \theta_2)) + \cos(7\theta_3) \\ \qquad + \cos(7(\pi/3 - \theta_3)) - \cos(7\pi/6) = 0 \\ F_3 = \cos(11\theta_1) + \cos(11(\pi/3 - \theta_1)) - \cos(11\theta_2) - \cos(11(\pi/3 - \theta_2)) \\ \qquad + \cos(11\theta_3) + \cos(11(\pi/3 - \theta_3)) - \cos(11\pi/6) = 0. \end{cases} \tag{14}$$

Similarly, by increasing the number of pulses in the PWM current, the amount of independent switching angles increase, and therefore, an additional harmonic can be eliminated. This is done by increasing the switching frequency of the inverter [52], [53]. However, as a result, the amount of equations to be solved are increased. To regulate the output current, SHE can be configured with amplitude modulation index control [5]. To implement this, a Fourier expression for the fundamental component is used and one less harmonic component can be eliminated [5]. Since SHE is not a main focus of this report, the procedure is not repeated here as it is covered in depth in [5], [52], and [53]. The main takeaway from this section should be the fact that the amount of equations to be solved grows proportionally to the number of pulses in the PWM current and, in turn, the switching frequency of the converter.

2.3.4 Principle of Shifted Gating Signals

As previously discussed, the CSI requires semiconductors that can achieve RB. The anti-series switch configurations shown in Fig. 2.3 (d)-(f) and shown in Fig. 2.23, require a special gating signal consideration in order to have RB operation. The solution is to delay the lower switch gating signal by a time value such that the lower switch is off for at least the duration of the transient period. This is known as the principle of shifted gating signals [40], [54]. The operation principle is summarized in Fig. 2.24, where t_d is the delay time selected by the designer. In the first quadrant, the upper and lower switch are off, no current travels through the switch, and the lower device behaves as a diode. In the second quadrant, the upper switch turns on but due to the delay, the lower switch remains off and continues diode operation. In the third part, the lower switch turns on and the device is said to be in steady state. Current conducts, through the upper switch forward channel and lower switch 3rd quadrant channel. In the final quadrant, the upper switch is turned off but the lower switch remains on for a few more nanoseconds. This is when another switch will turn on (i.e. the CSI is changing switching states), so it will rely on the other switch turning on to provide RB to avoid inter-phase shorts. For better understanding, Fig. 2.25 is provided and shows the operation principle of the dual switch CSI when transitioning switching states.

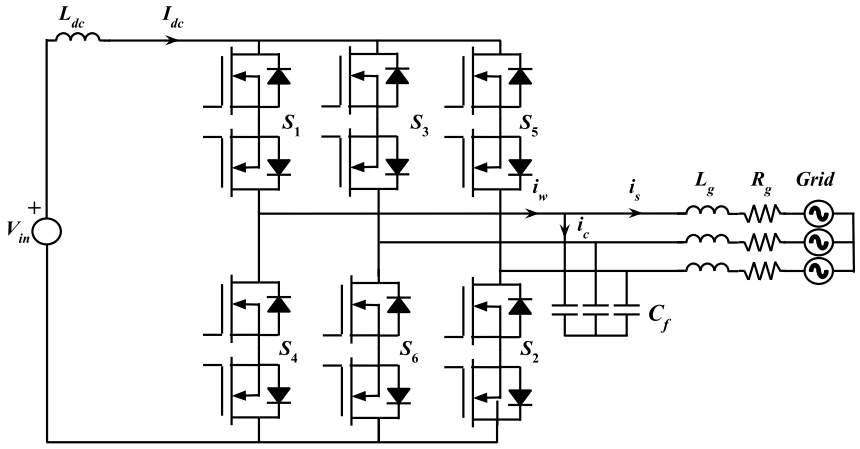


Figure 2.23: CSI with anti-series MOSFETs.

2.3.5 Modulation Scheme Selection for High Frequency Applications

At this time, it should be noted that SVM (SVM with shifted gating signals for the required switching cells) is the selected modulation to be used in this report given that high switching frequency will need to be obtained. First, SVM offers more simple scalability with switching frequency. On the contrary, SHE requires the engineer to solve an amount of equations proportional to the number of pulses

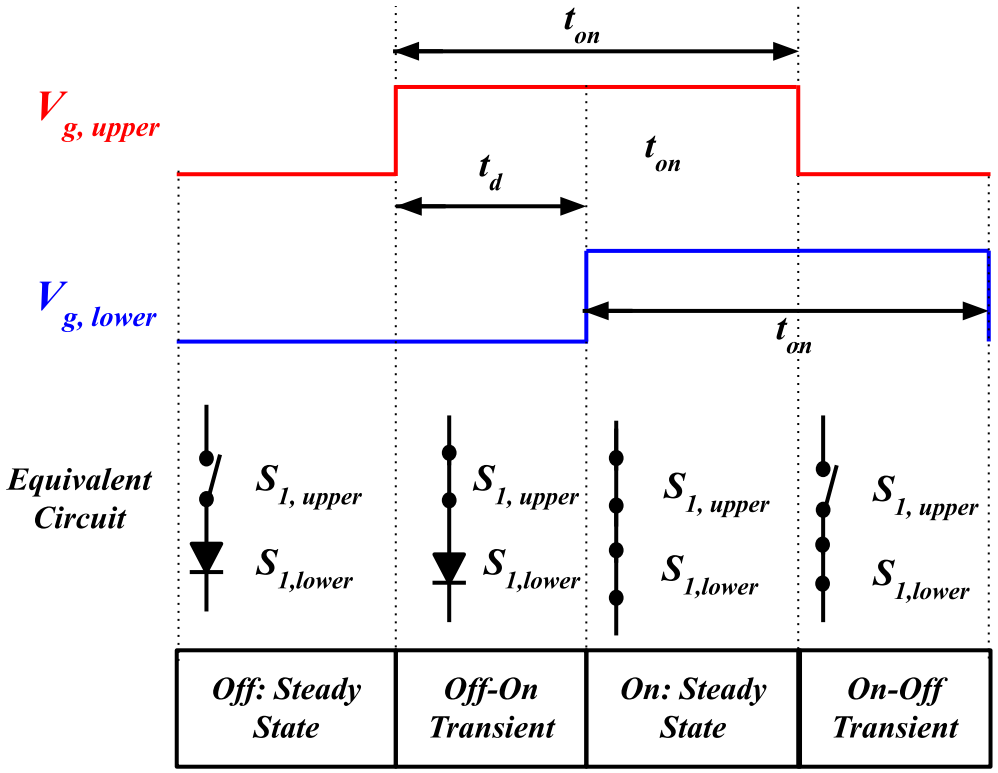
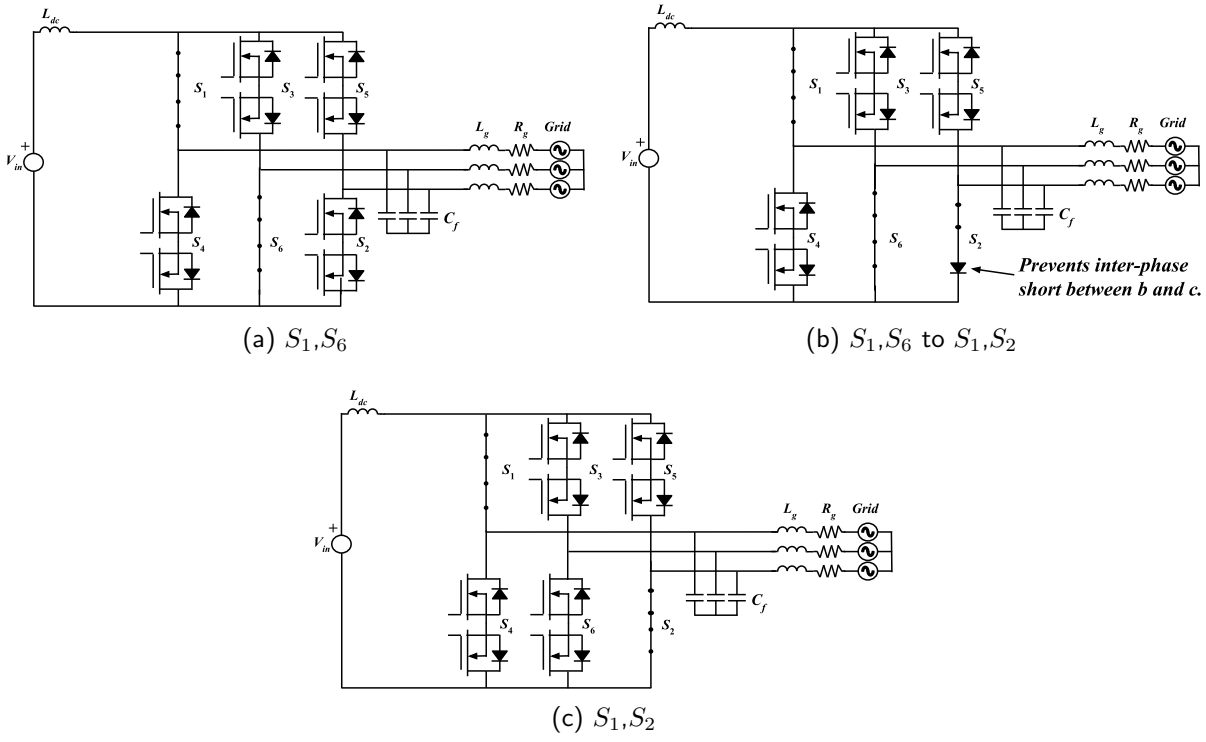


Figure 2.24: Principle of shifted gating signals to achieve reverse blocking.



(a) S_1,S_6

(b) S_1,S_6 to S_1,S_2

(c) S_1,S_2

Figure 2.25: Dual switch CSI transition from S_1, S_6 to S_1, S_2.

in the PWM current [5]. Meaning, even at 10s of kHz, approximately 30 equations need to be solved. The practicality in the implementation of this is low. Also, the purpose of SHE is to eliminate low order harmonics. This is naturally obtained with increasing the switching frequency. Next, SVM offers more controllability over the output current. The modulation index can be adjusted dynamically and the output current is controlled by the bypass operation states [5]. The bypass states also offer natural decoupling between the PV and grid, which is advantageous in solar inverters [4]. On the contrary, TPWM provides no bypass operation states and therefore, less control over the output current [5]. Also, the harmonic content of the PWM current produced by TPWM performs worse than that of SVM at unity modulating index [5]. Therefore, in order to minimize the PWM currents' THD when using TPWM, a modulation index of 0.85 is used [5]. This is undesirable for solar applications as an m_a value of one is usually used all through operation in order to draw maximum power from the PV array [4], [55]. Also, in the configuration studied, there is no rectifier stage or stage prior to the CSI to control the DC-link current as recommended when using TPWM [5].

2.4 Research Trends for CSIs in PV Systems + Comparison with VSI

It is important to keep in mind that in the power electronics industry, the main goals for advancement will always be increasing the power conversion efficiency, power density, and reliability, while decreasing the physical size/weight, cost, complexity, and meeting grid codes [13], [20], [56]. This point is reinforced further when observing the trends in the design goals with each advancement in the solar inverter topology covered in section 1.2. To reiterate, they include the removal of the LF grid-interfacing XFMR, suppression of LC and CMV, efficiency improvements with evenly distributed losses, delivered power quality improvement, decreased filtering requirements, limiting component count, reducing voltage stress across the semiconductors, and reducing the amount of power conversions in the system.

Another important point covered in section 1.2, is that the solar inverter market is currently dominated by VSI-based solutions [4], [6], [7], [8], [10]. There are a few additional factors that influence this. One is that VSI-based configurations are well-researched and established while also being naturally compatible with commercialized semiconductors (reverse conduction is required and achievable through the body diode of most commercialized devices) [57]. The other is that the CSI usually requires a large, bulky, and costly DC-link inductor while having a large amount of conduction loss due to the series-connected diodes [56], [57], [58]. However, the remainder of this section discusses some advantages and trends seen in the CSI for solar applications with some comparisons to the VSI.

When comparing the VSI to the CSI in grid-tied PV string inverter applications, it is important

to consider that the VSI requires a boost converter for proper operation and MPPT [56], [57], [59]. On the other hand, the CSI has natural boosting capabilities and in turn, does not require a boost converter stage [9], [56], [57], [59]. As a result, in this configuration, the CSI can naturally eliminate one lossy power conversion stage. In terms of output filtering, the CSI provides less THD than the VSI and dv/dt [57], [60]. This is due to the fact that the CL filter has higher damping capability than VSI filters but the CSI introduces resonance as a design challenge [60]. Since the DC-link ripple is controlled by the DC-link inductor, not a DC-link capacitor, the reliability of the CSI is higher [9], [57]. This is because 60-70% of VSI failures can be accounted for by the DC-link capacitor [9]. The DC-link inductor also creates higher power density for CSIs, typically 2 times the value of equivalent power rating VSIs [56].

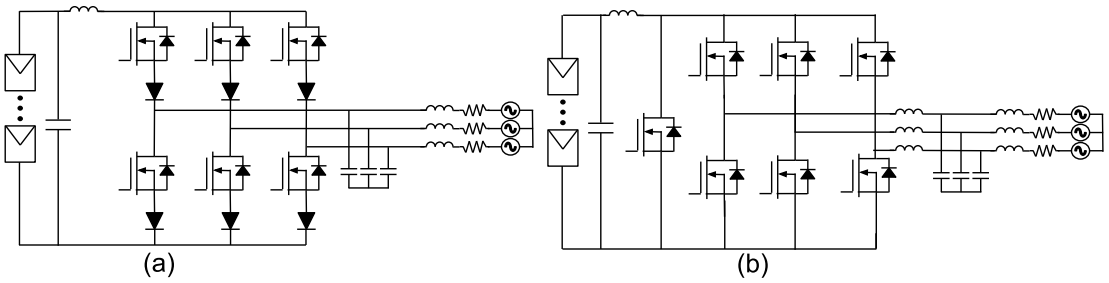


Figure 2.26: Solar inverters: (a) CSI, (b) 2L-VSI + boost converter stage.

Moving on, the standard DIN VDE 0126 provides limitations to the amount of LC that can be injected into the grid [8], [9]. The conventional CSI does not meet this standard naturally [9]. Solutions that work toward the elimination of the LF XFMR, LC, and CMV of the grid-tied CSI are discussed in detail in [9], [59], [61], and [62]. In [59], an optimal zero vector selection scheme is used to minimize the CMV at the expense of higher switching losses. In [9] and [61], a new CSI topology is proposed known as the four-leg CSI. It introduces an additional two switches across the DC bus, a common mode inductor (DC-link inductor value divided in two), and split PV capacitors [9], [61]. The results show a CSI configuration that can connect to the grid without an LF XFMR while still meeting the LC requirements. Also, the total conduction and switching losses are the same as that of a conventional CSI, just distributed over more switches [9], [61]. Similarly, [62] introduces a single switch across the DC side with a common mode inductor. This is referred to as the H7 CSI [62]. The outcome is suppressed LC such that the mentioned standards are met. However, another advantage is proven. Since the H7 switch is used to implement the zero vector, a reduction in overall conduction loss is seen [62]. Also, due to the altered modulation scheme implemented, zero current switching is achieved, and hence the switching loss in the main six switches are essentially zero [62]. Overall, LC solutions have already been exhausted in literature and have resulted in CSIs capable of complying with mentioned standards without degrading efficiency and with a lower component count than that of LC suppression solutions proposed for VSIs. Further investigation into the H7 CSI is carried out in [54] and [63]. Similar efficiency improvement results are

proven with conventional and newly developed modulation schemes for low power applications (<3kW). It is also pointed out that gating signal overlap is no longer required in this configuration. The four leg CSI and H7 CSI are shown in the figure below.

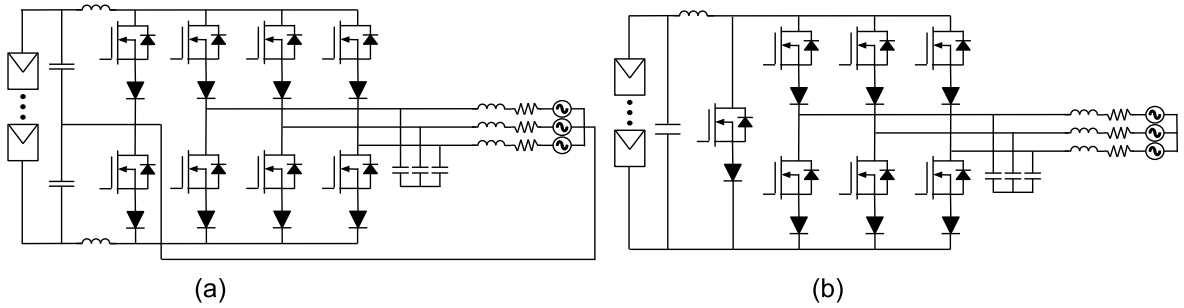


Figure 2.27: Solar inverters: (a) Four leg CSI, (b) H7 CSI.

Another method for increasing the efficiency include the H8 CSI presented [64], [65]. This configuration adds an additional switch to the H7 CSI that is in series with the DC-link inductor. The purpose of this converter is to add compatibility with BD switches to reduce conduction loss by using the 8th switch's body diode to block reverse currents [64], [65]. Note, if a diode is used, the converter becomes more lossy than the conventional H6 CSI [65]. Due to voltage clamping of the series diode, the main six switches receive zero voltage and zero current switching further reducing switching loss [65]. Of course, using parallel switches is also an option to reduce conduction losses by essentially dividing the current between multiple switches. This approach is taken in [58] and [66]. Therefore, this method is not discussed further.

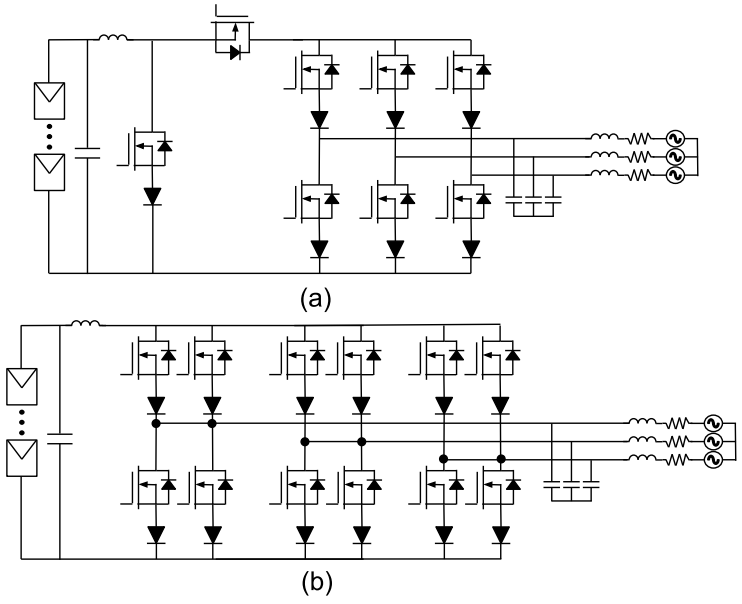


Figure 2.28: Solar inverters: (a) H8 CSI, (b) Parallel Switch CSI.

2.5 Dissertation Objectives

To summarize the prior section, VSI-based solutions dominate the current solar inverter market, however, the CSI introduces some interesting advantages making the topology a valued research area. These advantages include inherent short circuit protection, natural voltage boosting capabilities, increased reliability, lower switching losses (natural higher switching frequency capability), simple structure, and increased power density [5], [9], [56], [57], [59]. As discussed in the prior section, the CSI has seen a lot of research efforts in recent times. First, LC and CMV issues in CSI have already been resolved. Many successful attempts to improve efficiency have been seen with the creation of the H7, H8, and parallel switch CSI. However, these converters have an increase in component count and require more complex modulation schemes. As mentioned, it is speculated that WBG devices will push power converters to the "next generation" [4], [8], [10]. Although, the magnitude of WBG device advantages will depend on the ability of commercially available devices to harness the benefits of WBG material, as well as the converter configuration. With the roll-out of commercially available WBG devices, their advantages discussed in section 1.3 should be able to naturally improve the base CSI's efficiency through a reduction in RB switch conduction and switching losses as well as the DC-link inductor size, cost, and loss technical challenge. Therefore, this thesis analyzes and compares the efficiency of numerous switching cells presented in [35] and shown in Fig. 2.29 (a)-(f) using Powersim (PSIM) thermal module simulations. This provides context to the theoretical efficiency limits of the base CSI with enhanced next generation switches. The application selected is a 10 kW string inverter. This was selected due to the fact that string inverters are used in low to medium power applications, this is the region where WBG devices will be most useful. This is because high current rating WBG devices are not yet commercially available and having high frequency operation in 100 kW applications is yet to be seen. On top of that, string inverters provide flexibility in solar farms and can be utilized in most configurations to some extents, as discussed in Chapter 1.2. Three concurrent investigations are carried out throughout the report and shown in the flow charts in Fig. 2.30. First, the switching frequency is varied while keeping the modulation scheme, operating power, and temperature constant. At the end of this investigation, temperature if varied at a constant switching frequency value to comment on efficiency variation with temperature. The second investigation involves varying the CSI's operating power with fixed modulation scheme, switching frequency, and temperature. The inverter efficiency is characterized and compared to existing commercialized solutions. Finally, the effect of varying the modulation scheme on the CSI efficiency is characterized. Here, only case C is considered as the trends will remain constant for all switch configurations. Lastly, some insights on the cost of the CSI using each switch configuration are provided. The following paragraphs summarize the contents of the chapters.

Chapter 3 discusses the CSI's base ratings, semiconductor device rating selections, and sources of

loss that are considered in the CSI model. Fundamental loss calculations are reviewed for each device and an analytical switching loss model is proposed. Extra effort is put into sizing the DC-link inductor and filter components in accordance with IEEE 519-2014 in order to get accurate corresponding losses. Manufacturer data is relied upon to get passive component losses and theoretical calculations are provided to prove validity. The effect of varying the switching frequency and SVM sequence on passive components is studied. Filter performance indicators are reviewed and used to develop a filter loss optimization method.

Chapter 4 provides the PSIM thermal model simulation results for various conditions. First SQ1 SVM is used and the switching frequency is varied from 1 kHz to 100 kHz. The semiconductor performance is compared and contrasted by means of figures and characterizing parameters such as semiconductor efficiency and loss slope. The total loss (semiconductor + passive component loss) is compared at each frequency and an optimum switching frequency range for each switching cell configuration is proposed. Simulation results are compared to the results of the calculation methods purposed in Chapter 3. The effect of varying the SVM sequence on the efficiency of the CSI is studied. This study includes the passive component loss results collected in Chapter 3. The remaining sections provide further results for possible conditions encountered by the CSI in typical grid-tied operation. This includes varying power conditions, modulating index values, and temperatures.

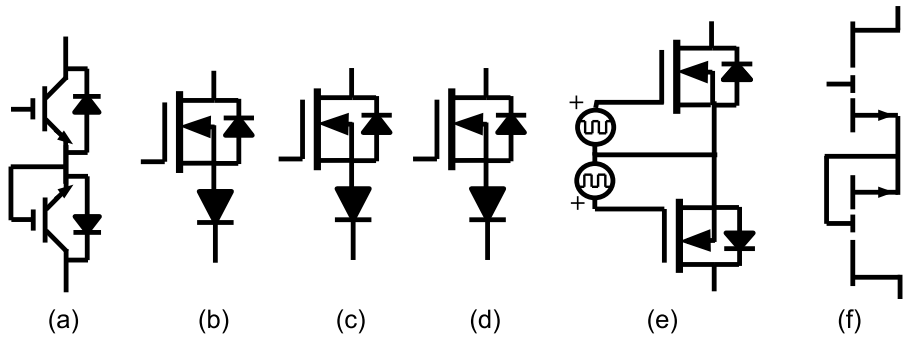


Figure 2.29: Various semiconductor solutions with reverse blocking capabilities: a) Case A – IGBT switch in series with IGBT body diode, b) Case B – Si MOSFET in series with discrete Si diode, c) Case C – SiC MOSFET in series with Si diode, d) Case D – SiC MOSFET in series with SiC Schottky Barrier Diode (SBD), e) Case E – Dual SiC switch (common source), and f) Case F – Anti-series GaN solution.

2.6 Summary

Section 2.1 Introduction to CSI Components

- Components of the CSI and their roles were discussed, including the DC-link inductor (L_{dc}), filter capacitor (C_f), etc.

Section 2.2 Review of Reverse Blocking Semiconductors

- Semiconductors compatible with the CSI were introduced and were developments are discussed.

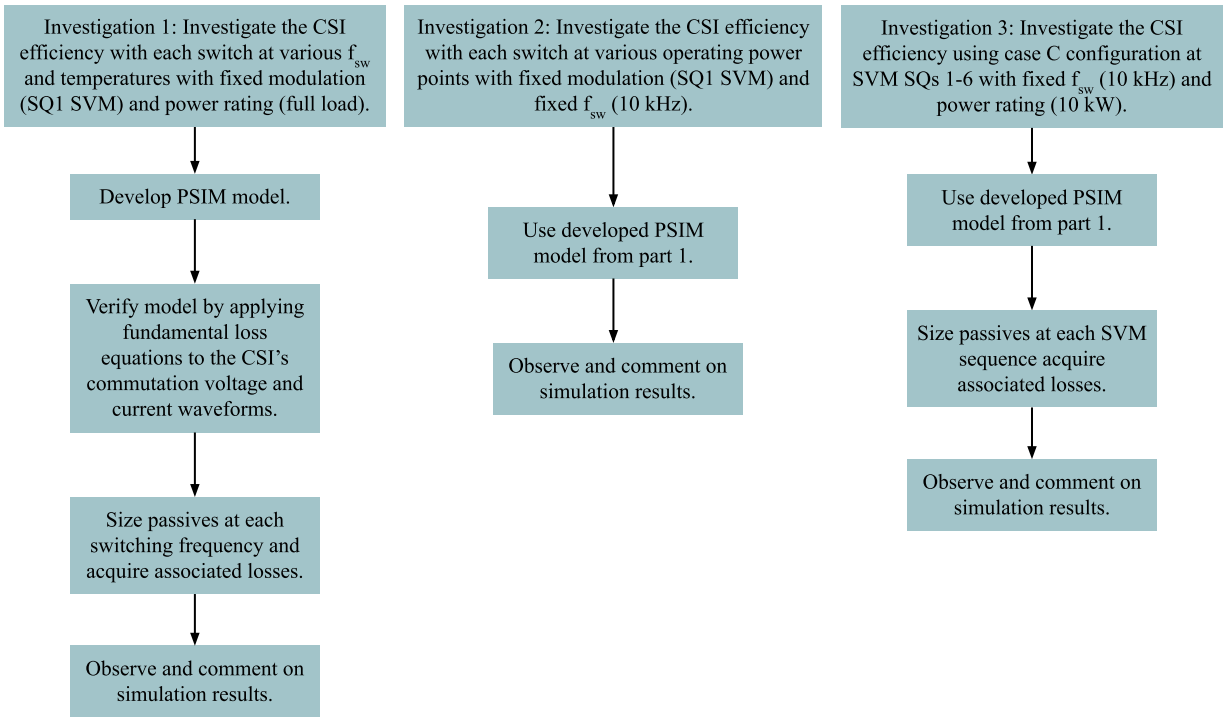


Figure 2.30: Flow charts of the three investigations carried out in this report.

- Defined reverse blocking, bidirectional, and monolithic switches and examples are provided.

Section 2.3 Modulation Schemes

- The theory behind the three primary modulation schemes used for the CSI were discussed. They include SHE, TPWM, and SVM.
- Each SVM sequence (SQ1-6) was explained in more detail as they will be used throughout the report.
- The principle of shifted gating signals to achieve RB in CSIs is discussed and will applied later in the report.
- The reasons for selecting SVM were highlighted and include: better scalability with increasing frequency than SHE, and more control-ability of the output current than TPWM.

Section 2.4 Research Trends for CSIs in PV Systems + Comparison with VSI

- Discussed research trends in solar inverters derived from Chapter 1.2.
- Mentioned that VSI dominates the solar inverter market due to the fact that it is a well-established technology with natural compatibility with commercially available semiconductors.
- Discussed the advantages of CSI over VSI and other research conducted in literature for CSIs in PV systems.

3 CSI Design, Ratings, & Sources of Loss

The purpose of this section is to discuss the losses considered in the developed PSIM simulation model. That is, the DC-link inductor, semiconductors, and filter components. The sizing methodology for each component is discussed. Properly sizing these components is crucial to the loss distribution. Further, loss values for the DC-link inductor are presented and verified with fundamental calculations. Basic, semiconductor loss equations are reviewed and an analytical method for estimating the switching loss is proposed. Finally, the filter capacitor and inductor are sized and a loss minimization process is discussed. The rating of the CSI is provided so per unit (pu) values have numeric meaning as well.

3.1 CSI Rating + Sources of Loss

Table 7 shows the considered CSI parameters. Note that these are based on typical 3-phase solar inverter products [4] - [10]. A 10 kW CSI tied to a 208 V_{LL}, 60 Hz grid is considered. Using the power conversion principle [5], the nominal DC-link voltage is 255 V while the input current is 39.22 A. The line resistance and inductance on the grid side are set to typical values, 0.01 pu and 0.1 pu respectively [67]. Fig. 3.1 shows the losses considered. They include the DC-link and filter inductors': winding, core, and AC losses. The output filter capacitor's equivalent series resistance (ESR) loss is considered. The semiconductor losses considered are the conduction and switching losses for the upper switch and the conduction and reverse recovery loss/switching loss for the RB device.

Table 7: CSI Ratings.

CSI Ratings	
Parameter	***Nominal Value***
Rated Power	10 kW
Grid Parameters	208 $V_{LL,rms}$, 60 Hz
Input Parameters (V_{in}, I_{dc})	255 V, 39.22 A
Output Phase Current	27.73 A
Line Resistance / Inductance	0.432 Ω / 1.14 mH

3.2 Semiconductors

3.2.1 Semiconductor Ratings

The voltage and current across and through the switching devices in the CSI configuration can be determined through simple analysis. For any active or zero switching states, the maximum voltage across the "off" switches equals the corresponding line-to-line voltage as shown in Fig. 2.7. The maximum current through any switch will equal the maximum DC-link current, which will be the average value plus the ripple current. The commutation voltage and current of a given switch in the CSI topology when

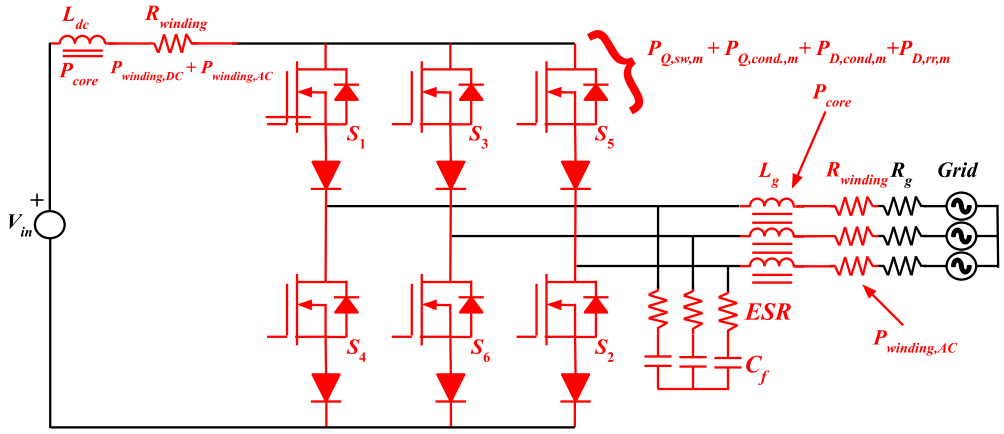


Figure 3.1: CSI Losses.

SQ1 SVM is deployed are shown in Fig. 3.2. When selecting the switch rating, a safety margin of 50% is deployed to the switch voltage and current ratings. Note that this is a standard to account for load failures, grid fluctuations, the device's safe operating area and to ensure the safety of the inverter [68], [69], [70], [71]. All of these factors are considered in (15) and (16). The selected devices are provided in Table 8.

$$V_{rated} = \sqrt{2} V_{LL,rms} \times 1.5 \tag{15}$$

$$I_{rated} = (I_{dc} + \Delta I_{dc}) \times 1.5 \tag{16}$$

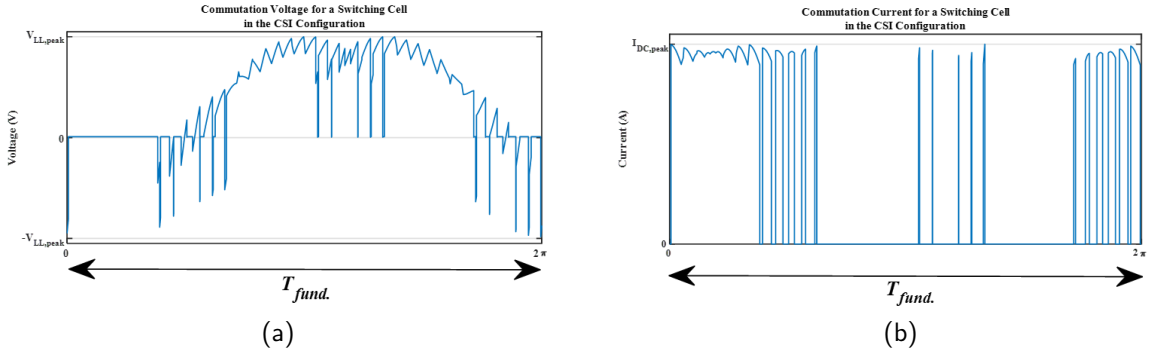


Figure 3.2: (a) Voltage across and (b) current through any given switch in the CSI configuration using SQ1 SVM ($f_{sw} = 1080$ Hz, $m_a = 1$).

Table 8: Selected semiconductor components for each configuration.

Semiconductors		
Part Type	***Manufacturer/Part Number***	***Voltage/Current Rating***
Case A: IGBT	Infineon/IKW3065ES5	650V/62A
Case B: Si MOSFET	STMictoelectronics/STY112N65M5	650V/61A
Case B & C: Si Diode	Rohm/RFS60TZ6S	650V/60A
Case C, D, E, & F: SiC MOSFET	Cree/C3M0025065K	650V/70A
Case D: SiC Schottky Diode	OnSemi/FFSH5065A	650V/60A
Case F: GaN MOSFET	GaN Systems/GS66516	650V/60A

3.2.2 Conduction Losses

The conduction loss of any MOSFET can be computed using (17). $R_{ds(on)}$ is the on-state resistance that must be scaled based on the operating drain to source current, I_{ds}, and junction temperature, T_j [68]. Similarly, the forward voltage, V_F, scaled considering the junction temperature and current through the device, is used to compute the conduction loss for the series-connected diode, body diode, and reverse conduction channel of the GaN device, as seen in (18). For the IGBT, the principle is the same, but the notation is changed in (19) to follow conventional nomenclature. For case E, since the principle of shifted gating signals is used, unique conduction loss equations must be derived since the current is passed through different mediums at different duty cycles. Since the lower switch turns on slightly after the upper, the body diode conducts during this period. Therefore, (18) can be used but the duty cycle must be refined. The body diode conducts for a duration equal to t_d and at every switching instant. As a result, multiplying t_d by f_{sw} gives the duty cycle of the lower switch's body diode. This modification is reflected in (20). For the remainder of the duty cycle, the MOSFET channel (third quadrant/reverse channel) of the lower switch will conduct. Hence, (21) can be used to compute the conduction loss of the reverse channel. Summing (20) and (21) will yield the total conduction loss of the lower C3M0025065K used in configuration E.

$$P_{Q,cond} = R_{ds(on)}(I_{ds}, T_j) \times I_{DC}^2 \times D \tag{17}$$

$$P_{D,cond} = V_F(I_D, T_j) \times I_{DC} \times D \tag{18}$$

$$P_{IGBT,cond} = V_{CE}(I_{CE}, T_j) \times I_{DC} \times D \tag{19}$$

$$P_{D,cond,lower} = V_F(I_D, T_j) \times I_{DC} \times t_d \times f_{sw} \tag{20}$$

$$P_{Q,cond,lower} = V_{F,3rdquad.}(I_D, T_j, V_{GS}) \times I_{DC} \times (D - t_d \times f_{sw}) \tag{21}$$

Of course, these equations depend heavily on the duty cycle of the device. For a CSI employing SVM, the duty cycle, D, for any of the six switches is 1/3. This is proven in the following lines, where the start of the derivation begins using the fundamental definition of the duty cycle. That is, the time that the switch is on divided by the period. Applying this to SQ1 SVM results in (22). Equation (23) defines expressions for the switch on-time duration in each sector. These equations consider S_1 operating with f_{sw}=540 Hz (3 sample periods per sector). Since S_1 remains on for the entirety of sector 1, the on-time is simply the summation of all dwell time vectors. Dwell time vectors are presented in the form of $T_{a,b}$, where a is the dwell time vector number (0-2) and b is the sample number within the sector. In sector 2, switch one is on for the duration of T_1 and, therefore, is the summation of the three T_1 occurrences. Similarly, in sectors 4 and 6, switch one is on for the duration of T_0 and T_2 respectively. This is expressed in (23) accordingly. For sectors, 3 and 5, S_1 remains off. Next, the period of the fundamental can be

written as the summation of all dwell time vectors in each sector (the total time duration of each sector). Since each sector has the same duration, (24) can be used to express the fundamental period. Finally, substituting (23) and (24) into (22) results in (25). Equation (25), proves that the duty cycle of any switch in the CSI is 1/3, independent of the m_a and f_{sw}. Since each SVM sequence works based on the same fundamental principle, this relationship remains true for all six sequences. Fig. 3.3 is provided in order to visualize the duty cycle derivation. It is worth mentioning that other modulation schemes (TPWM and SHE) also have a duty cycle equal to 1/3 [72].

$$D = \frac{t_{on}}{T_{fund.}} = \frac{t_{on,sector1} + t_{on,sector2} + t_{on,sector3} + t_{on,sector4} + t_{on,sector5} + t_{on,sector6}}{T_{fund.}} \tag{22}$$

$$\begin{cases} t_{on,sector1} = T_{1,1} + T_{2,1} + T_{0,1} + T_{1,2} + T_{2,2} + T_{0,2} + T_{1,3} + T_{2,3} + T_{0,3} \\ t_{on,sector2} = T_{1,1} + T_{1,2} + T_{1,3} \\ t_{on,sector3} = 0 \\ t_{on,sector4} = T_{0,1} + T_{0,2} + T_{0,3} \\ t_{on,sector5} = 0 \\ t_{on,sector6} = T_{2,1} + T_{2,2} + T_{2,3} \end{cases} \tag{23}$$

$$T_{fund.} = 6 \times t_{on,sector1} = 6 \times (T_{1,1} + T_{2,1} + T_{0,1} + T_{1,2} + T_{2,2} + T_{0,2} + T_{1,3} + T_{2,3} + T_{0,3}) \tag{24}$$

$$D = \frac{1}{3} \tag{25}$$

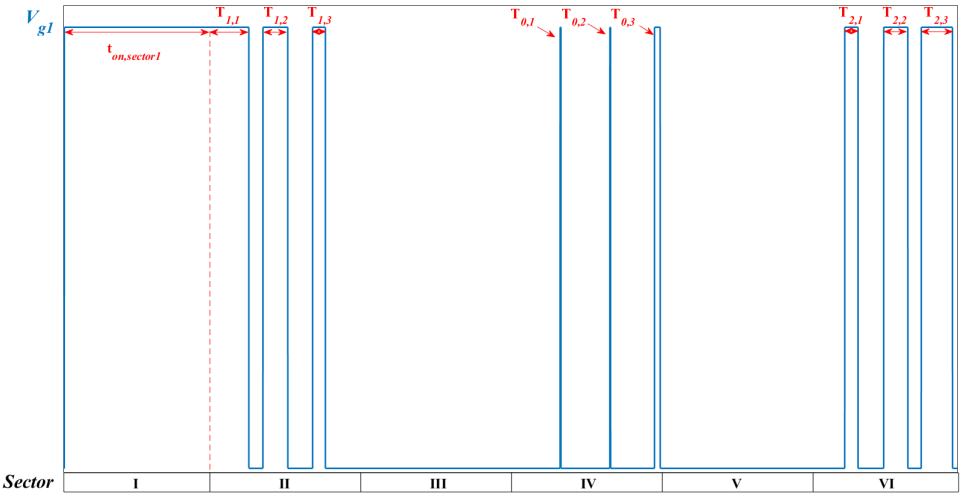


Figure 3.3: S_1 gating signal generated with labeled dwell times using SQ1 SVM ($f_{sw} = 540$ Hz, $m_a = 1$).

Continuing, now that fundamental equations have been discussed, specific functions for the conduction loss of each device studied can be derived. Again, to do this the datasheet information for each device is relied upon. First, considering the Si MOSFET (STY112N65M5), the conduction loss under full load conditions can be computed using (26). Here, the variation in the on-state resistance with temperature is modelled as a second order polynomial at a fixed current value (I_{ds} of 48 A is provided in the datasheet) and the value is scaled linearly the operating current (39.22 A). Fig. 1.9 provides more context as to why this is feasible. To be clear, it is because the device's on state resistance varies in a non-linear manner that can be represented by a second order polynomial, while the on-state resistance varies linearly with drain current. From there, the derived polynomials are substituted into (17). This process is repeated for the SiC MOSFET (C3M0025065K) and GaN HEMT resulting in (27) and (28). It should be noted that the nominal value of the the on-state resistance is defined in the datasheet and is the typical resistance at room temperature. Also, I_1 is the operating current and I_2 is the experimental datasheet value.

$$
\begin{aligned}
&P_{Q,cond,Si} = R_{ds(on)}(I_{ds} = 48A, T_j) \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(1.3584 \times 10^{-5} T_j^2 + 0.0072 T_j + 0.8067) \times \frac{R_{ds(on)}(I_1 = 39.22A)}{R_{ds(on)}(I_2 = 48A)}\right] \times R_{ds(on),nom} \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(1.3584 \times 10^{-5} T_j^2 + 0.0072 T_j + 0.8067) \times \frac{0.0011 I_1 + 0.9393}{0.0011 I_2 + 0.9393}\right] \times 0.022 \times (39.22)^2 \times \frac{1}{3} \\
&= (1.3584 \times 10^{-5} T_j^2 + 0.0072 T_j + 0.8067) \times 0.991 \times 0.022 \times (39.22)^2 \times \frac{1}{3}
\end{aligned}
\tag{26}
$$

$$
\begin{aligned}
&P_{Q,cond,SiC} = R_{ds(on)}(I_{ds} = 33.5A, T_j) \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(2.0354 \times 10^{-5} T_j^2 - 0.0019 T_j + 0.8067) \times \frac{R_{ds(on)}(I_1 = 39.22A)}{R_{ds(on)}(I_2 = 33.5A)}\right] \times R_{ds(on),nom} \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(2.0354 \times 10^{-5} T_j^2 - 0.0019 T_j + 0.8067) \times \frac{0.0013 I_1 + 0.9547}{0.0013 I_2 + 0.9547}\right] \times 0.025 \times (39.22)^2 \times \frac{1}{3} \\
&= (2.0354 \times 10^{-5} T_j^2 - 0.0019 T_j + 0.8067) \times 1.0075 \times 0.025 \times (39.22)^2 \times \frac{1}{3}
\end{aligned}
\tag{27}
$$

$$
\begin{aligned}
&P_{Q,cond,GaN} = R_{ds(on)}(I_{ds} = 18A, T_j) \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(2.6254 \times 10^{-5} T_j^2 - 0.0079 T_j + 0.7647) \times \frac{R_{ds(on)}(I_1 = 39.22A)}{R_{ds(on)}(I_2 = 18A)}\right] \times R_{ds(on),nom} \times (39.22)^2 \times \frac{1}{3} \\
&= \left[(2.6254 \times 10^{-5} T_j^2 - 0.0079 T_j + 0.7647) \times \frac{1.3253 \times 10^{-4} I_1 + 0.9994}{1.3253 \times 10^{-4} I_2 + 0.9994}\right] \times 0.025 \times (39.22)^2 \times \frac{1}{3} \\
&= (2.6254 \times 10^{-5} T_j^2 - 0.0079 T_j + 0.7647) \times 1.0028 \times 0.025 \times (39.22)^2 \times \frac{1}{3}
\end{aligned}
\tag{28}
$$

For the IGBT, (29) can be used to compute the conduction loss under full load conditions, derived

from (19). Here, the forward voltage as a function of the collector-emitter current is modelled using a second order polynomial. The variation of the forward voltage with temperature is assumed to be linear between the temperature values provided in the datasheet (25° and 150°) at the operating current value. This assumption is valid because the voltage drop value will fall in between the maximum and room temperature value. A similar process can be repeated for the RB devices including the IGBT body diode, Si diode, SiC SBD, SiC MOSFET third quadrant channel, and GaN reverse conduction channel as described by (29)-(34).

$$\begin{aligned}
&P_{IGBT,cond} = V_{CE}(T_j = 150^\circ, I_{CE}) \times (39.22) \times \frac{1}{3} \\
&= \left[(16.8955I_{CE}^2 - 7.2002I_{CE} - 0.5787) \times \frac{V_{CE}(T_{j,1} = 125^\circ C, I_{ds} = 39.22A)}{V_{CE}(T_{j,2} = 150^\circ C, I_{ds} = 39.22A)}\right] \times (39.22) \times \frac{1}{3} \\
&= \left[(16.8955I_{CE}^2 - 7.2002I_{CE} - 0.5787) \times \frac{0.00264T_{j,1} + 1.51}{0.00264T_{j,2} + 1.51}\right] \times (39.22) \times \frac{1}{3} \\
&= (16.8955I_{CE}^2 - 7.2002I_{CE} - 0.5787) \times 0.965 \times (39.22) \times \frac{1}{3}
\end{aligned} \tag{29}$$

$$\begin{aligned}
&P_{Q,cond,SiC,lower} = V_{F,3rdQuad.}(T_j = 175^\circ C, I_{ds}) \times (39.22) \times (\frac{1}{3} - t_d \times f_{sw}) \\
&= \left[0.0297I_{ds} \times \frac{V_{F,3rdQuad.}(T_{j,1} = 125^\circ C, I_{ds} = 39.22A)}{V_{F,3rdQuad.}(T_{j,2} = 175^\circ C, I_{ds} = 39.22A)}\right] \times (39.22) \times (\frac{1}{3} - t_d \times f_{sw}) \\
&= \left[0.0297I_{ds} \times \frac{0.0026T_{j,1} + 1.035}{0.0026T_{j,2} + 1.035}\right] \times (39.22) \times (\frac{1}{3} - t_d \times f_{sw}) \\
&= 0.0297I_{ds} \times 0.913 \times (39.22) \times (\frac{1}{3} - 60 \times 10^{-9} \times f_{sw})
\end{aligned} \tag{30}$$

$$\begin{aligned}
&P_{D,cond,Si} = V_F(T_j = 175^\circ C, I_D) \times (39.22) \times \frac{1}{3} \\
&= \left[(53.54I_D^2 - 26.5636I_D + 2.0295) \times \frac{V_F(T_{j,1} = 125^\circ C, I_{ds} = 39.22A)}{V_F(T_{j,2} = 150^\circ C, I_{ds} = 39.22A)}\right] \times (39.22) \times \frac{1}{3} \\
&= \left[(53.54I_D^2 - 26.5636I_D + 2.0295) \times \frac{-0.0045T_{j,1} + 1.035}{-0.0045T_{j,2} + 1.035}\right] \times (39.22) \times \frac{1}{3} \\
&= (53.54I_D^2 - 26.5636I_D + 2.0295) \times 1.19 \times (39.22) \times \frac{1}{3}
\end{aligned} \tag{31}$$

$$\begin{aligned}
&P_{D,cond,IGBT} = V_F(T_j = 150^\circ C, I_D) \times (39.22) \times \frac{1}{3} \\
&= \left[(26.5537I_D^2 - 14.694I_D + 0.48) \times \frac{V_F(T_{j,1} = 125^\circ C, I_{ds} = 39.22A)}{V_F(T_{j,2} = 150^\circ C, I_{ds} = 39.22A)}\right] \times (39.22) \times \frac{1}{3} \\
&= \left[(26.5537I_D^2 - 14.694I_D + 0.48) \times \frac{0.00019T_{j,1} + 1.63}{0.00019T_{j,2} + 1.63}\right] \times (39.22) \times \frac{1}{3} \\
&= (26.5537I_D^2 - 14.694I_D + 0.48) \times 1.003 \times (39.22) \times \frac{1}{3}
\end{aligned} \tag{32}$$

$$
\begin{aligned}
P_{D,cond,SiC} &= V_F(T_j = 175°C, I_D) \times (39.22) \times \frac{1}{3} \\
&= \left[(24.75I_D^2 - 13.78I_D - 0.865) \times \frac{V_F(T_{j,1} = 125°C, I_{ds} = 39.22A)}{V_F(T_{j,2} = 175°C, I_{ds} = 39.22A)}\right] \times (39.22) \times \frac{1}{3} \\
&= \left[(24.75I_D^2 - 13.78I_D - 0.865) \times \frac{0.0015T_{j,1} + 1.35}{0.0015T_{j,2} + 1.35}\right] \times (39.22) \times \frac{1}{3} \\
&= (24.75I_D^2 - 13.78I_D - 0.865) \times 0.953 \times (39.22) \times \frac{1}{3}
\end{aligned}
\tag{33}
$$

$$
\begin{aligned}
P_{D,cond,GaN} &= V_F(T_j = 175°C, I_D) \times (39.22) \times \frac{1}{3} \\
&= \left[(0.202I_D^2 + 7.276I_D - 5.48) \times \frac{V_F(T_{j,1} = 125°C, I_{ds} = 39.22A)}{V_F(T_{j,2} = 150°C, I_{ds} = 39.22A)}\right] \times (39.22) \times \frac{1}{3} \\
&= \left[(0.202I_D^2 + 7.276I_D - 5.48) \times \frac{0.0271T_{j,1} + 2.82}{0.0271T_{j,2} + 2.82}\right] \times (39.22) \times \frac{1}{3} \\
&= (0.202I_D^2 + 7.276I_D - 5.48) \times 0.902 \times (39.22) \times \frac{1}{3}
\end{aligned}
\tag{34}
$$

3.2.3 Switching Losses

Since the switches in the CSI configuration are directly connected to the grid, the turn-on and turn-off energy will differ at each switching instant due to the AC voltage. To account for this, (35) suggests that the turn on/off energy at each switching instant/sample number in a given SVM sector, n, should be computed. To get the switching loss over one period of the fundamental, the summation of the turn-on and off energies are multiplied by the fundamental/grid frequency. Continuing, (36) and (37) provide an expression for the turn-on and turn-off energy respectively, and are substituted into (35) when carrying out the computations. Equations (36) and (37) assume a linear relationship between the turn-on/off energy, $E_{on/off}$, and the voltage across the switch at the turn-on/off instant, $V_{Son/off}$, as suggested in [68]. Therefore, $V_{Son/off}$ is the actual measured voltage across the switch and $V_{S,datasheet}$ refers to the test voltage for the energy curves provided in the manufacturer product details. The turn-on/off energy value is read from the datasheet at the DC-link current value. This can be carried out using curve fitting of Fig. 1.10 and substituting into the respective equations. It should be mentioned that the DC-link current will also vary but for switching loss calculations, the average value is sufficient, provided that the ripple is low (<12%). To account for the variation in switching energy with gate resistance, R_G, and T_j, the energy is scaled linearly with the given energy at the actual R_G and T_j and the datasheet value of R_G and T_j [68]. Once again, these facts are reflected in (36) and (37). Note that $E_{on/off}(T_j)$ can also be implemented using curve fitting of the curves presented in Fig. 1.11, where all curves can be approximated accurately using a first order polynomial. Due to the turn-on mechanism of diodes, the loss during this process can be neglected [73]. However, switching loss of diodes is dominant during

the turn-off process due to reverse recovery currents, and cannot be neglected. Equation (38) is used to estimate the reverse recovery loss of the series-connected diode/body diode of the RB device. Here, the reverse recovery charge, Q_{rr}, is scaled based on the operating current, $f_{fund.}$ is set to the grid frequency to get the average value over one cycle of the fundamental, and $V_{R,n}$ is the turn-off voltage at a given switching instant [73], [74].

$$P_{SW} = [(E_{on,1} + E_{on,2}... + E_{on,n}) + (E_{off,1} + E_{off,2}... + E_{off,n})] \times f_{fund} \tag{35}$$

$$\begin{aligned} E_{on,n} &= \frac{V_{Son,n}}{V_{S,datasheet}} \times E_{on,datasheet}(I_{DC}, T_j, R_G) \\ &= \frac{V_{Son,n}}{V_{S,datasheet}} \times \frac{E_{on}(T_j)}{E_{on}(T_{j,datasheet})} \times \frac{E_{on}(R_{G(on)})}{E_{on}(R_{G(on),datasheet})} \times E_{on,datasheet}(I_{DC}) \end{aligned} \tag{36}$$

$$\begin{aligned} E_{off,n} &= \frac{V_{Soff,n}}{V_{S,datasheet}} \times E_{off,datasheet}(I_{DC}, T_j, R_G) \\ &= \frac{V_{Soff,n}}{V_{S,datasheet}} \times \frac{E_{off}(T_j)}{E_{off}(T_{j,datasheet})} \times \frac{E_{off}(R_{G(off)})}{E_{off}(R_{G(off),datasheet})} \times E_{off,datasheet}(I_{DC}) \end{aligned} \tag{37}$$

$$P_{SW,D} = \frac{1}{4} \times Q_{rr} \times V_R \times f_{fund.} \times \frac{I_{DC} \times D}{I_{F,datasheet}} \tag{38}$$

The analysis of the switching loss in this section assumes ideal switching action of the CSI RB switch cell. This means that when a given upper switch turns on, the lower device immediately begins conducting and when the upper switch turns off, the lower device turns off (begins RB). In CSIs, low switching loss is inherent due to low commutation voltages when the grid voltage is around the zero-crossing point. For the upper switch in S_1, the switching loss is dominant in the even SVM sectors. In sector 1, the switching loss can be neglected because there is only one turn-on instant with relatively low commutation voltage. For sectors 3 and 5, upper S_1 remains off and therefore, there are no switching losses produced. For upper S_1, both the turn-on and turn-off loss are prominent in the 4th SVM sector, while only the turn-on loss dominates in the 6th sector. For sector 2, the turn-off losses of the upper switch for the last $N/2$ samples (or switching instances interchangeably) must be considered, where N is the number of samples in each sector. The following paragraph explains the reasoning behind why switching loss is dominant in different sectors.

Of course, the voltage across the switch, and as a result, the switching loss, depend on the prior and future space vector switch states. This is shown in Fig. 3.5. Here, the figure shows the space vector state with the corresponding voltage across S_1. For example, in sector 4 when transitioning from I_4 to I_5, the commutation voltage equals $V_{BA} - V_{CA}$. Similarly, when transitioning from I_5 to I_0, the commutation voltage equals V_{CA}. Similar arguments can be made in each switching loss dominant SVM sector. As mentioned, the turn-off loss at the end of sector 2 must be considered. This is due to the AC output

voltage. At the beginning of sector 2, V_{BA} and V_{CA} are negative and therefore, blocked by the lower device/diode. Toward the end of the sector duration, V_{BA} becomes positive, producing turn-off loss in the upper switch. The reason that switching loss is high in sector 4 is that V_{BA} and V_{CA} are at peak values for the entirety. This creates turn-on and off loss in the upper switch. In sector 6, V_{BA} is negative and V_{CA} is positive, resulting in higher turn-on loss than turn-off for the upper switch. The voltage across the entire S_1 (upper plus RB device) is shown in Fig. 3.4 with the corresponding gating signal and SVM sector. Similar analysis can be done for the lower device. The RB device's switching loss for S_1 is dominant in sectors 2 and 6. Again, these are sectors that have high reverse voltages (V_{CA} and V_{BA} are at peak negative values). The respective commutation voltages can be estimated using (39)-(44), where negative results are neglected. V_g is the RMS grid phase voltage, f_s is the SVM sampling frequency, and θ_{ref} is a derived reference angle, synthesized by the difference between the SVM reference angle, θ, and the grid angle. The SVM reference angle, can be estimated using the term in (45), where θ_{n-1} is the SVM reference angle value at the previous sample instant in degrees. Similar arguments can be made for each switch due to SVM's repeating nature. Practically, these equations can be used at low switching frequencies and scaled linearly for higher switching frequencies in order to keep a low amount of computations. They are also used for just S_1 and can be multiplied by 6 to account for all six switches assuming even loss distribution and no manufacturer error. Finally, it should be noted that the equations are derived at unity PF but even if the PF varies, the loss distribution will not see significant change [63].

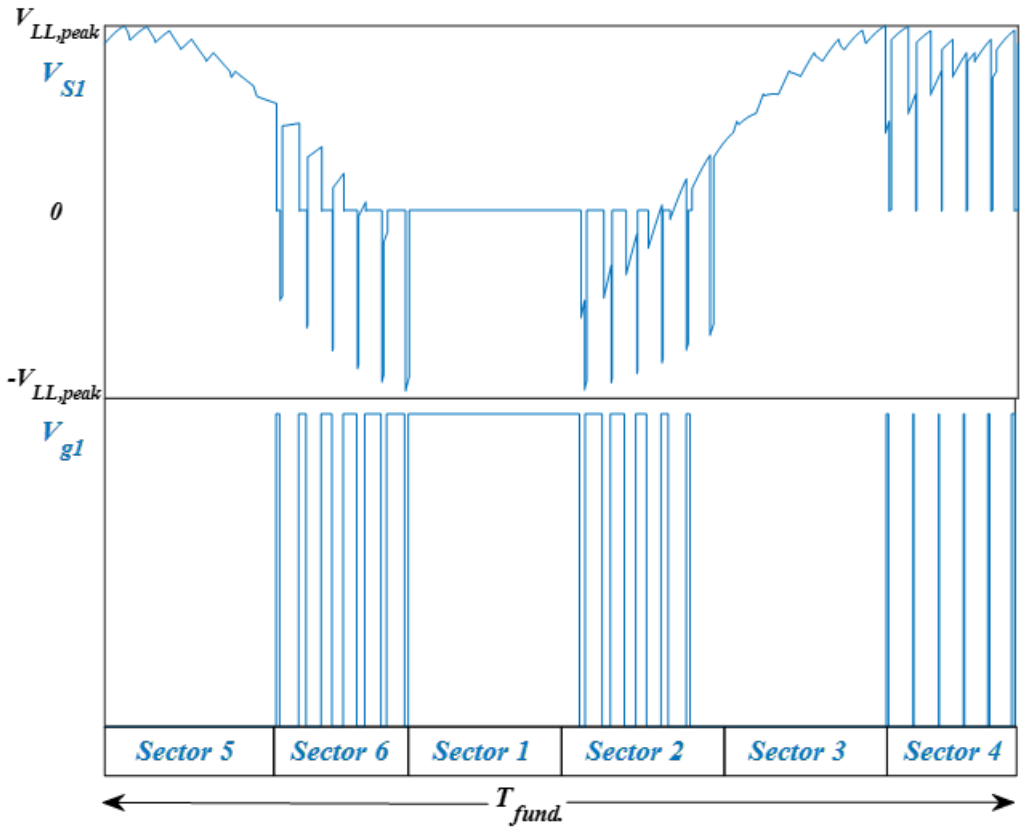


Figure 3.4: Commutation voltage of S_1, at f_{sw}=1080Hz.

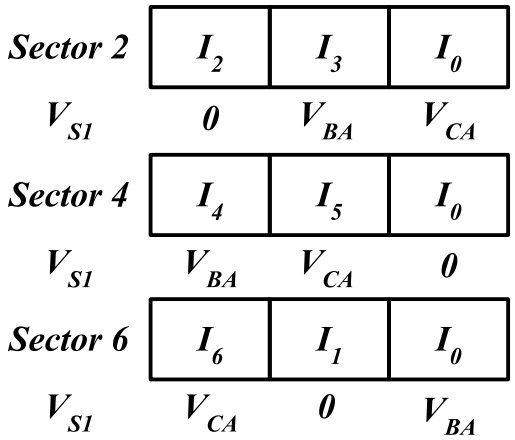


Figure 3.5: Voltage across S_1 during dominant switching loss sectors.

$$V_{S1,on(Sec.2)} = \sqrt{6}V_g cos(\theta + \theta_{ref} - 2|\frac{N}{2} - n| \times \frac{\pi}{180}) \tag{39}$$

$$V_{S1,on(Sec.4)} = \sqrt{6}V_g cos(\theta' - \frac{f_{fund.}}{f_s} \times 4(n-1) \times \frac{\pi^2}{180}) \tag{40}$$

$$V_{S1,off(Sec.4)} = \sqrt{6}V_g cos(\theta' - \frac{f_{fund.}}{f_s} \times (n-1) \times \frac{\pi^2}{180}) \tag{41}$$

$$V_{S1,on(Sec.6)} = \sqrt{6}V_g cos(\theta' - \frac{f_{fund.}}{f_s} \times (n-1) \times \frac{\pi^2}{180}) \tag{42}$$

$$V_{D1,off(Sec.2)} = \sqrt{6}V_g cos(\theta') \tag{43}$$

$$V_{D1,off(Sec.6)} = \sqrt{6}V_g cos(\theta' - \frac{f_{fund.}}{f_s} \times (2n - \frac{N}{2} + 1) \times \frac{\pi^2}{180}) \tag{44}$$

$$\theta' = \theta - \theta_{ref} = \theta_{n-1} + \frac{f_{fund.}}{f_s} \times 360 - \theta_{ref} \tag{45}$$

With the release of WBG devices, manufacturers have more motivation to provide switching energy curves at various conditions in order to show the superior switching performance. However, for conventional Si MOSFETs, no such curves are provided in the datasheet. Instead, calculations using the various capacitance and charge values provided are relied upon. In order to compute the switching loss of the selected Si MOSFET (STY112N65M5), the theory presented in [75] and [76] is used. First, the turn-on and turn-off energy at each switching instant are computed by (46) and (47) respectively. Where, $t_{fu,n}$ and $t_{ru,n}$ are the fall and rise time of the voltage across S_1 at each switching instant and are calculated based on the switching process of the Si MOSFET [75], [76]. These values can be computed with (48)-(51). Here, R_G is the sum of the selected external gate resistance and the internal gate resistance, V_{GS} is the selected gate driver voltage, and $V_{plat.}$ is the miller plateau voltage [75] - [77]. These equations assume the gate-to-drain capacitance dominates during switching transients. Therefore, $C_{gd,1,n}$ and $C_{gd,2,n}$ are the gate-to-drain capacitance at the voltage at the beginning of the switching process and the gate-to-drain capacitance at the voltage during the on-state ($I_{DC} \times R_{ds(on)}$) at each switching instant. Similarly, for

the voltage rise time, (50) and (51) can be used. The plateau voltage can be computed using (52), where V_{TH} is the threshold voltage, and K is the slope of the MOSFET's transfer characteristics [78]. The average value of the two rise and fall mechanisms is averaged using (53) and (54) and used in the energy equations [76]. Finally, substituting all factors into (55) will provide an estimate of the switching loss. The switching loss calculation results for all cases are shown in the next chapter.

$$E_{on,n} = V_{Son,n} * I_{DC} * t_{fu,n} \tag{46}$$

$$E_{off,n} = V_{Soff,n} * I_{DC} * t_{ru,n} \tag{47}$$

$$t_{fu,1,n} = V_{Son,n} \times R_G \times \frac{C_{gd,1}}{V_{GS} - V_{plat.}} \tag{48}$$

$$t_{fu,2,n} = V_{Son,n} \times R_G \times \frac{C_{gd,2}}{V_{GS} - V_{plat.}} \tag{49}$$

$$t_{ru,1,n} = V_{Soff,n} \times R_G \times \frac{C_{gd,1}}{V_{plat.}} \tag{50}$$

$$t_{ru,2,n} = V_{Soff,n} \times R_G \times \frac{C_{gd,2}}{V_{plat.}} \tag{51}$$

$$V_{plat.} = (V_{TH} + sqrt\frac{I_{DC}}{K}) \tag{52}$$

$$t_{fu,n} = \frac{t_{fu,1,n} + t_{fu,2,n}}{2} \tag{53}$$

$$t_{ru,n} = \frac{t_{ru,1,n} + t_{ru,2,n}}{2} \tag{54}$$

$$P_{fsw,Si} = (\sum E_{on,n} + \sum E_{off,n}) \times f_{fund.} \tag{55}$$

3.3 DC-link Inductor

3.3.1 DC-link Inductor Sizing

The size of the DC-link inductor is determined by (56) which is derived from the volt-second principle [59], [79]. The size of the inductor depends on the allowable current ripple ΔI_{dc}, often set to 12% of the rated DC-link current, the voltage across the inductor V_L, and the time duration that V_L is applied ΔT_s. These values are dependent on the modulation scheme used [79]. An analysis method is proposed in [79], where the voltage-second principle is applied to each SVM switch state, and the largest inductance value from these computations is selected to be the minimum inductance required to achieve the desired ripple current. As mentioned in a prior section, when a zero vector is applied, the DC-link voltage is zero, and when an active vector is applied the DC-link voltage is clamped to the grid voltage. Therefore, (57) can be written. Applying the voltage-second principle to SQ1 operating with a sampling frequency of 1080Hz results in (58). It should be noted that these are equations are written for sector 1, however, in any other sector, the resultant value of L_{dc} will be the same [79]. Essentially, (57) computes the area between V_{in} and V_{dc}, resulting in the required inductance value. Figures 3.6 and 3.7 show the PSIM model simulation using the C code block to detect the switch state and output the inductance value. The results show an inductor size of 3.42 mH, 1.71 mH, and 366 uH at f_{sw} of 1080 Hz, 2160 Hz, and 10080 Hz respectively.

$$L_{dc,min,SQ1} = \frac{V_L \times \Delta T}{\Delta I_{dc}} \tag{56}$$

$$V_L = \begin{cases} [S_1, S_6], V_{in} - v_{ab} \\ [S_1, S_2], V_{in} - v_{ac} \\ [S_2, S_3], V_{in} - v_{bc} \\ [S_3, S_4], V_{in} - v_{ba} \\ [S_4, S_5], V_{in} - v_{ca} \\ [S_5, S_6], V_{in} - v_{cb} \\ [S_1, S_4], [S_2, S_5], [S_3, S_6], V_{in} \end{cases} \tag{57}$$

$$L_{dc,min} = \begin{cases} [S_1, S_6], L_{dc,1} = \frac{|V_{in} - \bar{v_{ab}}| \times T_{1,1}}{0.12 \times I_{DC}} \\ [S_1, S_2], L_{dc,2} = \frac{|V_{in} - \bar{v_{ac}}| \times T_{2,1}}{0.12 \times I_{DC}} \\ [S_1, S_4], L_{dc,3} = \frac{V_{in} \times T_{0,1}}{0.12 \times I_{DC}} \\ [S_1, S_6], L_{dc,4} = \frac{|V_{in} - \bar{v_{ab}}| \times T_{1,2}}{0.12 \times I_{DC}} \\ [S_1, S_2], L_{dc,5} = \frac{|V_{in} - \bar{v_{ac}}| \times T_{2,2}}{0.12 \times I_{DC}} \\ [S_1, S_4], L_{dc,6} = \frac{V_{in} \times T_{0,2}}{0.12 \times I_{DC}} \\ [S_1, S_6], L_{dc,7} = \frac{|V_{in} - \bar{v_{ab}}| \times T_{1,3}}{0.12 \times I_{DC}} \\ [S_1, S_2], L_{dc,8} = \frac{|V_{in} - \bar{v_{ac}}| \times T_{2,3}}{0.12 \times I_{DC}} \\ [S_1, S_4], L_{dc,9} = \frac{V_{in} \times T_{0,3}}{0.12 \times I_{DC}} \end{cases} \tag{58}$$

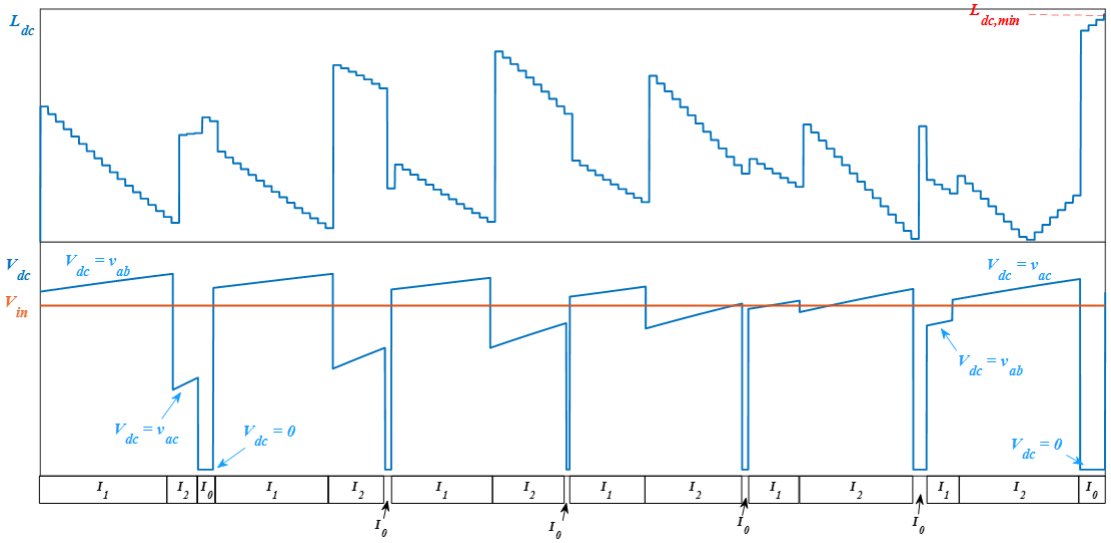


Figure 3.6: DC-link inductor sizing simulation results in sector 1 using SQ1 SVM (f_{sw}=1080 Hz, m_a=1, ΔI_{dc}=12%).

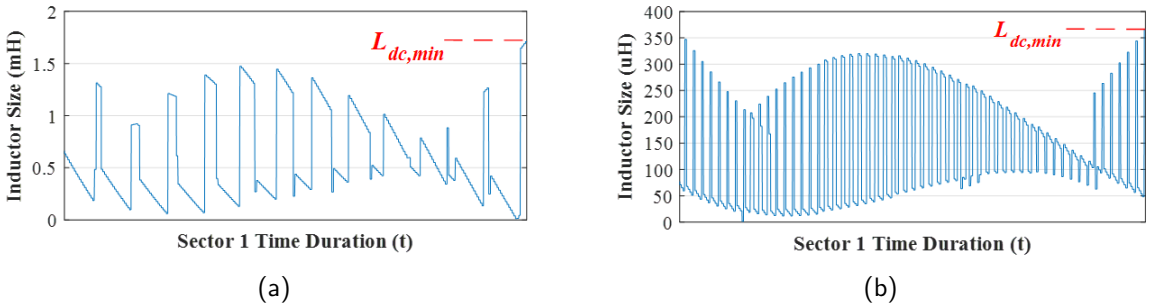


Figure 3.7: DC-link inductor sizing simulation results in sector 1 using SQ1 SVM (m_a=1, ΔI_{dc}=12%, C_f=0.325 pu): (a) f_{sw}=2160 Hz (b) f_{sw}=10080 Hz.

By observing these figures, it can be noted that the maximum inductance occurs during the final zero vector of each sector, irrespective of the switching frequency. Therefore, (59) can be written, where θ_{last} is the intersection point with the T_1 dwell time vector and the carrier during the final sampling period in any given sector, this point can be closely estimated using the (60). Here, θ_{start} is the SVM reference vector's angle at the start of the sector being analyzed and k is the sector number. Using the angle values in (60), results in the sine term always being 1/2 and results in the further simplified expression shown in (61). Two important points can be deduced from (61). That is, the equation agrees with simple physics that the inductor value will decrease disproportionately to switching frequency. Also, if V_{in} is adjusted in agreeance with grid-tied operation, the DC-link inductor will be at its maximum for m_a equal to one [79]. The DC-link inductor size for various switching frequencies from 1080 Hz to 100.08 kHz are provided in Table 9 (graphed in Fig. 3.8) along with additional parameters including the weight, volume, and loss parameters (to be discussed in the following section). Micrometal's inductor design tool found in [80] is used to extract the additional practical characteristics. The design tool doesn't provide an option to design for the DC-inductor current in CSI configuration. However, it provides the option for a boost converter. This is one assumption in this design process as the DC-current waveform produced by any given SVM sequence will differ from the square wave voltage across the inductor seen in a buck converter. Nevertheless, by selecting the on-voltage to V_{in} and the off-voltage to $(V_{in} - \hat{V}_{LL})/2$, the same current ripple value is achieved in the design tool, and the designed inductor produces the desired ripple current.

$$\begin{aligned} L_{dc,min} &= \frac{(Vin-0)\times T0}{\Delta Idc} = \frac{(Vin-0)\times(Ts-T2-T1)}{\Delta Idc} \\ &= \frac{(Vin-0)\times(Ts-3\times ma\times sin(\theta_{last}))}{\Delta Idc} = \frac{Vin\times(1-\sqrt{3}\times ma\times sin(\theta_{last}))}{2\times f_{sw}\times\Delta Idc} \end{aligned} \tag{59}$$

$$\theta_{last} = \begin{cases} (\theta_{start}+\frac{\pi}{3}) - (k-1)\times\frac{\pi}{3}, 0 \le \theta < \frac{11\pi}{6} \\ (\theta_{start}-\frac{5\pi}{3}), \frac{11\pi}{6} \le \theta \le 2\pi \end{cases} \tag{60}$$

$$L_{dc,min,SQ1} = \frac{V_{in}\times(1-\frac{\sqrt{3}}{2}m_a)}{2\times f_{sw}\times\Delta I_{dc}} \tag{61}$$

Table 9: DC-Link inductor design results at various switching frequencies for SQ1 SVM.

DC-link Inductor Parameter	**Switching Frequency (Hz)**							
	1080	***2160***	***5040***	***10080***	***20160***	***40320***	***80280***	***100080***
DC-Link Inductance (H)	$3.42m$	$1.71m$	732μ	366μ	183μ	91.5μ	48μ	38.5μ
Core Loss (W)	3.524	2.073	0.2977	0.763	1.051	1.088	1.465	1.709
DC Winding Loss (W)	47.438	38.809	28.201	14.261	5.934	3.556	2.279	1.478
AC Winding Loss (W)	0.402	0.380	0.203	0.285	0.161	0.134	0.119	0.086
Weight (g)	27500	10900	10400	5080	2660	2540	1080	779
Volume (cm^3)	2390	734	734	218	171	165	81.3	55.7

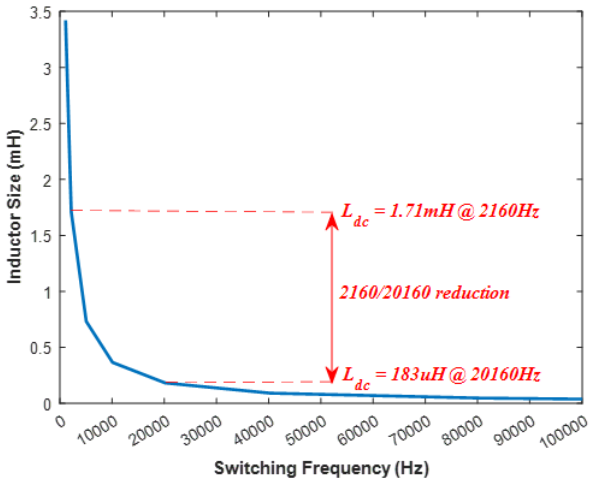


Figure 3.8: L_{dc} versus f_{sw} for SQ1 SVM.

3.3.2 DC-link Inductor Losses

The power losses associated with the DC-link inductor must be computed accurately to have a good idea of the power loss in the CSI. This is because the inductor is critical to CSI operation and cannot be bypassed or replaced. On top of that, the DC-link inductor produces a high amount of loss. As mentioned, the three types of loss are associated with the inductor: DC winding loss, AC winding loss, and core loss [81], [82], [83]. The DC winding loss results from the wire resistance and the DC current, computed using (62) [82]. As previously mentioned, Micrometals' inductor design tool was used to select the inductor parameters (Table 9). Through this tool, the DC resistance, R_{DC}, is provided. Since the method of determining R_{DC} is not disclosed by Micrometals, verification calculations were carried out to determine validity. Equation (63) is used to carry this out where r_L is the resistance per unit length of the selected wire gauge, N_T is the number of turns, and L_T is the mean length per turn [84]. Equation (64) is used to compute the resistance per unit length, where ρ is the conductivity of the wire material at 20°C ($1.68 \times 10^{-8}\Omega$m for copper) and d is the diameter of the American wire gage (AWG) wire [84]. It should be noted that all inductors selected use #2 AWG cable size based on the circular mills amp rule of thumb [85]. Equation (65) is used to adjust the resistance value based on the ambient temperature it is expected to be exposed to. In this expression, α is the temperature coefficient of the material, 0.00393 for copper. The results of the calculations are shown in Table 10.

$$P_{DC} = R_{DC} \times {I_{DC}}^2 \tag{62}$$

$$R_{DC} = r_L \times N_T \times L_T \tag{63}$$

$$r_L = \frac{4\rho}{\pi d^2} \tag{64}$$

$$R_{DC,T} = R_{DC,ref} \times (1 + \alpha(T - T_{ref})) \tag{65}$$

The AC winding loss is caused by the AC resistance of the wire. This is a theoretical resistance based on the skin effect and proximity effect [86]. The Micrometals inductor design tool computes the AC resistance to DC resistance ratio, R_{AC}/R_{DC}, value based on a modified Dowel model presented in [87]. Other methods are presented in [84]. Since the AC-resistance computation relies upon many geometrical variables of the inductor, conductors, and conductor spacing, that are not provided by the manufacturer, the values from the design tool are simply used. On top of that, the AC winding loss is only a small percentage of the overall inductor loss as shown in Table 9. Once the AC resistance is obtained, the loss produced by it can be computed using the equation below, where the current term equates to the RMS of the ripple current.

$$P_{AC,winding} = R_{AC} \times (\frac{\Delta I_{dc}}{\sqrt{2}})^2 \tag{66}$$

Next, the core losses are the result of an alternating magnetic field in the core of the inductor causing hysteresis and eddy currents [81], [82], [85]. Again, the design tool provides the core loss for the user. The method used involves computing the peak AC flux density using (72) [85]. In this equation, E_{rms} is the RMS voltage across the inductor, A_e is the effective cross-sectional area of the core, N_T is the number of turns, f is the frequency of the AC components, and the 10^8 factor comes from the conversion tesla to gauss [85]. From there, Micrometals provides curve fitting functions to model the inductor characteristics and performance. The design tool uses the curve fitting function for B_{pk} vs core loss per cm^3. This is shown in (68) where B_{pk} is expressed in gauss, f is the frequency of the AC components, and a-d are curve fitting values provided in the material datasheets [85], [88]. Equation (69) is used to convert the core loss from mW/cm^3 to watts (W) by using the effective cross sectional area and effective length of the core in cm^2 and cm respectively.

$$B_{pk} = \frac{E_{rms} \times 10^8}{4.44 \times A_e \times N_T \times f} \tag{67}$$

$$Core\ Loss = (\frac{mW}{cm^3}) = \frac{f}{\frac{a}{{B_{pk}}^3} + \frac{b}{{B_{pk}}^{2.3}} + \frac{c}{{B_{pk}}^{1.65}}} + d \bullet {B_{pk}}^2 \bullet f^2 \tag{68}$$

$$P_L(W) = Core\ Loss \times A_e \times L_e \times 10^3 \tag{69}$$

These calculations can be further verified using an alternate theoretical methods. For instance, a method for computing the core loss is provided in [89]. Here, the maximum and minimum magnetizing fields, H_{max} are H_{min}, are computed using (70) and (71) respectively, where N is the number of turns, l_e is the effective magnetic length, and ΔI_{dc} is the ripple current value. The $0.4 \times \pi$ term takes care of the conversion from AT/cm to Oersteds (Oe). The maximum occurs at the peak of the DC current ripple while the minimum occurs at the minimum value of the DC current. From this, the peak flux density

at either condition can be computed using the B-H curve of the material [89]. A curve fitted function of the B-H curve is provided for each core material in [88] and is shown in (72). Here, H is the magnetizing force in Oe, u_i is the reference permeability, and a-d are curve fitting values provided in the datasheet. The average value between the two is used as the peak flux density to be substituted into (68). The calculation results using this method are shown in Table 10 and the relative loss compares the results form Table 9 presented in the previous section.

$$H_{max} = 0.4 \times \pi \times \frac{N}{l_e}(Idc + \frac{\Delta Idc}{2}) \tag{70}$$

$$H_{min} = 0.4 \times \pi \times \frac{N}{l_e}(Idc - \frac{\Delta Idc}{2}) \tag{71}$$

$$B_{pk} = \frac{u_i}{\frac{1}{H+aH^b} + \frac{1}{cH^d} + \frac{1}{e}} \tag{72}$$

$$B_{pk} = \frac{Bpk(H_{max}) - Bpk(H_{min})}{2} \tag{73}$$

Table 10: DC-Link inductor loss calculations and relative error when compared to the Micrometals design tool (Table 9).

f_{sw} ***(Hz)***	***1080***	***2160***	***5040***	***10080***	***20160***	***40320***	***80280***	***100080***
DC Winding Loss Calc. (W)	44.965	36.136	12.874	13.536	5.673	3.423	2.179	1.408
Relative Error (%)	5.34	5.79	4.35	5.41	4.40	3.74	4.39	4.74
Core Loss Calc. (W)	2.94	1.82	3.129	0.673	0.896	0.978	1.33	1.395
Relative Error (%)	17.09	13.5	19.42	16.62	14.75	10.1	9.2	18.38

By observing Table 10, it can be noted that the DC winding power loss can be estimated accurately with fundamental equations or the Micrometals design tool. Given that the relative error is less than 6% for all calculations, the values provided by Micrometals are verified. Any small amount of error can be accounted for by a difference in the selected temperature scaling methods (α constant), the diameter value, ρ constant, or simply rounding. For the core loss calculation, a higher relative error is consistent across all calculations. This is caused by the fact that the design tool simply computed the peak flux density at the maximum current value, whereas the theoretical method covered averaged the maximum and minimum cases. Regardless, the results are within a few watts of each other but the Micrometals results will be used in the following chapter to have a 'worst case scenario' situation.

Of course, increasing the switching frequency will decrease the associated power losses. However it is worth noting the two mechanisms that enable this. First, with reduced inductance comes reduced number of turns and winding length. This will reduce the winding resistance losses as per (63). The next is the fact that there are cores developed specifically for high switching applications that will have lower core loss characteristics. For instance sendust alloy powder cores enable MHz switching frequency while molypermalloy, silicon iron, and nickel iron enable low core losses up to 200 kHz [90]. For iron powder cores, the core material based on the application's switching frequency can be found in [85].

3.3.3 DC-link Inductor Sizing with Different SVM Sequences

Since the size of the DC-link inductor depends on the voltage across the DC-link inductor and the time duration of said voltage, changing the space vector sequence affects the required inductance. Hence, this section repeats the analysis in the prior section in order to size the inductor for each SVM sequence. Equations are derived for each case and the results are compared to determine which sequence minimizes the DC-link inductor (Table 11). To start with, the simulation results of the DC-link inductor size for SQ2 SVM for f_{sw} set to 1080 Hz, 2160 Hz, and 10080 Hz are shown in Fig. 3.9, Fig. 3.10 (a), and Fig. 3.10 (b) respectively. At 1080 Hz, the result is a 3.23 mH (0.282 pu) inductor. Of course, as the switching frequency increases, the inductor size decreases proportionally. This results in inductor sizes of 1.59 mH and 318.5 uH at 2160 Hz, and 10080 Hz. By observing figures 3.9 and 3.10, it can be noted the maximum inductance occurs during the T_2 dwell time around the middle sample instant ($\frac{N}{2} - 1^{th}$ sample). Therefore, (74) can be written, where θ is estimated by (75). Here, θ_{start} is the SVM angle at the beginning of the sector.

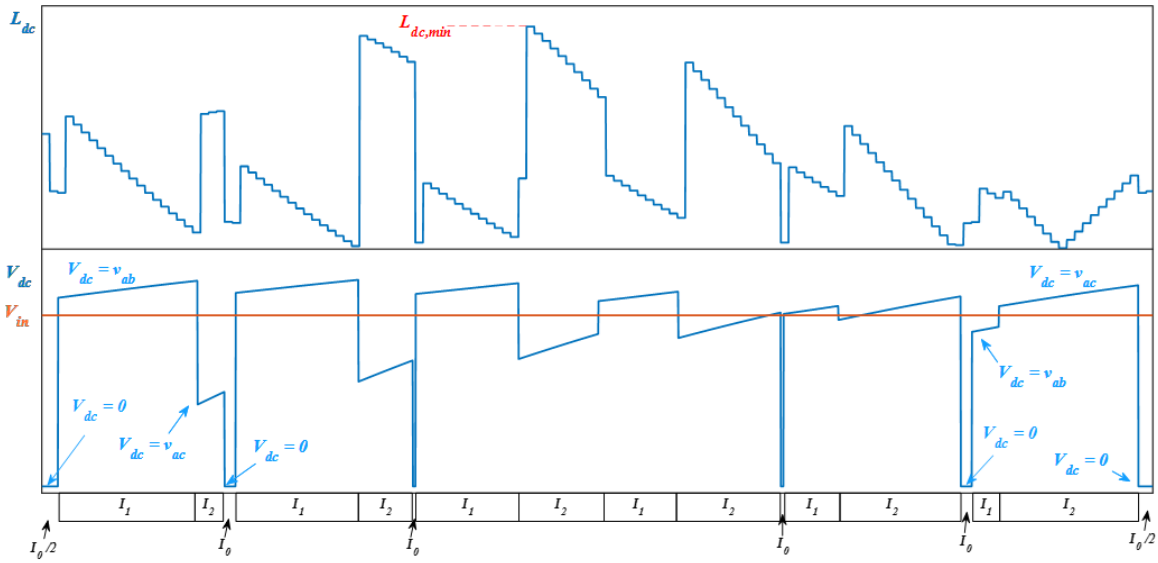


Figure 3.9: DC-link inductor sizing simulation results in sector 1 using SQ2 SVM (f_{sw}=1080Hz, m_a=1, ΔI_{dc}=12%, C_f=0.25 pu).

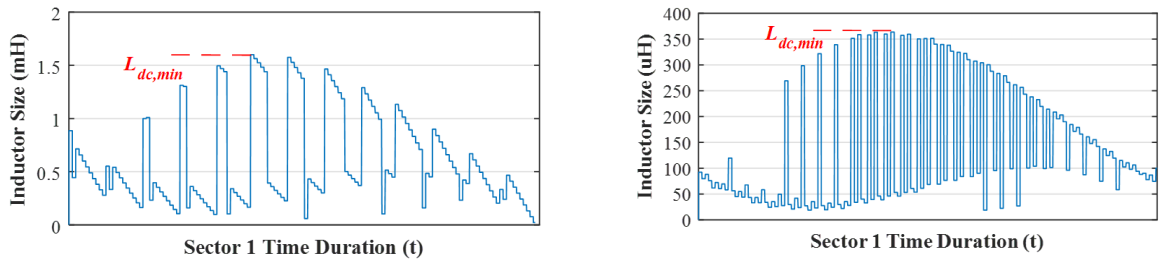


Figure 3.10: DC-link inductor sizing simulation results in sector 1 using SQ2 SVM (m_a=1, ΔI_{dc}=12%): (a) f_{sw}=2160 Hz (b) f_{sw}=10080 Hz.

$$L_{dc,min,SQ2} = \frac{(V_{in} - v_{ac}) \times T_2}{\Delta I_{dc}} = \frac{m_a \times (V_{in} - \sqrt{3} V_g cos(\theta)) \times sin(\theta + \frac{\pi}{6})}{2 \times f_{sw} \times \Delta I_{dc}} \tag{74}$$

$$\theta = (\frac{N}{2} - 1) \times \frac{f_{fund.}}{f_s} \times 360 + \theta_{start} \tag{75}$$

Moving onto SQ3, the simulation results are shown in figures 3.11 and 3.12 for the same range of switching frequency. Note, that the same sampling frequencies selected for the SQ2 case are used (2160 Hz, 4320 Hz, and 20160 Hz). However, since the SQ3 pattern decreases the switching frequency, there is a slight reduction in switching frequency (60 Hz reduction). The resulting values at the mentioned frequencies are 5.54 mH, 2.86 mH, and 622 uH. Again, the maximum inductance occurs during the T_2 vector at the middle sample value ($\frac{N}{2} + 1^{th}$ sample). Therefore, (74) can also be used to estimate the inductance for SQ3. However, the angle computation must be adjusted as in (76).

$$\theta = (\frac{N}{2} + 1) \times \frac{f_{fund.}}{f_s} \times 360 + \theta_{start} \tag{76}$$

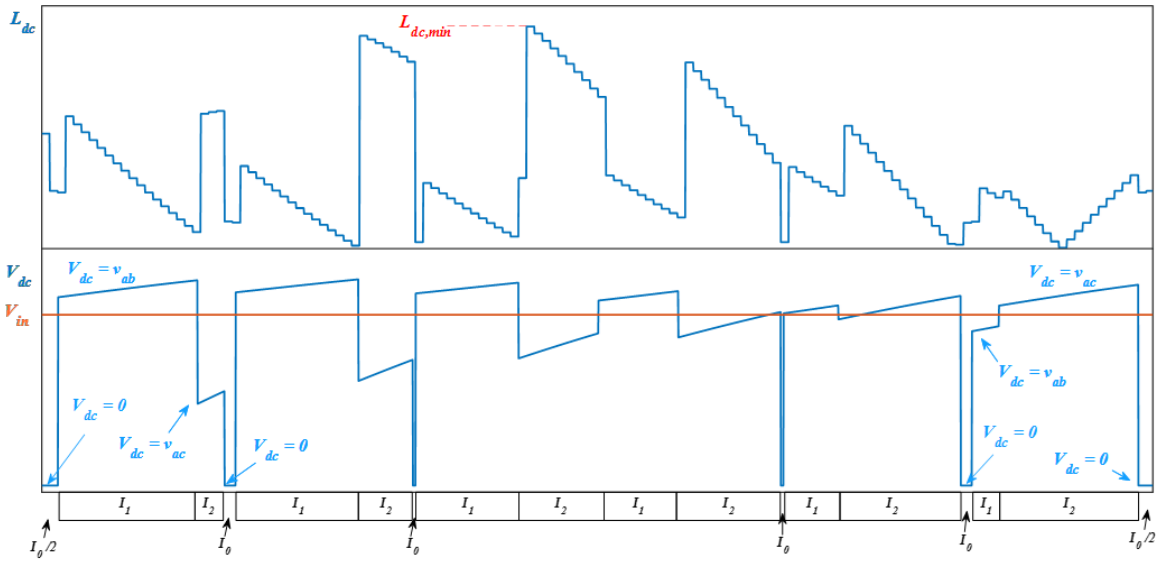


Figure 3.11: DC-link inductor sizing simulation results in sector 1 using SQ3 SVM (f_{sw}=1020 Hz, m_a=1, ΔI_{dc}=12%, C_f=0.59 pu).

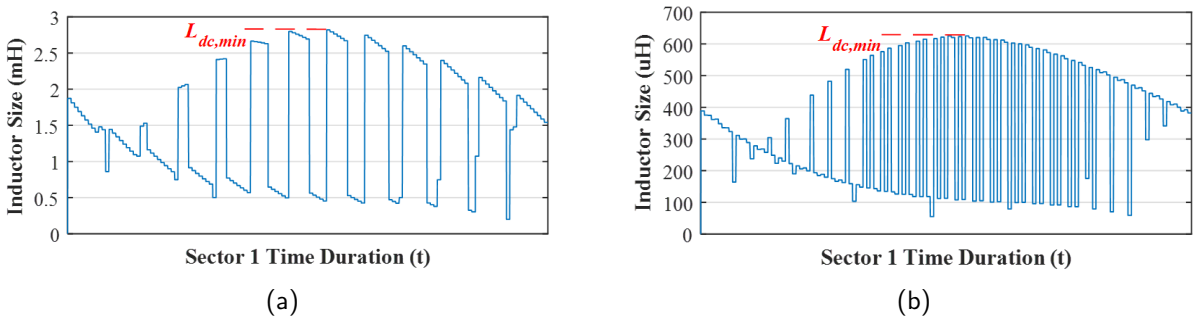


Figure 3.12: DC-link inductor sizing simulation results in sector 1 using SQ3 SVM (m_a=1, ΔI_{dc}=12%): (a) f_{sw}=2100 Hz (b) f_{sw}=10020 Hz.

For SQ4, the maximum inductance also occurs around a middle sample instant during T_2. This is seen in figures 3.13 and 3.14 for switching frequencies of 1080 Hz, 2040 Hz, and 10260 Hz (f_s= 1800 Hz, 3960 Hz, 20520 Hz accordingly). It should be noted that SQ4 requires an odd number of samples in a given sector in order to keep waveform symmetry in the PWM current. Therefore, 2160 Hz and 10080 Hz are not obtainable, it will become SQ5, in terms of harmonic performance. To keep the comparison fair, the harmonic performance must behave the same, therefore, the closest obtainable switching frequencies are selected. The resulting inductor sizes are 4.23 mH, 2.21 mH, and 445 uH as the frequency increases. Since the maximum inductance occurs during the T_2 dwell time, (74) can be used once again. However, the angle equation must be slightly tweaked as shown in (77).

$$\theta = (\frac{N}{2} - \frac{1}{2}) \times \frac{f_{fund.}}{f_s} \times 360 + \theta_{start} \tag{77}$$

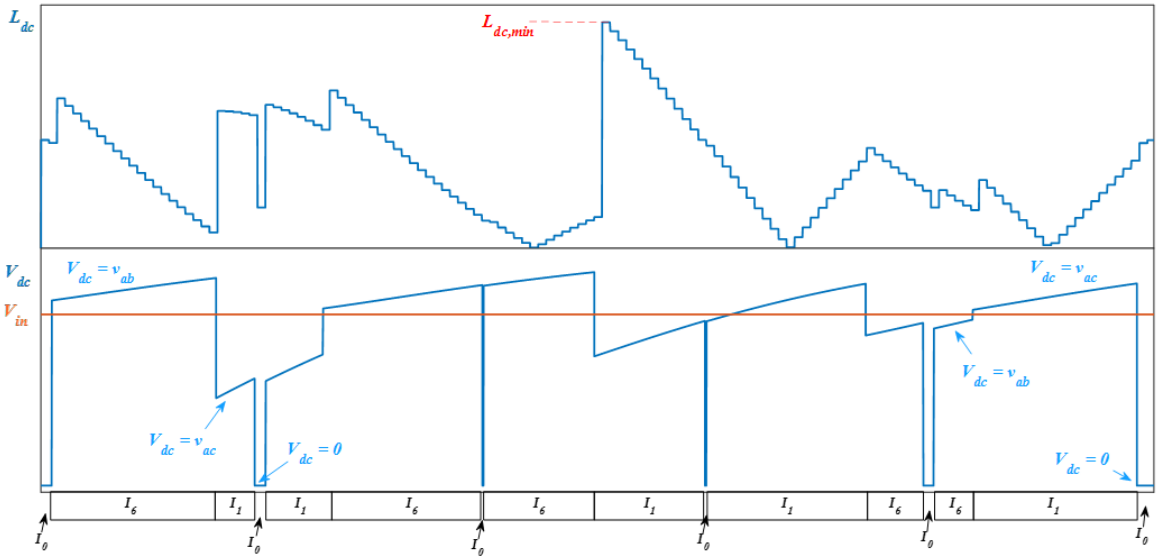


Figure 3.13: DC-link inductor sizing simulation results in sector 1 using SQ4 SVM (f_{sw}=1080 Hz, m_a=1, ΔI_{dc}=12%, C_f=0.3 pu).

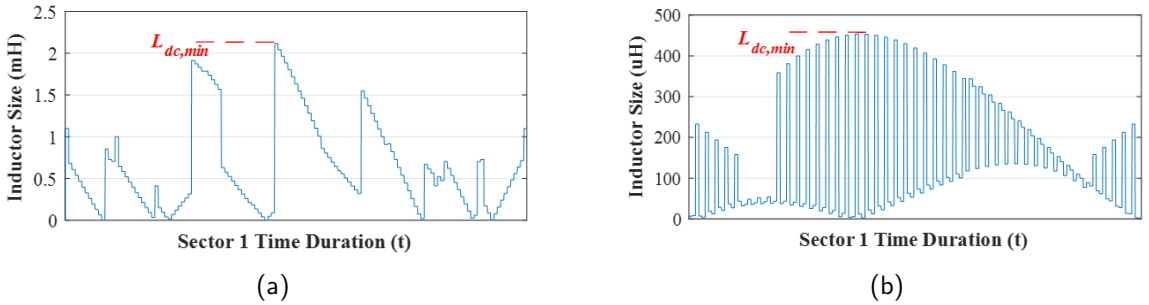


Figure 3.14: DC-link inductor sizing simulation results in sector 1 using SQ4 SVM (m_a=1, ΔI_{dc}=12%): (a) f_{sw}=2040 Hz (b) f_{sw}=10080 Hz.

For SQ5, the results for the DC-link inductor sizing are shown in figures 3.15 and 3.16. The sampling frequencies are 2880Hz, 5760Hz, and 26880Hz resulting in switching frequencies of 1080 Hz, 2160 Hz, and 10080 Hz. The required inductance for each switching frequency is 5.92 mH, 2.98 mH, and 650 uH. Again, the maximum DC-link inductance occurs during the middle sample T_2 dwell time. However, for the lowest switching frequency, the maximum inductance occurs during the transition from the first T_1 dwell time to the T_2 dwell time. If Fig. 3.15 is observed closely, the peak during the middle T_2 vector is very close to the maximum and will be assumed as so in order to reuse (74). Similar to the prior sections, the angle term can be corrected for SQ5 using (78).

$$\theta = (\frac{N}{2} + 2) \times \frac{f_{fund.}}{f_s} \times 360 + \theta_{start} \tag{78}$$

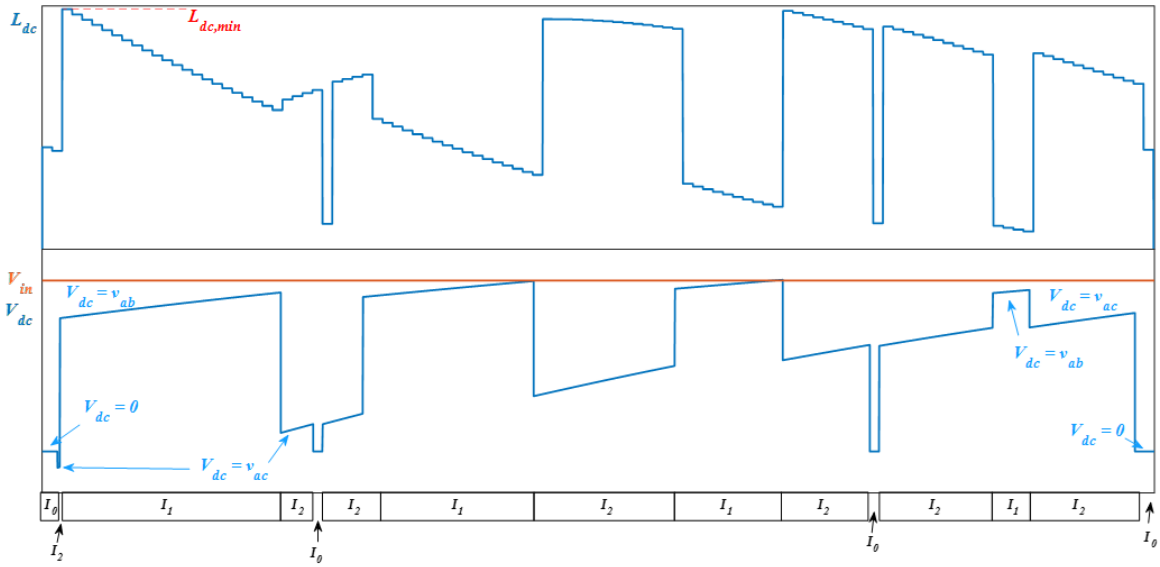


Figure 3.15: DC-link inductor sizing simulation results in sector 1 using SQ5 SVM (f_{sw}=1080 Hz, m_a=1, ΔI_{dc}=12%, C_f=0.8 pu).

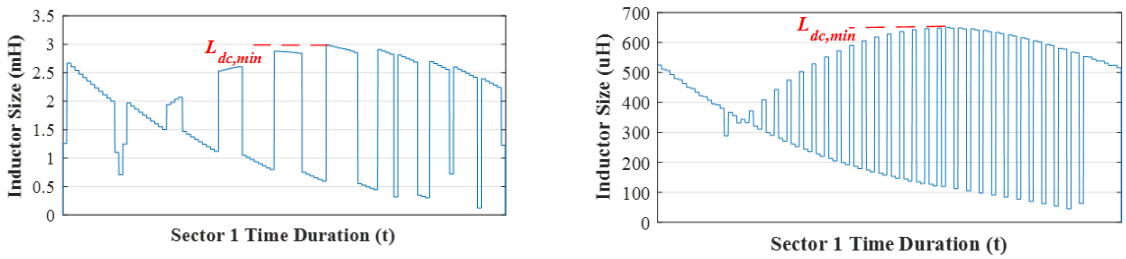


Figure 3.16: DC-link inductor sizing simulation results in sector 1 using SQ5 SVM (m_a=1, ΔI_{dc}=12%): (a) f_{sw}=2160 Hz (b) f_{sw}=10080 Hz.

The results for the DC-link inductor sizing for SQ6 are shown in figures 3.17 and 3.18. The same sampling/switching frequencies used for SQ5 are reused here. The resulting inductor sizes are 4.17 mH, 2.24 mH, and 514.92 uH respectively. Once again, the maximum inductance occurs during the T_2 vector. So (74) can be used along with the modified angle below.

$$\theta = (\frac{N}{2} - 1) \times \frac{f_{fund.}}{f_s} \times 360 + \theta_{start} \tag{79}$$

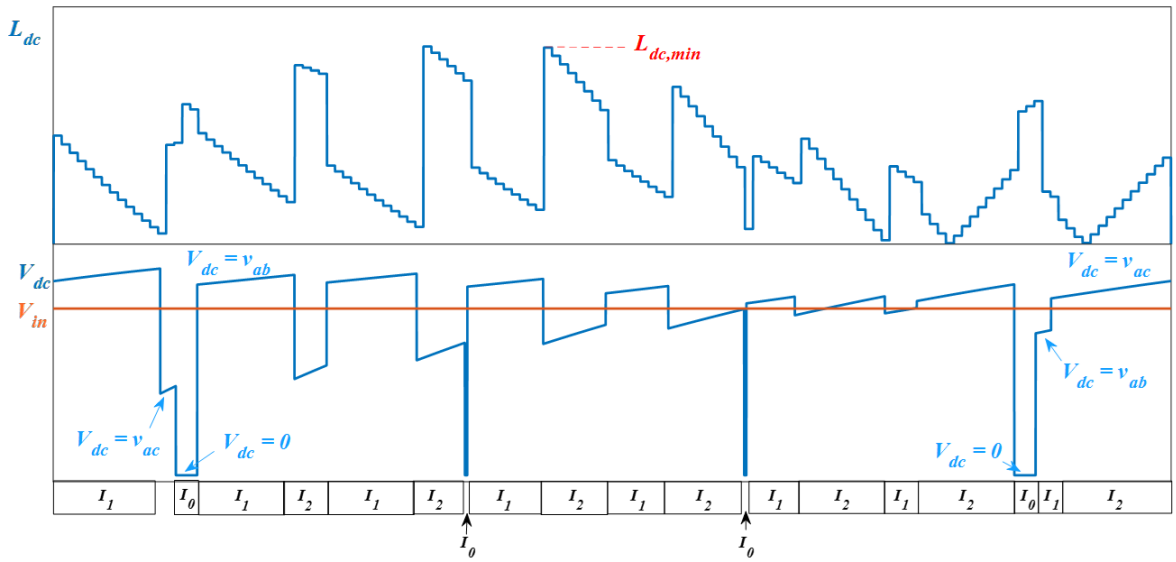


Figure 3.17: DC-link inductor sizing simulation results in sector 1 using SQ6 SVM (f_{sw}=1080 Hz, m_a=1, ΔI_{dc}=12%, C_f=0.325pu).

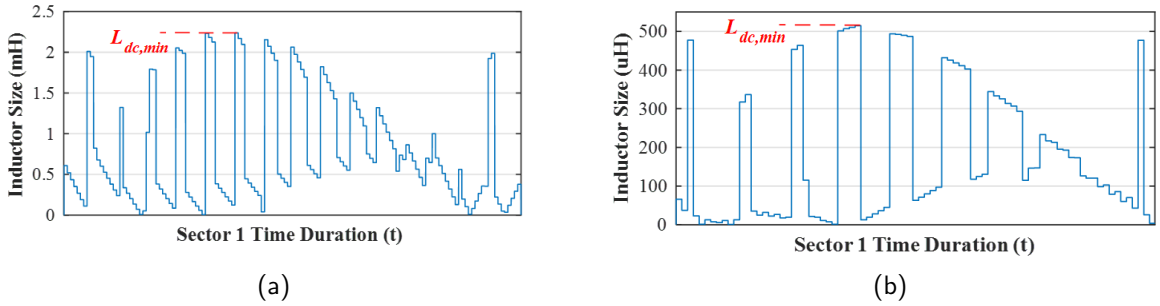


Figure 3.18: DC-link inductor sizing simulation results in sector 1 using SQ6 SVM (m_a=1, ΔI_{dc}=12%): (a) f_{sw}=2160 Hz (b) f_{sw}=10080 Hz.

The results of all inductor sizes and calculations using the equations presented throughout the section are shown in Table 11. There is little relative error between calculated and simulated values, meaning that the equations provide a good estimate of the DC-link inductor size required to achieve the desired ripple current value. In terms of minimizing the DC-link inductor size, SQ2 provides the lowest value followed closely by SQ1. Using Micrometal's inductor design tool, the loss distribution for the selected inductors for each sequence at f_{sw} set to 10 kHz are shown in Table 12. These computed sizes and losses will be used in Chapter 4 in order to compare the total loss distribution between CSIs

implementing each sequence. For fair comparison, the same core is used to show the effect of the inductor size on the corresponding losses.

Table 11: DC-Link Inductor Design Results At Various Switching Frequencies for SQ1-SQ6 SVM.

fsw / ***SQ***	***1080Hz (1020 for SQ3)***	***2160Hz (2100 for SQ3, 2040 for SQ4)***	***10080Hz (10020 for SQ3)***
SQ1	3.42m	1.71m	366u
SQ1 Calc.	3.36m	1.68m	360.07u
SQ2	3.23m	1.59m	318.5u
SQ2 Calc.	3.38m	1.69m	326.2u
SQ3	5.54m	2.86m	622u
SQ3 Calc.	6.23m	2.71m	592u
SQ4	4.23m	2.21m	445u
SQ4 Calc.	4.64m	2.33m	480.56u
SQ5	5.92m	2.98m	650u
SQ5 Calc.	5.65m	2.19m	680.22u
SQ6	4.17m	2.24m	514.92u
SQ6 Calc.	4.39m	1.95m	481.92u

Table 12: DC-Link inductor design results using Mircometal's E827-34 core at various SVM sequences (f_{sw} = 10 kHz).

DC-Link Inductor Parameters	**SVM Sequence**					
	SQ1	***SQ2***	***SQ3***	***SQ4***	***SQ5***	***SQ6***
DC-Link Inductance (μH)	366	318.5	622	445	650	514.92
Inductor Core Loss (W)	3.583	3.098	4.953	4.217	6.418	5.140
DC Winding Loss (W)	6.547	5.753	11.15	8.182	11.92	9.304
AC Winding Loss (W)	0.0475	0.0417	0.0809	0.0594	0.0865	0.0675

Now that the design of the DC-link inductor for various SVM sequences and switching frequency are complete, it is worth noting considerations that limit the downsizing of the inductor. The first and most dominant reason is thermal considerations. Since increasing the switching frequency is effective at decrease the core area, the smaller core will usually have higher temperature per area unit due to heat as a byproduct of core and winding loss [85], [91]. This can cause thermal runaway due to the fact that most cores have a loss coefficient that is positive with temperature once a critical value is reached [91]. The second factor is the operation of the inverter itself. For instance, decreasing the inductor will reduce the effects of the inherent short circuit protection that the CSI offers.

3.4 CL Filter

This section analyzes the sizing of the CL low-pass filter components, their associated losses, and an optimization method. There are four main variables that affect the sizing. They include the harmonic distortion limits, resonant frequency, quality factor, and efficiency. The first section analyzes a method of sizing the filter capacitor based on the corresponding IEEE standard with a fixed value of filter inductance. Next, the effect of quality factor and resonant frequency on the filter performance is analyzed. Design constraints based on the desired filter performance are set. Minimum requirements for component size

are derived from this. Section 3.4.3 provides loss functions for the filter inductor and capacitor in order to have an understanding of their associated losses. Finally, a method for minimizing the power losses without sacrificing filter performance is presented. The filter configuration considered is shown in Fig. 3.19. The designs are carried out with unity m_a since the CSI will mostly operate at this value to extract maximum power from the PV array [4], [59]. The assumptions for any analysis in this section include ideal inductor and capacitor values (no fluctuations in values or manufacturer error) and any induced phase angle by the filter is minimal and can be corrected with one of the many control schemes covered in literature [92], [93]. The overall goal is to have filter components and their loss values selected for SQ1 SVM with f_{sw} equalling 1 kHz to 100 kHz and for SQ1-SQ6 at f_{sw} at 10 kHz for the analysis in Chapter 4.

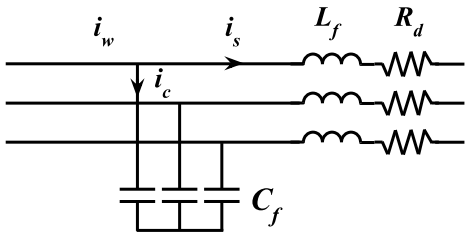


Figure 3.19: CL Filter Configuration.

3.4.1 Filter Capacitor Sizing Based on Harmonic Requirements with Fixed Inductance

As previously discussed, the CL filter at the output of the CSI is used to filter harmonics from the PWM current waveform. This will ensure a good quality current waveform is supplied to the grid. The definition of "good quality" grid current is defined by the IEEE 519-2014 standard [5], [67]. The standard defines two main rules: (1) the THD must be less than or equal to 5%, and (2) the individual harmonic components must be below the values defined in Table 13 [67], [94]. Notice, the standard only defines individual harmonic limitations on odd-order, non-triplen harmonics from 5-49. In order to design for these requirements, the magnitude of the filter TF, shown in Equation (80), must be used. Also, an idea of the typical harmonic component magnitudes is required. Using the frequency modulation index, m_f, the harmonic content of the PWM current can be generalized across all switching frequencies [95]. Table 14 shows the results of the generalized harmonic spectrum considering only the most dominant harmonics, where m_f is defined in (81). The generalized harmonic spectrum for SQ2-SQ6 SVM can be found in the Appendix Table A1-A5.

Table 13: IEEE 519-2014 Individual Harmonic Component Limitations

Harmonic Number	**5&7**	**11&13**	**17&19**	**23, 25, 29, 31**	**35, 37, 41, 43, 47, 49**
Percentage of the fundamental $I_{w,n}/I_{w,1}$ (%)	4	2	1.5	0.6	0.3

$$I_s(n) = \frac{1}{\sqrt{(j\omega nRC_f)^2 + ((j\omega n)^2 L_f C_f + 1)^2}} \times I_w(n) \tag{80}$$

Table 14: Dominant harmonics for SQ1 SVM expressed in terms of m_f for m_a=1.

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental (%)***
$m_f - 13$	0.6
$m_f - 11$	0.65
$m_f - 7$	1.8
$m_f - 5$	1.2
$m_f - 1$	12.5
$m_f + 1$	29
$m_f + 5$	25
$m_f + 7$	12
$m_f + 11$	3
$m_f + 13$	3
$m_f + 17$	5
$m_f + 19$	18
$m_f + 23$	4
$m_f + 25$	8
$m_f + 29$	12
$m_f + 31$	10

$$m_f = \frac{f_s}{f_{fund.}} \tag{81}$$

Now that key variables are defined, the procedure for determining the required filter capacitance must be discussed. First, to meet individual harmonic limitations, (80) is applied to each harmonic, where the IEEE 519-2014 requirement value is substituted for $I_s(n)$ and the harmonic content value from Table 14 is substituted for $I_w(n)$. From this, the required capacitance is determined for each individual harmonic component and the maximum value is taken as the overall required capacitance. An example of this procedure is shown in Table 15 where the required filter capacitance is derived for SQ1 SVM operating at a switching frequency of 1080Hz. The resulting capacitance is 0.8048 pu or 494.16 µF to meet the IEEE requirement for the 41^{st} harmonic. To check the required capacitance for the first rule, THD less than 5%, the resulting THD with varying capacitance can be plotted as in Fig. 3.20. The resulting capacitance is 29.6 µF. Since the required capacitance for the individual harmonics is larger, that value is selected in order to comply with the standard.

Since using the dominant harmonics is an estimate, the actual harmonic content is extracted from a PSIM simulation and the calculations are carried out in the second row of Table 16. By comparing the two results, it can be seen that the dominant harmonic assumption generally over estimates the filter capacitance by a relatively small margin. Through this comparison, the approximation is deemed reliable and used in future analysis presented. Now, the effect of varying the switching frequency must be discussed. Since IEEE 519-2014 only defines limitations on the 5th-50th harmonic number, once

Table 15: Filter capacitance design results for SQ1 SVM at f_{sw}=1080 Hz and L_f = 0.1 pu considering individual harmonics.

SQ1 SVM f_{sw} = 1080Hz												
Harmonic Order	***23***	***25***	***29***	***31***	***35***	***37***	***41***	***43***	***47***	***49***	***53***	***55***
IEEE Requirement	0.6	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	N/A	N/A
i_w (%)	0.6	0.65	1.8	1.2	12.5	29	25	12	3	3	5	18
Req. C_f (pu)	0	0	0	0	0.2206	0.4582	0.8048	0.3513	0.0735	0.0677	-	-

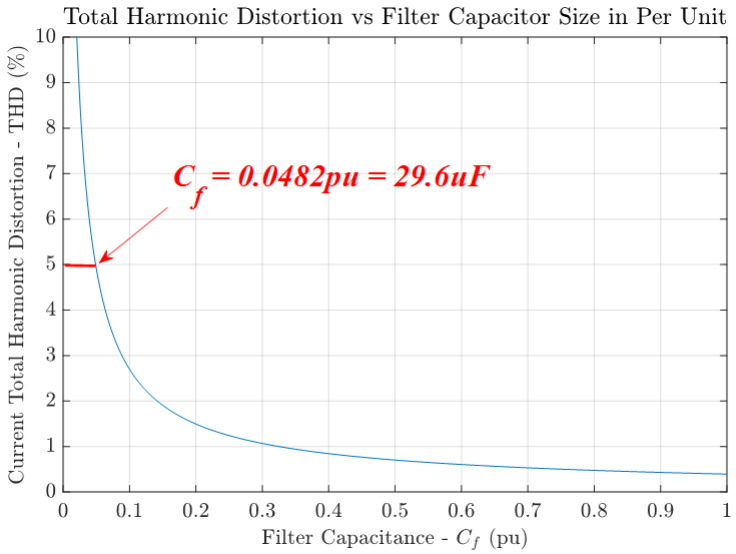


Figure 3.20: Capacitor design results for SQ1 SVM with f_{sw}=1080Hz and L_f = 0.1pu considering only the THD<5% requirement.

the sampling frequency of the CSI is increased to a certain value, these harmonic values will naturally meet the limitations. Again, using the results in Table 14, the value of sampling frequency is 3420 Hz (m_f=57). Therefore, when operating at a sampling frequency greater than or equal to 3420 Hz, the filter design procedure simplifies. Meaning, the only requirement to design for is the THD<5% rule and the computations for each individual harmonic can be skipped. The design results for the filter capacitance at switching frequencies of 2160 Hz and 10080 Hz are shown in Fig. 3.21. The design results for SQ1-SQ6 at a switching frequency of 10080 Hz are summarized in Table 17 and shown in Fig. 3.22. From these graphics, it can be seen that SQ1 and SQ2 produce less harmonic content than the other four sequences, resulting in the smallest capacitor values. SQ4 has the worst harmonic performance resulting in the largest required minimum capacitance, followed by SQ3, SQ5, and SQ6.

Table 16: Filter capacitance design results at various switching frequencies for SQ1 SVM with L_f = 0.1 pu.

f_{sw} (kHz)	***1***	***2***	***5***	***10***	***20***	***40***	***80***	***100***
Capacitance (μF) (Dominant Harmonic Approximation)	494.16	19.28	2.83	0.644	0.141	0.0456	0.00142	0.00328
Capacitance (μF) (Simulated Harmonic Spectrum)	420.14	19.65	1.965	0.511	0.125	0.0324	0.00841	0.00219

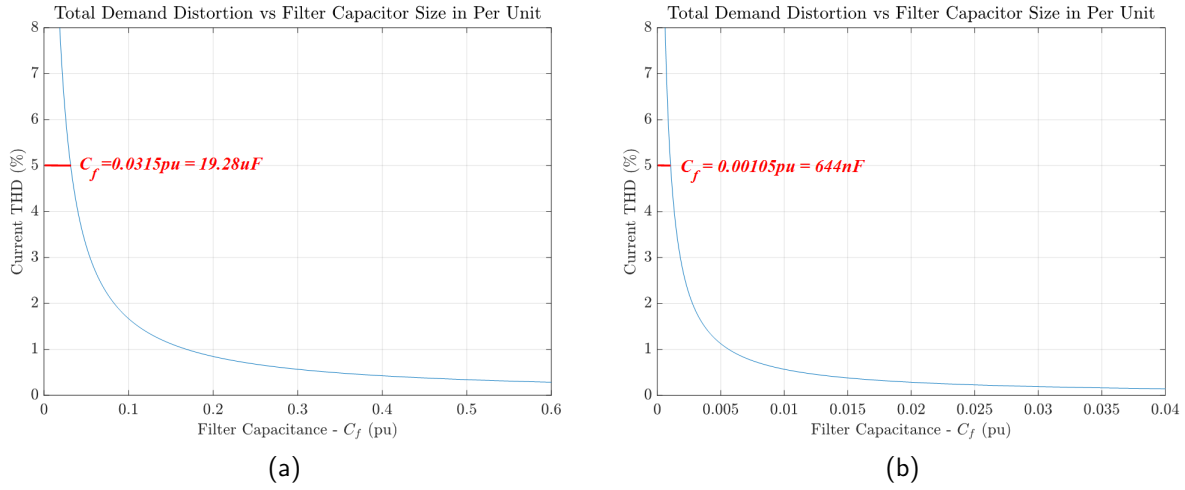


Figure 3.21: Filter capacitor design results for SQ1 SVM (a) f_{sw}=2160 Hz (b) f_{sw}=10080 Hz ($m_a = 1$).

Table 17: Capacitance design results for SQ1-SQ6, $L_f = 0.1$ pu, approximate f_{sw}=10 kHz.

SVM Sequence	SQ1	SQ2	SQ3	SQ4	SQ5	SQ6
Capacitance (µF)	0.644	0.653	5.258	21.79	3.59	2.76

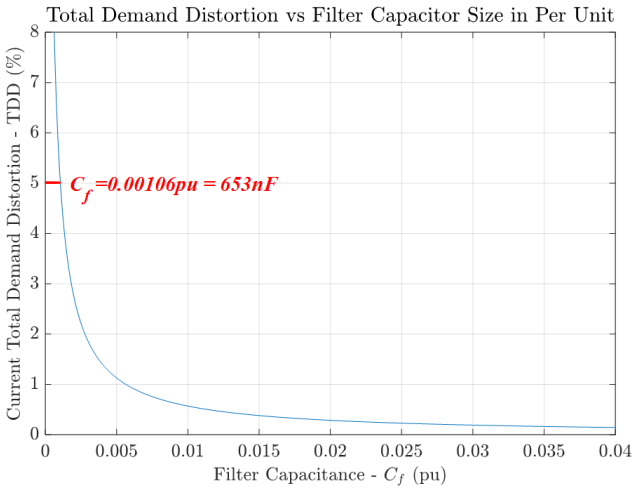
3.4.2 CL Value Limits Based on Filter Performance Parameters

Performing simple analysis on Fig. 3.19 results in the transfer function shown in (82). There are some important parameters that affect the frequency response that must be discussed. First, is the quality factor, Q, of the filter shown in (83). The quality factor is a quantifier of how damped the system is. For filters, a high value of Q implies that low-order harmonics can lay within the bandwidth of the resonant frequency range (to be discussed) [96]. On the contrary, low quality factor implies high power losses [96].

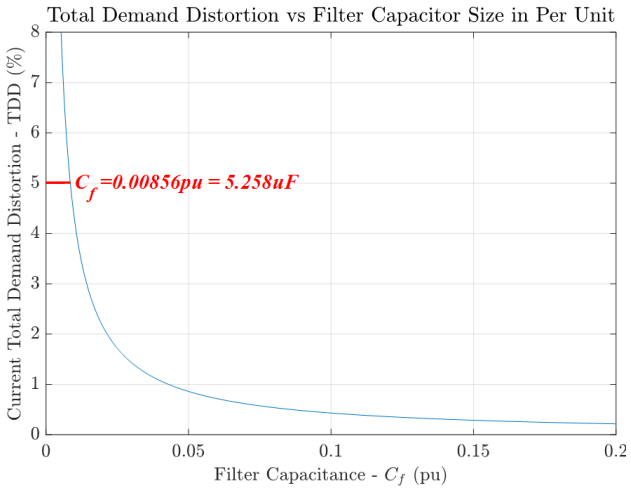
$$I_s(n) = \frac{1}{s^2 C_f L_f + s C_f R_d + 1} \times I_w(n) \tag{82}$$

$$Q = \frac{Z_o}{R} = \frac{\sqrt{\frac{L_f}{C_f}}}{R_d} \tag{83}$$

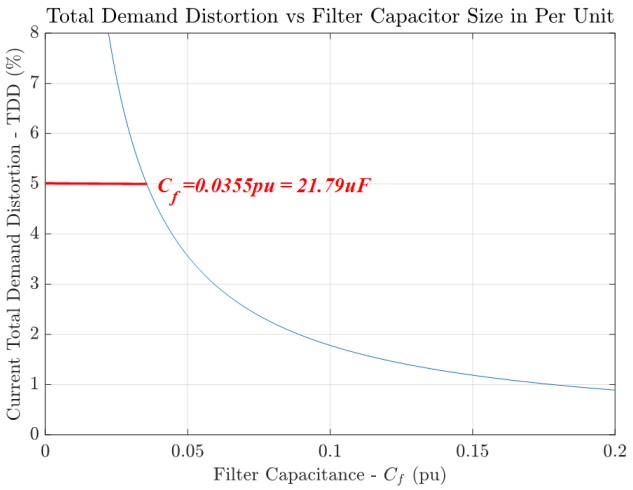
Continuing, the CL filter design procedure must consider the resonant frequency, f_{res} [67], [96], [97]. This is because if harmonics fall in the $f_{res.}$ region, said harmonics would see a gain [93]. As shown in (84), the location of f_{res} directly depends on the value of the filter capacitor and inductor. In literature, it is typical to design for the resonant frequency to appear around at least less than half of the sampling frequency value [97]. This is derived from the fact that dominant harmonics will appear centered around the sampling frequency. If the resonant frequency is much less than the sampling frequency, low magnitude harmonics will be in the resonant frequency bandwidth, and the gain will be insignificant. The effect of varying Q and f_{res} on the performance of the filter is shown in Fig. 3.23. In this image, it can be seen



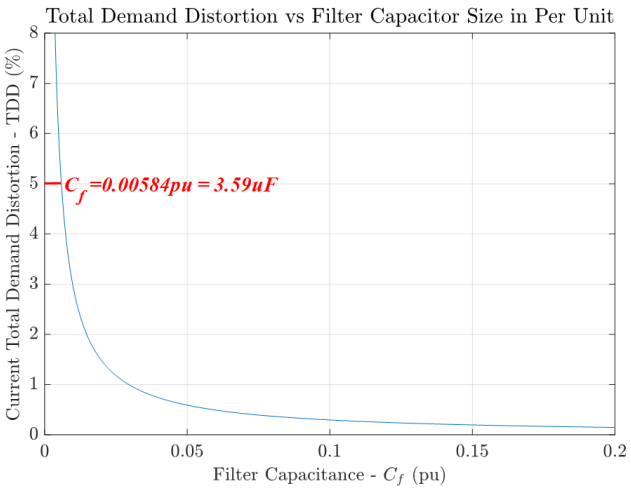
(a) SQ2.



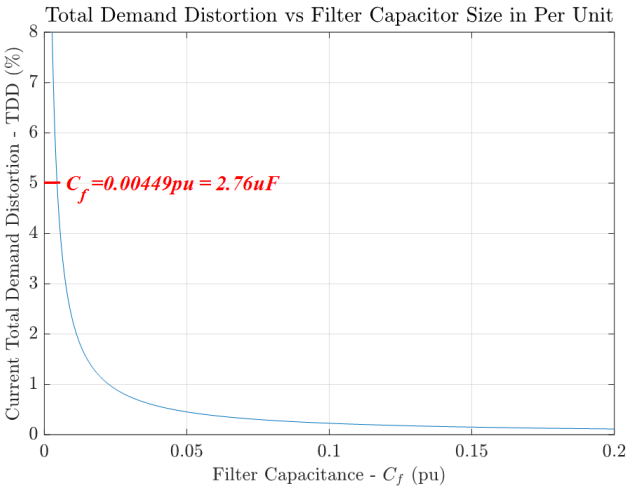
(b) SQ3.



(c) SQ4.



(d) SQ5.



(e) SQ6.

Figure 3.22: Filter capacitor design results for SQ2-SQ6 for f_{sw} ≈10 kHz.

that the location of the resonant frequency changes as L×C changes. As the quality factor decreases, the frequency response is more damped. Changing the quality factor can be done by changing the L/C ratio or the physical damping resistor. However, if the damping resistance is increased, the power losses of the filter increase. Practically, some value of damping resistance is required, for any analysis in this section, 0.1pu is selected as a reasonable value [67], [93]. It should be noted that for this particular filter configuration, a quality factor of 1 through 4 is recommended and have similar harmonic attenuation performance when f_{res} is less than or equal to 1/2 that of the sampling frequency [93], [96].

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{84}$$

$$Design\,Constraint : f_{res} \leq \frac{f_s}{2} \tag{85}$$

$$Design\,Constraint : 1 \leq Q \leq 4 \tag{86}$$

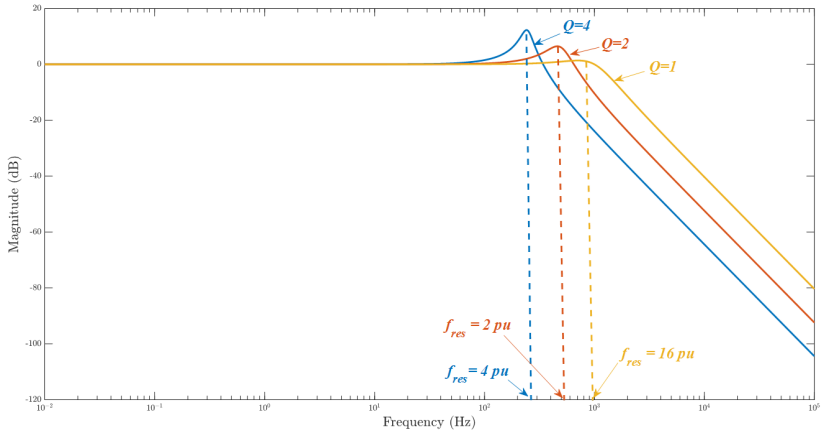
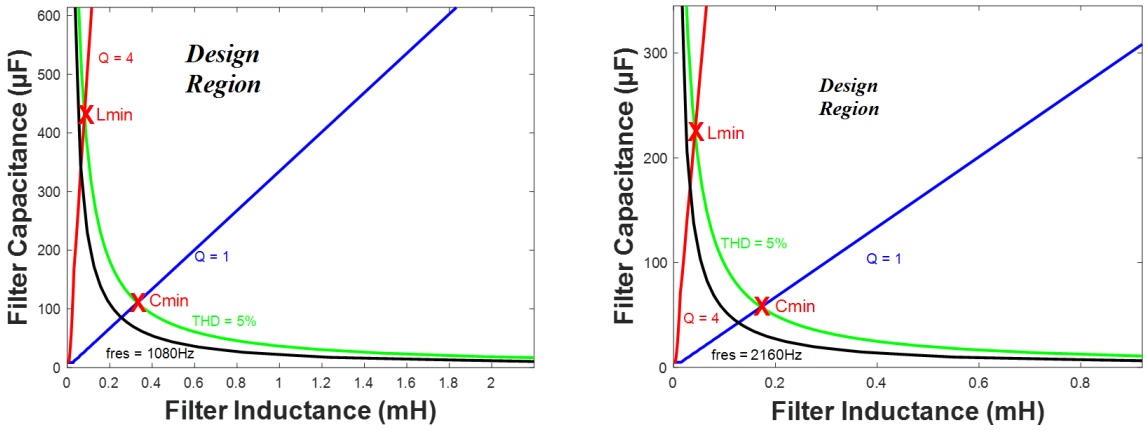


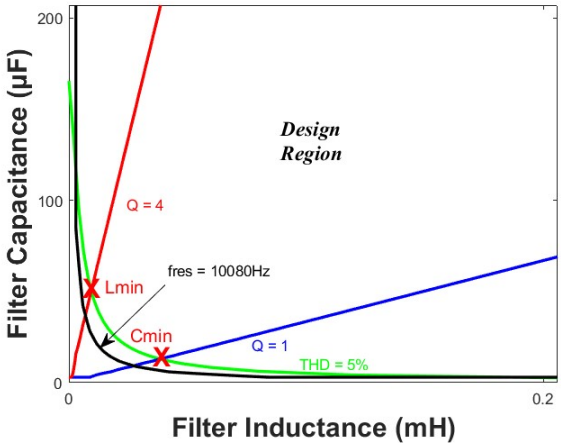
Figure 3.23: Frequency response of the filter configuration with three cases: Case 1: Q=4, L=0.1pu (blue), Case 2: Q=2, L=0.025, Case 3: Q=1, L=0.0063pu. C=0.6pu and Rd=0.1pu for all cases.

From the discussed design goals, the lower limits of the filter inductance and capacitance can be defined. Consider Fig. 3.24, the contours of the quality factor set to 1 and 4 are plotted along with the THD set to the IEEE 519 limitation and the resonant frequency set to 1/2 of the sampling frequency for various switching frequencies using SQ1 SVM are shown. The THD plot is created using the dominant harmonic assumption from the prior section. The quality factor contours are created using a damping resistance set to 0.1 pu. The results can help determine the minimum capacitance and inductance. This is done by finding the intersection point of the quality factor contours and the THD or resonant frequency contours (which ever one requires larger components). It should be noted that as the switching frequency increases, the THD and resonant frequency curves moves inward (toward the x and y-axis of the graph). This makes sense as smaller components will be required and the resonant frequency value is increasing also causing a decrease in component size. In all cases, the resonant frequency contour requires smaller components than the THD contour. As a result, the intersection points with the THD curves are used

and the 'design region' becomes the area enclosed by the quality factor curves and THD curve. Note, that the resonant frequency will be naturally met in this area because as the values of C_f and L_f increase, the resonant frequency is pushed to lower frequency, even further away from dominant harmonics. Fig. 3.25 shows the results when repeating the discussed procedure for each SVM sequence at a switching frequency of 10 kHz. The minimum inductance and capacitance values are summarized in Table 19. The performance from each sequence does not differ as drastically in the prior section because these are minimum values. If the minimum L is selected, the same trend derived in the previous section would show for the capacitance values for each respective sequence. It should also be noted that the minimum inductance and capacitance values are independent of each other, they cannot be used together as the required THD will not be met. They are simply the lower boundary derived from the design goals with the maximum value being as high as the designer would require (typ. L $<$ 0.6 pu, C $<$ 2.5 pu for low f_{sw} [5]).



(a) f_{sw} = 1080Hz. (b) f_{sw} = 2160Hz.



(c) f_{sw} = 10080Hz.

Figure 3.24: Contours for quality factor set to 1 and 4, resonant frequency set to 1/2 of the sampling frequency, and THD set to 5% using SQ1 SVM with various switching frequencies.

Table 18: Minimum filter capacitance and inductance based on f_{res}, Q, and THD contour results at various switching frequencies (SQ1 SVM).

f_{sw} ***(kHz)***	***1***	***2***	***5***	***10***	***20***	***40***	***80***	***100***
Min. L (μH)	80.79	43.15	18.38	9.51	4.72	2.41	1.72	0.952
Min. C (μF)	111.64	57.1	26.16	13.37	6.44	3.20	1.65	1.33

Table 19: Minimum capacitance and inductance for SQ1-SQ6 with f_{sw}=10 kHz.

	SQ1	SQ2	SQ3	SQ4	SQ5	SQ6
Min. L (μH)	9.51	8.86	8.78	10.57	7.26	8.59
Min. C (μF)	13.37	12.19	12.10	14.45	10.06	11.61

3.4.3 Filter Loss

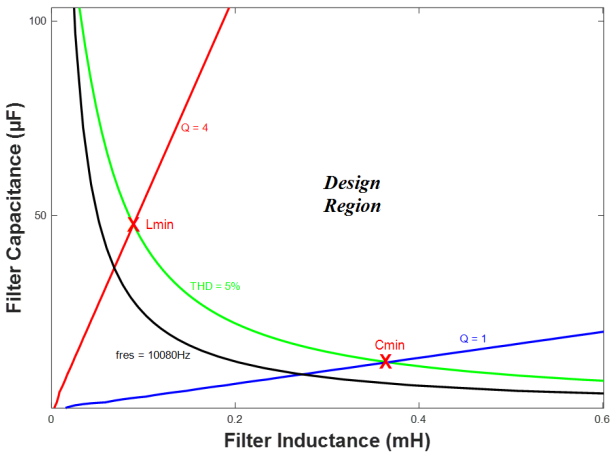
The purpose of this section is to discuss the mechanisms of loss in the filter components and show typical loss functions for the capacitor and inductor. To begin with, the mechanism of loss in the filter capacitor is the equivalent series resistance (ESR) [98], [99]. The simple formula is shown in (87). Here, i_c is the current through the filter capacitor, which can be expressed as the summation of the fundamental component and dominant harmonics from i_w covered in the previous section. The ESR is defined by (88), where $tan(\delta)$ is the loss tangent of the capacitor and Z_c is the impedance of the capacitor at the application's frequency [98]. To consider the power dissipated by individual harmonic components, (89) can be used [99]. However, based on the calculations provided in Table B1 in the Appendix, using (90) to estimate the loss is adequate. The case presented in the Appendix uses the worst case scenario, which is the maximum power point based on the graphs to be introduced (C_f = 390μF, ESR = 0.475Ω) at the lowest considered switching frequency (f_{sw} = 1080Hz). The results show that power dissipated due to harmonic content only accounts for 3.4% of the total power loss of the capacitor. Therefore, (90) is simply used to compute the power loss of the capacitor.

$$P_{loss,C_f} = i_c^2 \times ESR \tag{87}$$

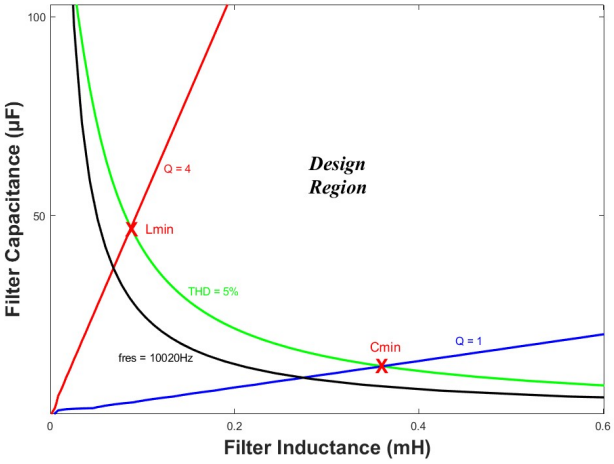
$$ESR = \frac{tan(\delta)}{|Z_c|} \tag{88}$$

$$\begin{aligned} P_{loss,C_f} = I_{c,1}^2 \times ESR + \frac{I_{c,m_f-13}^2}{2\pi \times C_f \times f_{m_f-13}} \times tan(\delta) + \frac{I_{c,m_f-11}^2}{2\pi \times C_f \times f_{m_f-11}} \times tan(\delta) \\ + \frac{I_{c,m_f-7}^2}{2\pi \times C_f \times f_{m_f-7}} \times tan(\delta) + \frac{I_{c,m_f-5}^2}{2\pi \times C_f \times f_{m_f-5}} \times tan(\delta) + ... \end{aligned} \tag{89}$$

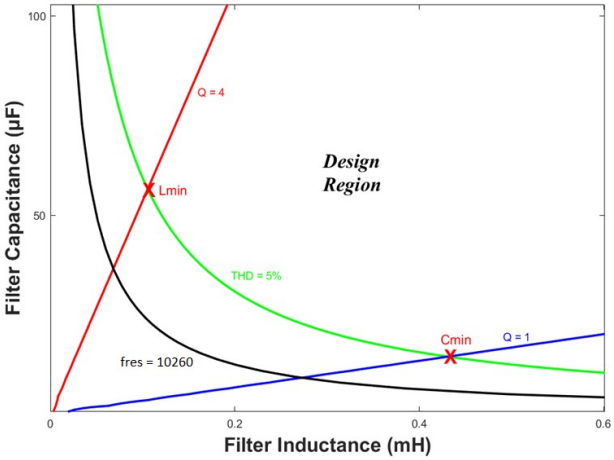
$$P_{loss,C_f} \approx I_{c,1}^2 \times ESR \tag{90}$$



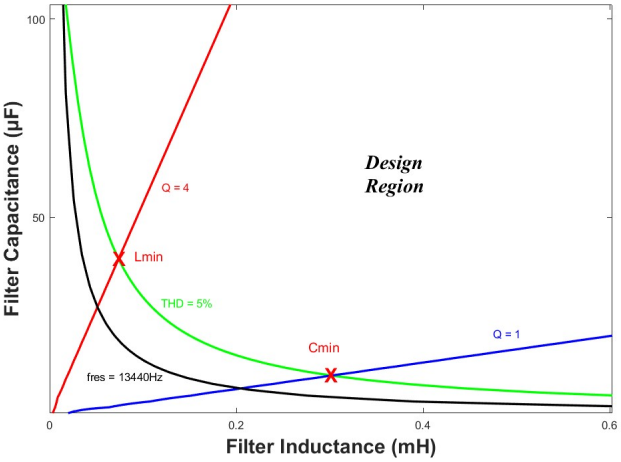
(a) SQ2.



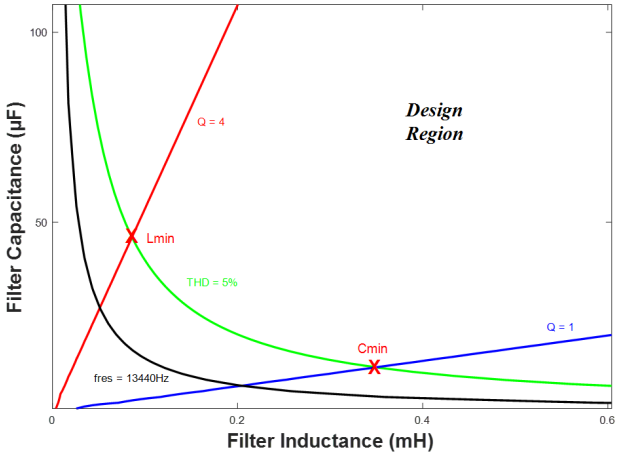
(b) SQ3.



(c) SQ4.



(d) SQ5.



(e) SQ6.

Figure 3.25: Contours for quality factor set to 1 and 4, resonant frequency set to 1/2 of the sampling frequency, and THD set to 5% using SQ2-SQ6 at f_{sw} = 10kHz. The minimum capacitor and inductor points indicated.

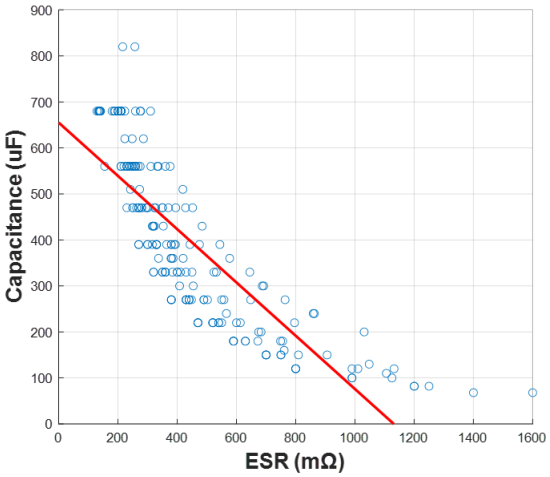
Next, the ESR value depends on many material level properties of the capacitors. Therefore, manufacturer data is used to derive an accurate selection. According to [100], ceramic (single and multi-

layer), film, and aluminum electrolytic capacitors are typically used in 100 V_{ac} range applications such as the one studied in this report. From this, manufacturer data can be used to develop typical ESR values to estimate the power loss of the filter capacitor. Fig. 3.26 (a)-(c) show scatter plots of ESR data taken from commercially available capacitors with voltage ratings of 120 V_{ac} to 400 V_{ac}. A line of best fit (red) is created to estimate the ESR based on the selected capacitor value. It should be mentioned that, generally speaking, electrolytic capacitors have a wider range of values when compared to film and ceramic. This fact is reinforced by the data presented in the figures below. The range of electrolytic capacitors considered is 2 μF to 655 μF. For film capacitors, the range of available capacitors is 1 μF to 70 μF and for ceramic capacitors, the range commercially available is 1 nF to 1 μF. For all capacitor technologies, there is an inverse relationship between capacitance and the ESR value (see (88)). This is a simple explanation as to why the the ESR values are larger for film and ceramic capacitors. One other thing that must be accounted for when computing the power loss is the variation of the fundamental capacitor current when varying the filter capacitance. Equation (91) is derived from the current division principle. Assuming the grid impedance, Z_{grid}, is constant with the damping resistance + line resistance set to 0.1 pu and the line inductance set to 0.1pu as well [67], the fundamental component of the capacitor current is provided in Fig. 3.27.

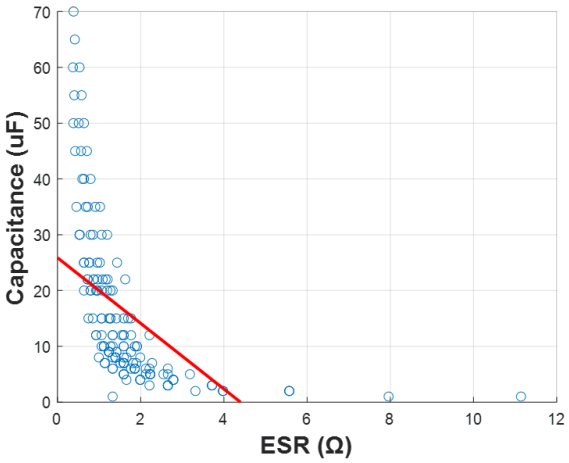
$$I_{c,1} = I_{w,1} \times \frac{Z_{grid}}{Z_{grid} + Z_{C_f}} = I_{w,1} \times \frac{R_g + jL_g}{R_g + jL_g + \frac{1}{\omega C_f}} \tag{91}$$

Finally, using the ESR data and capacitor current, Fig. 3.28 is crafted. These loss functions will assist in the power loss optimization process. Some notes on these functions, the ceramic capacitance essentially has negligible power losses, even though the ESR can be quite high. This is because the capacitor current in the considered capacitance region (1nF to 1μF) is very low (0-8mA). Similar arguments can be made for the other technologies as the ESR will decrease with increasing capacitance, and the fundamental capacitor current will increase with increasing capacitance.

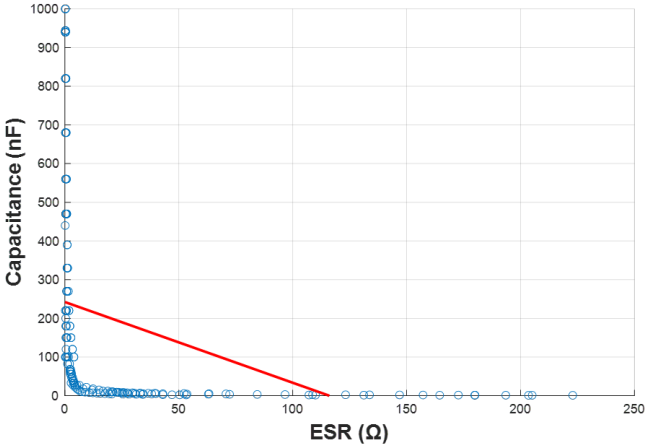
For the AC filter inductor, the core materials recommended by Micrometals include -26, -38, -40, -45, and -52 iron powder mixes [101]. Again, for this section, the Micrometals design tool will be relied upon to select the inductor and provide corresponding loss parameters. This is because there are many core and conductor shapes and sizes that can be considered. Although, for a 1mH, -26 iron powder core material, #15 AWG (based on full load current), 20 strand conductor, and 52cm mean length per turn (MLT) AC filter inductor, the process for selecting the inductor parameters is shown below. This is the design procedure details that the design tool will consider and use to compute the losses. First, the number of turns is derived based on the energy stored in the inductor [101]. The energy stored by the inductor can be computed using (92) [101]. Using the corresponding AC energy storage vs ampere turn curve for the selected core material provided in [101], the required number of turns can be computed. Based on the contours provided in the previous section, there is no need to increase the inductance larger



(a) Electrolytic capacitors ESR data from Vishay and Kemet (V_R = 120-400V_{ac}).



(b) Film capacitors ESR data from Vishay, Kemet, and TDK (V_R = 120-400V_{ac}).



(c) Ceramic capacitors ESR data from Vishay and Kemet(V_R = 120-400V_{ac}).

Figure 3.26: ESR line of best fit functions derived from commercially avaible products.

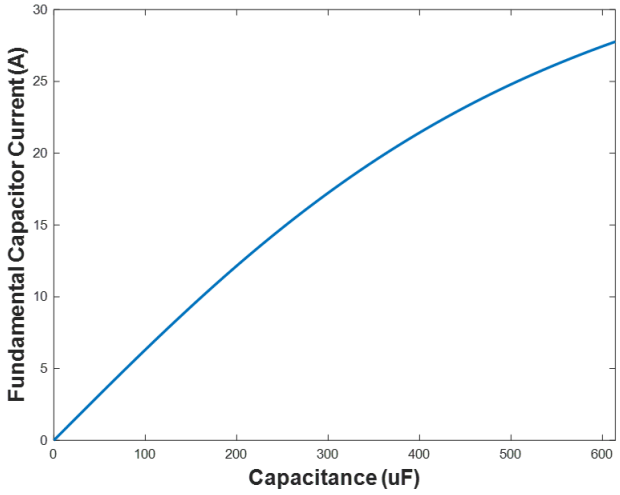
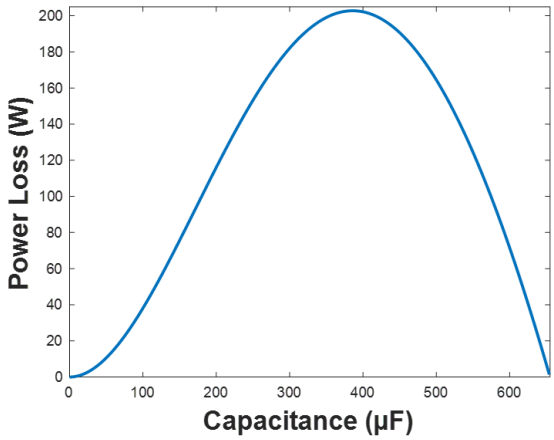
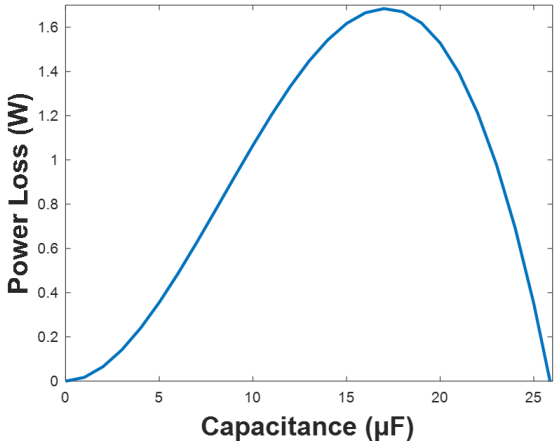


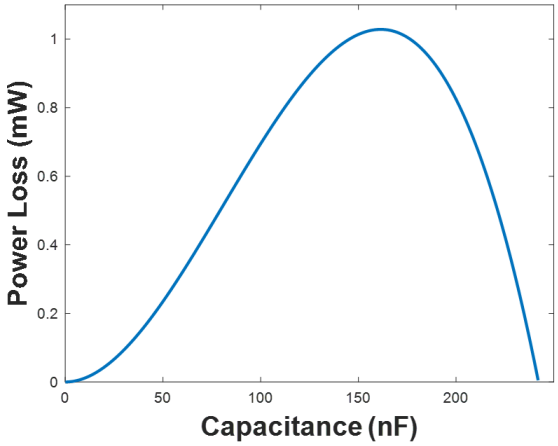
Figure 3.27: Effect of varying filter capacitance on the fundamental capacitor current.



(a) Electrolytic capacitor power loss function.



(b) Film capacitor power loss function.



(c) Ceramic capacitor power loss function.

Figure 3.28: Power loss functions of the various capacitor technologies.

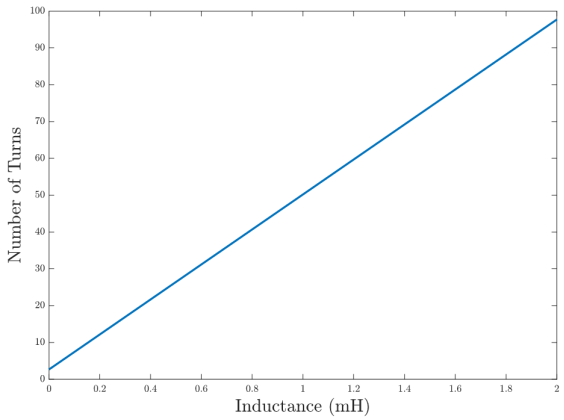
than 2mH. Hence, the considered region of inductance is 0-2mH. The required number of turns is provided in Fig. 3.29 (a). From this value the winding loss can be computed using (62)-(64), where the number of conductor strands should be considered in (62). The results of the winding loss are shown in Fig. 3.29 (b).

$$E = \frac{1}{2} \times L \times I_{RMS}^2 \tag{92}$$

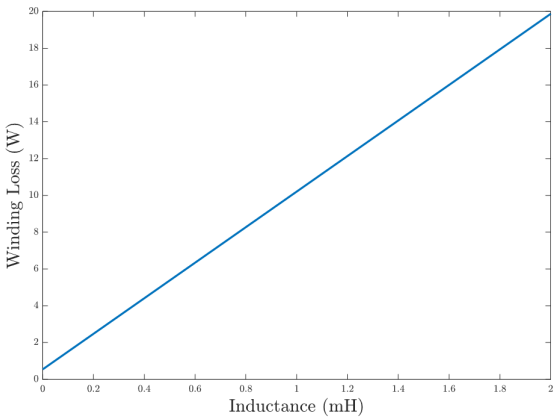
Fig. 3.29 (c) shows the core loss of the inductor for toroidal shaped core with an effective area of $6.85cm^2$ and effective length of $25cm$. The magnetizing force in Oe is computed using (93). From this (72) can be used to estimate the peak AC flux density and the result can be inputted into the core loss function in (58) (the same as the DC-link inductor studied earlier). The total loss of the AC inductor is shown in Fig. 3.29 (d). It should be noted again that the number of turns is proportional to the inductor value and as a result, so is the winding loss provided that other parameters such as the wire gauge and MLT remain constant. The core loss also increases with inductance but the curve is non-linear due to

the core properties. Please note, this curve will vary depending on the selected core.

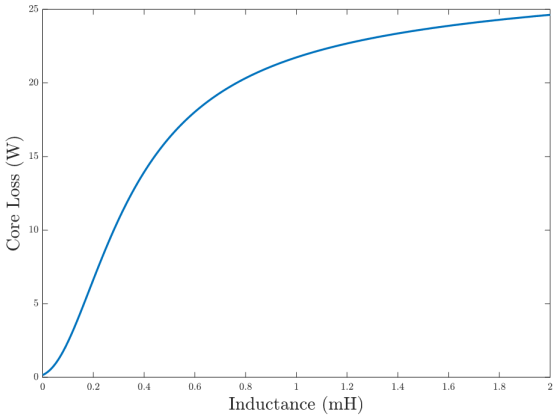
$$H = 0.4 \times \pi \times \frac{N}{l_e}(I_{peak}) \tag{93}$$



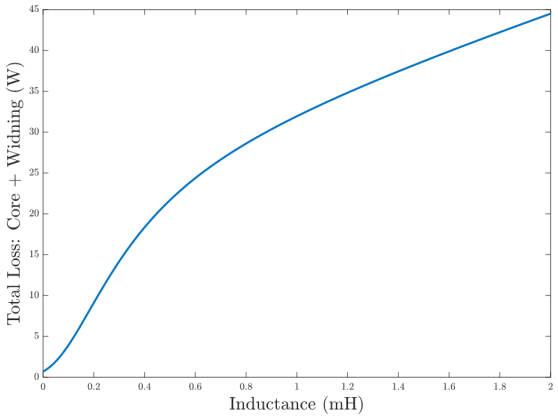
(a) Required number of turns for the inductor value.



(b) Winding loss of the inductor.



(c) Core loss of the torodial core using -26 iron powder material.



(d) Total power loss of the inductor.

Figure 3.29: Typical AC filter inductor loss profile.

3.4.4 Selection of Filter Values

Based on the loss functions discussed in the previous section, optimizing the filter loss comes down to minimizing the filter inductor first. This is because the winding loss is proportional to inductance and there is a degree of freedom in the capacitance selection. If the capacitance is low enough to use film or ceramic capacitors, any value in the previously analyzed ranges is sufficient in terms of loss. However, if the capacitance is required to be large (in the range of analyzed electrolytic capacitors), avoiding the loss region between 180 μF to 575 μF is beneficial. This is because power dissipation of the capacitor alone will exceed 1% of the rated power, when it is recommended that the entire filter network does dissipate more than 1% of the rated power [96]. When selecting the minimum inductance value, the capacitance

(designed using the procedure in section 3.4.1) lands in the high loss region of the electrolytic capacitor power loss function. Therefore, to minimize power loss, the minimum capacitance value is selected and the corresponding inductance value is selected. Note, this value can be read from the contour figures or designed in a similar fashion to Fig. 3.21 and Fig. 3.22, both yield the same results. From there, the inductor that generates the least amount of loss from the Micrometal's design tool is selected. It can be noted that this results in a quality factor of 4, backing the point stated earlier that the higher Q corresponds to lower losses. To further expand on this point we can observe the results at the highest switching frequency (100080 Hz). If the minimum inductor size is selected, that is 0.952 μH, the resulting capacitor size is 6.75 μF. From the loss function, this results in a film capacitor with 0.46 W of loss. From the Mircometal's design tool, the minimum loss is 0.065 W. Considering these values, the total loss is 1.575 W compared to the selected values in Table 20 that result in 0.924 W. Repeating the same procedure for 80 kHz switching frequency shows that a 5.93 μF capacitor producing 0.38 W of loss and a 1.72 μH inductor producing 0.196 W of power loss is required for a quality factor of 1. The total loss is 1.73 W compared to 1.43 W using a Q of 4. This trend is constant across all switching frequencies. At lower switching frequencies, the capacitor will be large when L is minimized, resulting in high loss electrolytic capacitors. At higher switching frequencies, the inductor losses do not improve by a significant margin when selecting the minimum value while minimizing C results in lower losses. This is why one reason why the procedure for the 1 kHz switching frequency case. It also differs because individual harmonics must be considered. If the minimum value of C is used, the resulting inductor is large and therefore, lossy. Specifically, for $C_f = 111.64$ μF, the required inductance to meet grid codes is 4.3 mH. To compensate, the capacitance is set to 1 pu, where the loss of the capacitor will be quite low based on the power loss function, and the corresponding inductance is selected. The resulting inductor value is 785 μH, which will be much less lossy than the 4.3 mH inductor. The resulting quality factor and resonant frequency is 2.62 and 229.2 Hz, which fall in the desired design region. Table 20 shows the selected filter values, their losses, and performance indicators for each switching frequency to be considered in Chapter 4 when using SQ1 SVM. Table 21 shows the resulting filter components and loss parameters when varying the SVM sequences with fixed switching frequency (10 kHz) and following the same procedure highlighted earlier in the paragraph. Since, the switching frequency is high, there is little variation in performance and loss as seen. If they were ranked on component loss and size it would be SQ5 in first, SQ6 in second, SQ3 and 4 tied for third, SQ1 in fifth, and SQ4 is last. One final thing to note is the decreasing volume of the filter capacitor as the switching frequency increases.

Table 20: Selected filter capacitance and inductance with additional loss and performance values for varying switching frequency using SQ1 SVM.

f_{sw}	***1***	***2***	***5***	***10***	***20***	***40***	***80***	***100***
Filter Inductor Parameters								
L_f ***(μH)***	785	173	76.4	38.98	19.33	9.85	4.895	2.72
Core Loss (W)	2.43	0.6048	0.4372	0.1495	0.0632	0.0458	0.0244	0.01904
Winding Loss (W)	6.18	1.697	1.385	0.982	0.777	0.581	0.361	0.288
Weight (g)	1870	555	318	168	82.9	62.2	62.2	60.3
Filter Capacitor Parameters								
C ***(μF)***	614.01	57.1	26.16	13.37	6.44	3.20	1.65	1.33
ESR Loss (W)	53.96	6.98	1.76	1.28	0.46	0.14	0.091	0.009
Cap. Technology	Electrolytic	Film	Film	Film	Film	Film	Film	Ceramic
Volume (cm^3)	192.42	125.64	77.63	33.18	24.57	10.81	8.47	0.00195
CL Filter Parameters								
Quality Factor, Q	2.62	4	4	4	4	4	4	4
f_{res} ***(Hz)***	229.2	1601.3	3557.3	6963.8	14253.6	28348.3	56001.8	83677.7
Total Loss (W)	187.71	27.86	10.76	7.24	3.89	2.29	1.43	0.924

Table 21: Selected filter capacitance and inductance with additional loss and performance values for varying SVM sequence at f_{sw}=10 kHz.

Sequence	***1***	***2***	***3***	***4***	***5***	***6***
Filter Inductor Parameters						
L_f ***(μH)***	38.98	36.33	36.08	43.11	29.76	35.29
Core Loss (W)	0.1495	0.1492	0.1492	0.1621	0.1012	0.1492
Winding Loss (W)	0.982	0.899	0.899	1.183	0.9048	1.0482
Weight (g)	168	294	294	298	249	294
Filter Capacitor Parameters						
C ***(μF)***	13.37	12.19	12.10	14.45	10.06	11.61
ESR Loss (W)	1.28	1.297	1.297	1.455	1.098	1.297
Cap. Technology	Film	Film	Film	Film	Film	Film
Volume (cm^3)	33.18	33.26	33.26	41.5	33.18	33.18
CL Filter Parameters						
Quality Factor, Q	4	4	4	4	4	4
f_{res} ***(Hz)***	6963.8	7562.9	7617.2	6376.7	9178.5	7865.1
Total Loss (W)	7.24	7.04	7.04	8.40	6.31	7.04

3.5 Summary

Section 3.1 CSI Rating + Sources of Loss

- The 10kW CSI ratings considered in this report are provided in Table 7.

Section 3.2 Semiconductors

- The semiconductor voltage and current ratings were derived and the selected devices considered throughout the report are provided in Table 8.
- Equations for the conduction loss for each device were discussed and the duty cycle of the switch using SVM is determined to be fixed at 1/3, independent of the switching frequency or modulation index.

- The switching loss is discussed for each technology and equations to compute the loss are proposed based on dominant switching loss SVM sectors. This resulted in Equations (26)-(36).
- A method to compute the switching loss for Si MOSFETs based on the capacitance was discussed.

Section 3.3 DC-Link Inductor

- Section 3.3.1 computes the required DC-link inductance for 12% ripple current when using SQ1 SVM for f_{sw} varying between 1kHz to 100kHz. The results with corresponding losses provided by the Micrometal's design tool are found in Table 9. Of course the DC-link inductor value decreases proportionally to the switching frequency.
- Section 3.3.2 verifies the losses in Table 9 by using theoretical equations, the relative error is low for DC winding loss. The error is higher for core losses due to the different methods of computations. Micrometal's values are used because it uses 'worst case scenario' values.
- Section 3.3.3 repeated the analysis done in 3.3.1 for each SVM SQ2-6. The required DC-link inductance for each sequence was derived at a few different switching frequencies. An equation to compute the required inductance for each case is presented. The results for the DC-link inductor size and related losses are provided in Table 12 to be used in Chapter 4. The results showed that SQ2 produces the smallest required inductance followed by SQ1, SQ4, SQ6, SQ3, and SQ5.

Section 3.4 CL Filter

- Section 3.4.1 showed how the required filter capacitance is computed based on IEEE-519 2014. The required capacitance when using SQ1 SVM for switching frequencies 1-100kHz are shown with the filter inductance fixed at 0.1pu. A method for generalizing the harmonic content of the PWM current at different frequencies was shown and compared to the capacitor size required when using the simulation results for the harmonic spectrum. Generally, the approximation slightly over-sized the capacitor but this was deemed acceptable. Results of filter capacitor sizing for different SVM sequences were compared with L_f=0.1pu resulting in SQ1 with the lowest followed by SQ2, SQ6, SQ5, SQ3, and SQ4.
- Section 3.4.4 showed the method behind the selection of filter components and their losses based on the required filter performance and the loss functions discussed in previous sections. Tables 20 and 21 summarized the results will be used in Chapter 4.

4 Simulation Results

This section presents the simulation results for the PSIM thermal module simulations under various conditions. The following sentences will discuss some assumptions that the simulation model makes.

First, the switching loss of the SiC SBD and GaN reverse conduction channel are neglected. This is because the SBD is a majority carrier device, meaning there are no minority carriers that must discharge during switching transients [15], [20]. Here, the switching loss is caused by output capacitance of the device, which is low. For the GaN device, there is no body diode as discussed. Therefore, the switching loss is also a product of the output capacitance, which is quite low for GaN devices [42]. The second assumption is that the datasheet values are accurate to the actual performance of the device. This means that there is no manufacturing error modelled. Finally, energy curves at different junction temperatures are derived by assuming a linear relationship between the energy at a given current and energy at the same current but different junction temperature [68]. This relationship is described by (94). To reiterate other assumptions made throughout the design of the passive components includes ideal inductor and capacitor values (no fluctuations or manufacturer error) and any induced phase angle by the filter is minimal and can be corrected with control. The ambient temperature is set to 125°C for all simulations and calculations in section 4.1, 4.2, and 4.4. For section 4.3, the ambient temperature is varied to see the effect of temperature on the performance of each configuration. The t_d value for all simulations involving case E is set to 60 ns based on the switching time characteristics of the C3M0025065K. Specifically, it is the summation of the delay and turn on/off times. This is the minimum value (best case scenario) and allows for the completion of the turn on and turn off process of respective switching states in order to achieve RB. The gate driver voltage for all configurations is 15/0 V, except for the GaN device that uses 6/0 V. The gate resistance for all cases is set to 2.5 Ω. The selected semiconductors are re-shown in Table 22 and the considered switching cells presented in Chapter 2 are showcased again for reader convenience. This can be seen in Fig. 4.1. The CSI rating is provided in Table 7.

$$E_{on/off}vsI(T_{j,2}) = \frac{E_{on/off}(I_1, T_{j,1})}{E_{on/off}(I_1, T_{j,2})} \times E_{on/off}vsI(T_{j,1}) \tag{94}$$

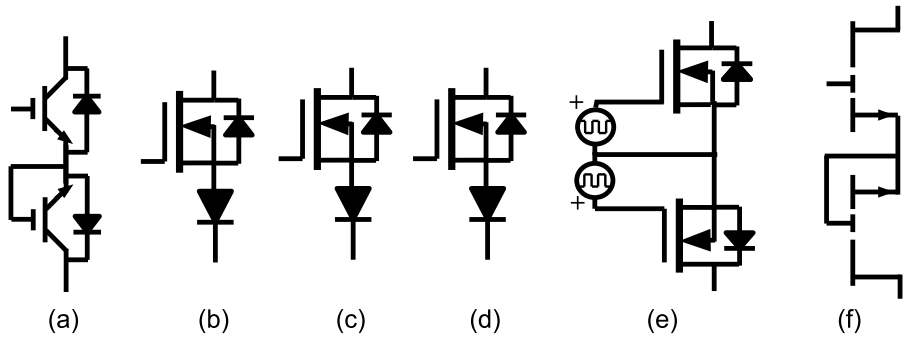


Figure 4.1: Studied switch configurations: a) Case A: IGBT switch in series with IGBT body diode, b) Case B: Si MOSFET in series with discrete Si diode, c) Case C: SiC MOSFET in series with Si diode, d) Case D: SiC MOSFET in series with SiC SBD, e) Case E: Dual SiC switch, and f) Case F: Anti-series GaN solution.

Table 22: Selected semiconductor components for each configuration with gate driver parameters.

Semiconductors		
Part Type	***Manufacturer/Part Number***	***Gate Driver Parameters***
Case A: IGBT	Infineon/IKW3065ES5	$R_G = 2.5\Omega$, $V_{GE} = 15/0V$
Case B: Si MOSFET	STMictoelectronics/STY112N65M5	$R_G = 2.5\Omega$, $V_{GS} = 15/0V$
Case B & C: Si Diode	Rohm/RFS60TZ6S	-
Case C, D, E, & F: SiC MOSFET	Cree/C3M0025065K	$R_G = 2.5\Omega$, $V_{GS} = 15/0V$
Case D: SiC Schottky Diode	OnSemi/FFSH5065A	-
Case F: GaN MOSFET	GaN Systems/GS66516	$R_G = 2.5\Omega$, $V_{GS}6/0V$

4.1 Efficiency vs Switching Frequency

4.1.1 Semiconductor Losses

This section studies the loss of each case, A-F with varying switching frequency from 1kHz to 100kHz considering only the semiconductor losses under full load conditions. SQ1 SVM is used, however, since the switch duty cycle is fixed for all SVM sequences, the same semiconductor loss results would be expected for any sequence. The goals are to study and compare the loss distribution of each switch configuration. Key observations on each technology are made. First, the simulation results are presented in Fig. 4.2. Here the orange portion represents the conduction loss of the RB device (lower device) for each switch configuration. The blue portion represents the conduction loss of the upper switch and the yellow portion shows the switching loss of the upper device. The purple section accounts for a small portion of the loss but is the reverse recovery loss or switching loss of the lower device depending on the switch configuration.

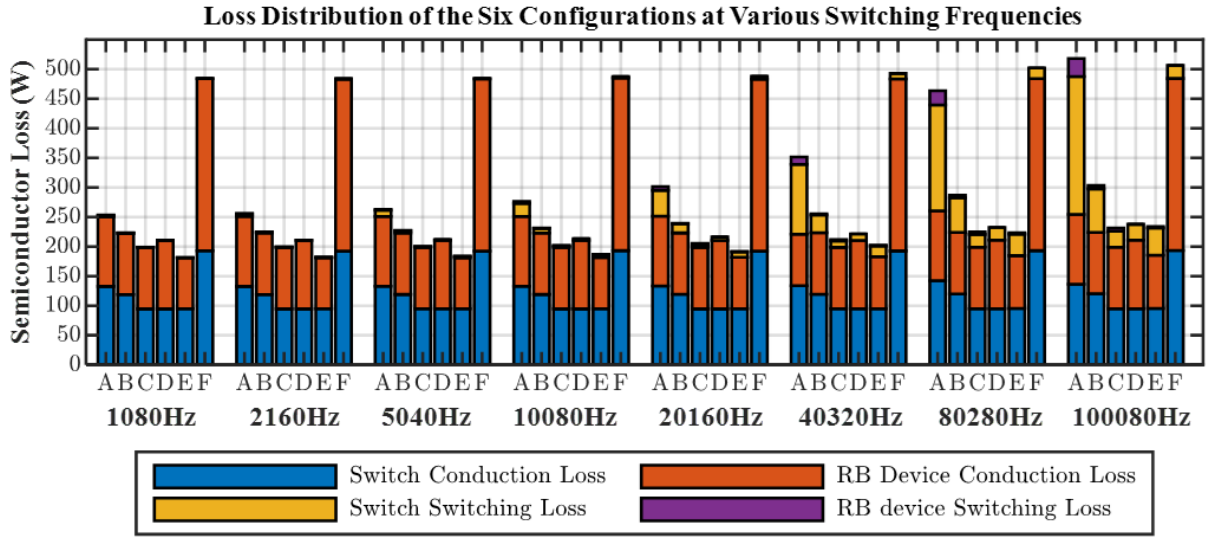


Figure 4.2: Loss distribution for each switch configuration at various switching frequencies ($T_j = 125°C$).

Starting with the analysis of the conduction loss produced by each configuration, the upper switches, i.e., the IGBT (case A), Si (case B), SiC (case C, D, and E), and GaN (case F) device produce 22.1 W,

19.85 W, 15.76 W, and 32.1 W of conduction loss per switch, respectively. These values are reflected in Table 23. Comparing the SiC MOSFET and Si MOSFET shows a 20.6% reduction due to the decrease of on-state resistance at the same operating conditions. That is, from 38.7mΩ for the Si device to 30.75 mΩ for the SiC MOSFET. When replacing the IGBT with the SiC MOSFET, a 28.7% reduction in the conduction loss is seen. On the other hand, the GaN device has the worst conduction loss performance due to high on-state resistance at the operating temperature. At high temperatures, the on-state resistance of the GaN-HEMT is 65.6 $m\Omega$, which is more than 2 times that of the SiC MOSFET studied. On the contrary, at room temperature it is 25 $m\Omega$, which is very comparable to the SiC MOSFET. This shows one flaw of the GaN device, its on-state resistance is very sensitive to increasing temperature. When considering all six switches, the conduction loss of the upper switch for case A accounts for 132.6 W, for case B, 119.1 W, for case C, D, and E, 94.56 W, and for case F, 192.6 W. This is shown in Fig. 4.3. Note that the conduction loss for all upper switches are not frequency dependent, so this figure shows the results for all considered switching frequencies. Overall, the SiC MOSFET provides the best conduction loss performance.

Table 23: Conduction loss of the upper switch devices (per switch).

Configuration	***Conduction Loss Per Switch (W)***
Case A: IGBT	22.1
Case B: Si MOSFET	19.85
Case C,D,E: SiC MOSFET	15.76
Case F: GaN-HEMT	32.1

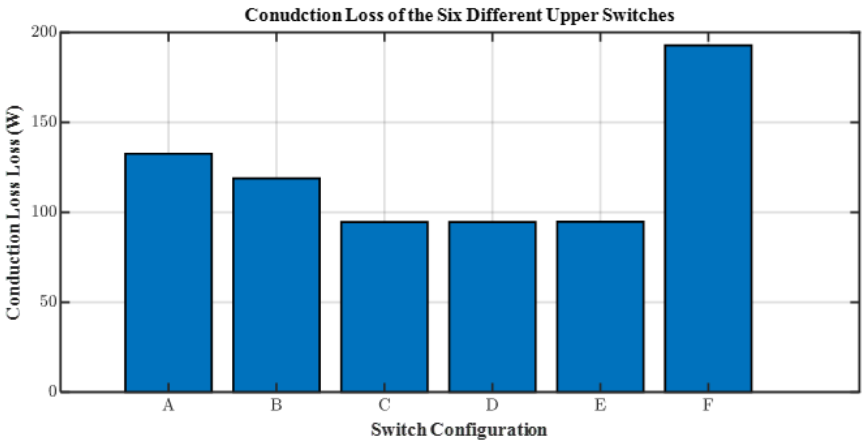


Figure 4.3: Conduction loss of the upper switch considering all six switches ($T_j = 125^{\circ}$C) (extracted from Fig. 4.2).

For the RB devices, i.e. the IGBT body diode, Si diode, SiC SBD, lower SiC switch in Case E, and the GaN reverse channel produce 19.7 W, 17.3 W, 19.3 W, 14.4 W (at $f_{sw} = 1080$ Hz), and 64.8 W of conduction loss per switch respectively. As seen, Case E offers the best conduction loss performance

but at the cost of an additional gate driver. It is worth noting that the conduction loss for Case E's lower switch is actually frequency dependent as discussed in Chapter 3. This is because the body diode conducts during turn-on transients and the reverse conduction channel conducts during steady state. Since the body diode conducts during every switch transition, the conduction loss of the body diode increases by a factor equal to that of the increase in switching frequency. The different mediums have different loss parameters. The C3M0025065K body diode introduces a 4 V drop but the duty cycle is low, keeping the conduction loss low (10.85 mW). On the other hand, the 3rd quadrant voltage drop of the device is 1.1 V at the same operating conditions, and will handle the current for a large majority of the conduction period. This value of forward voltage is lower than any device used in this study and hence, explaining the reduction in conduction loss. To remind the reader, the delay time, t_d (discussed in Chapter 2.3.4) is set to 60 ns. Reducing the delay time will further reduce the conduction loss as per (20) and (21). However, decreasing this value can result in the destruction of the inverter. This is because insufficient time is provided for the other SVM state switch to fully turn on leaving no RB. Therefore, the time delay parameter is a trade off between higher conduction loss and the destruction of the inverter. When comparing Case E to the IGBT body diode and Si diode, a 27% and 17% reduction in loss is seen. It is important to note that the SiC SBD does not provide significant improvement when compared to the IGBT body diode and actually increases the conduction loss due to a higher forward voltage drop compared to the Si diode by 11.4%. For more information regarding this, one should refer back to Chapter 1.3. Again, the GaN device's reverse conduction channel produces the highest forward voltage (around 5 V) and in turn, the highest amount of conduction loss at 48.5 W. It should be noted that even at room temperature the GaN device produces a high forward voltage drop with a nominal value of 2.9 V. It is recommended to use the reverse conduction channel in low duty cycle applications to keep conduction loss at a more reasonable value. The loss findings for each switch are summarized in Table 24 and Fig. 4.4. For the lower switch solutions, the SiC MOSFET was the best preformer while GaN was the worst in terms of conduction loss.

Table 24: Conduction loss of the RB device in each configuration (per switch).

Configuration	***Conduction Loss Per Switch (W)***
Case A: IGBT Body Diode	19.69
Case B, C: Si Diode	17.33
Case D: SiC SBD	19.31
Case E: SiC MOSFET 3^{rd} Quadrant + Body Diode (at f_{sw}=1080 Hz)	14.36 + 10.85m
Case E: SiC MOSFET 3^{rd} Quadrant + Body Diode (at f_{sw}=10080 Hz)	14.13 + 0.891
Case F: GaN Reverse	48.5

Moving onto the switching loss, the results at f_{sw} = 10080 Hz per switch are shown clearly in Fig.

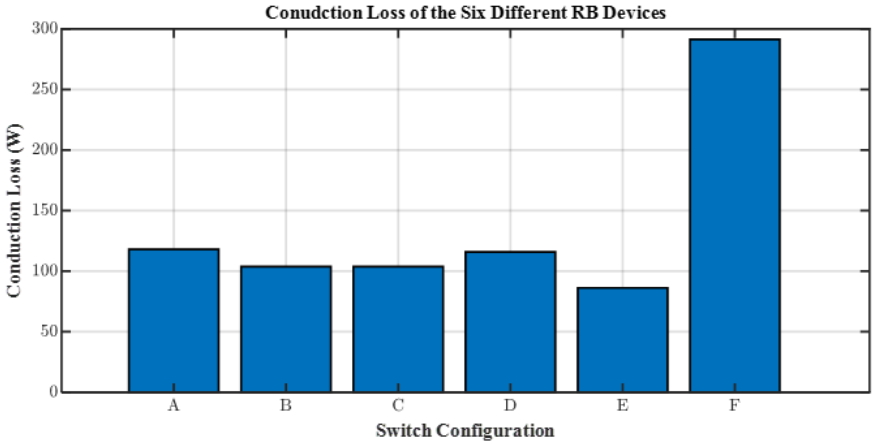


Figure 4.4: Conduction loss of the RB device in each switch configuration considering all six switches ($T_j = 125°C$) (extracted from Fig. 4.2).

4.5. Case A-F produce 4.21 W, 1.38 W, 0.578 W, 0.48 W, 0.837 W, and 0.405 W respectively, see Table 25 for clarity. The SiC MOSFET (Case C) provides an 86% and 58% switching loss reduction when compared to Case A and B accordingly. Comparing Case C to D, the effect of replacing the Si diode with SiC SBD can be seen. The result is a 17% reduction in the switching loss. This is negligible due to the CSI's inherently low switching loss and since the switching loss of a single switch configuration is in the mW range. Case E sees an increase in switching loss when compared to case C and D due to increased reverse recovery loss in the SiC MOSFET body diode than the SiC SBD and Si diode. Implementing the GaN device provides the lowest switching loss amongst all configurations. It introduces an additional 15.6% reduction in switching loss when comparing to the SiC case. The switching loss percentage relative to the semiconductor loss for configuration A-F grows from 1%-51%, 0.33%-26.1%, 0.18%-14%, 0.14%-11.34%, 0.33%-21%, and 0.05%-4.37% respectively when increasing the switching frequency from 1 kHz to 100 kHz. This trend is shown in figures 4.6-4.11. Of course, these figures will show that conduction loss is the dominant loss in the semiconductors. However, they are shown to see how the switching loss increases for each technology.

Table 25: Switching loss of the switch configurations in cases A-F (per switch).

Configuration	***Switching Loss Per Switch (W)***
Case A: IGBT + IGBT Body Diode	4.21
Case B: Si MOSFET + Si Diode	1.38
Case C: SiC MOSFET + Si Diode	0.578
Case D: SiC MOSFET + SiC SBD	0.48
Case E: Dual SiC MOSFET	0.837
Case F: GaN Solution	0.405

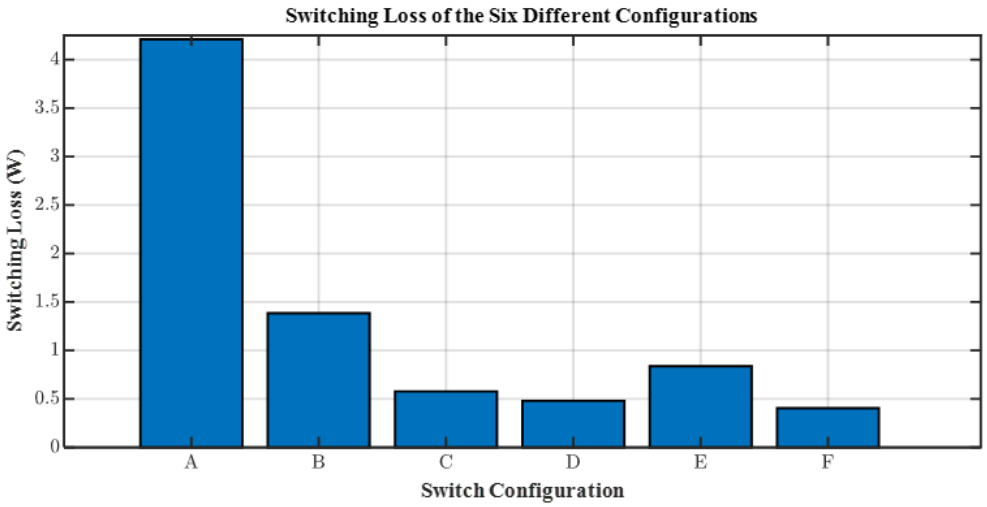
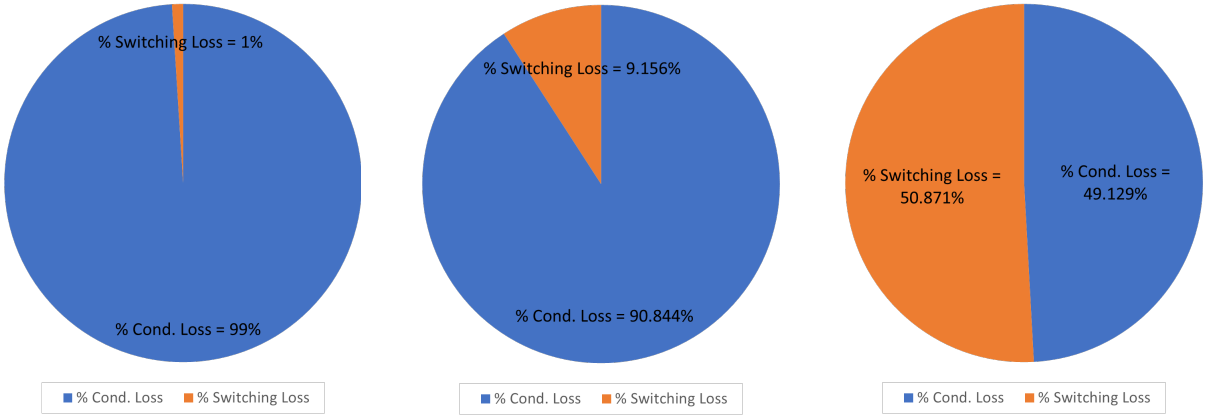


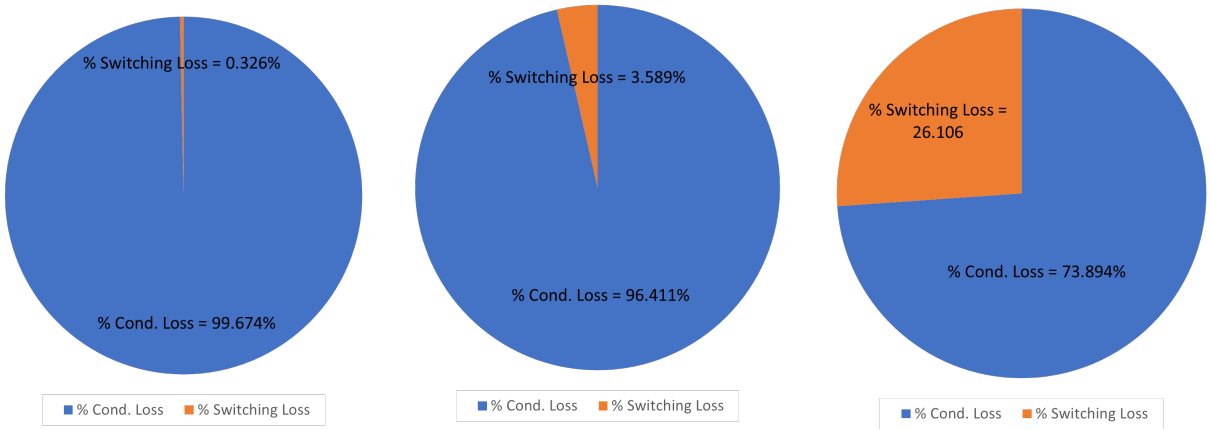
Figure 4.5: Switching loss of each switch configuration (upper + lower device) considering one switch ($T_j = 125°C$) (extracted from Fig. 4.2).



(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

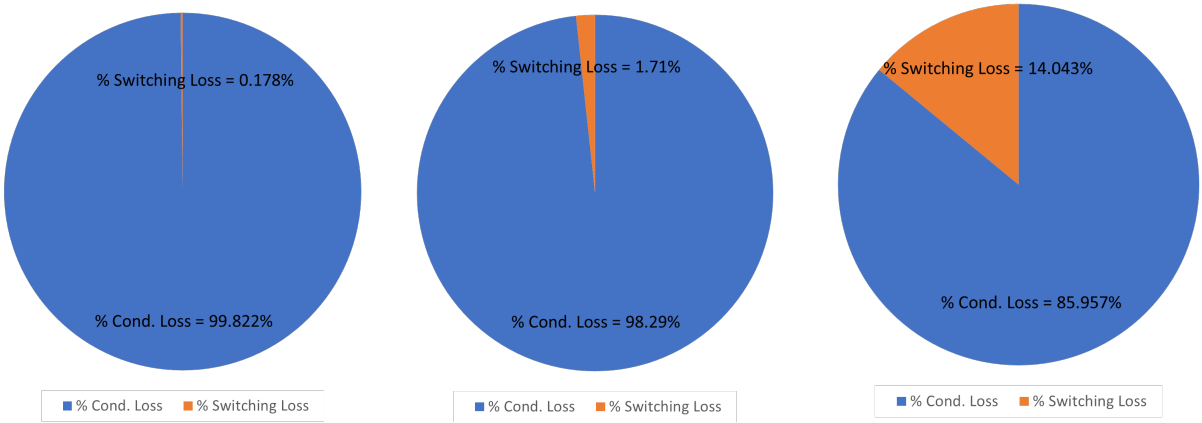
Figure 4.6: Percentage breakdown of the semiconductor loss at various switching frequencies for case A: IGBT + IGBT body diode.

The efficiency of the CSI considering only the semiconductor losses, coined the 'Semiconductor Efficiency' plotted versus switching frequency is shown in Fig. 4.12. Some notes can be made off of these results. Of course, each switch configuration's maximum efficiency will occur at the lowest switching frequency. The respective peak efficiency values are shown in Table 26 and discussed throughout this paragraph. The IGBT solution's maximum efficiency is 97.45% and sees the largest roll off with increasing switching frequency due to the device parameters discussed earlier. Using the power loss versus switching frequency curve shown in Fig. 4.13, the 'loss slope' in W/Hz (Watts per Hertz) of each switch cell can be defined. This will define the expected power loss increase with the increase in switching frequency over the entire range considered. For the IGBT case it is 2.674 mW/Hz. For case B, the maximum efficiency is 97.765% and the loss slope is 0.8064 mW/Hz, less than one third that of the IGBT due to the superior switching loss performance of MOSFET over IGBT. For case C, the maximum efficiency is 98.01% and the loss slope is 0.3278 mW/Hz. As discussed, the improvement in efficiency when comparing case C



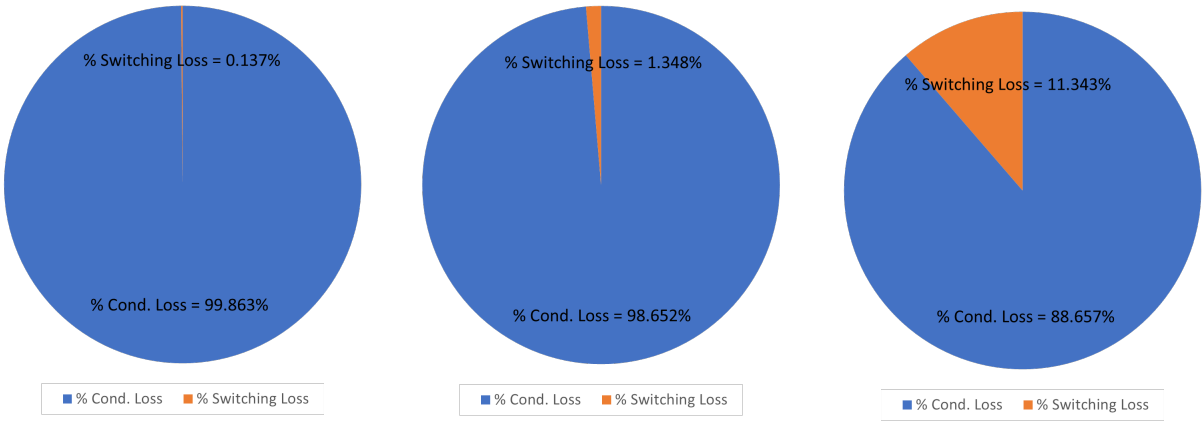
(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

Figure 4.7: Percentage breakdown of the semiconductor loss at various switching frequencies for case B: Si MOSFET + Si diode.



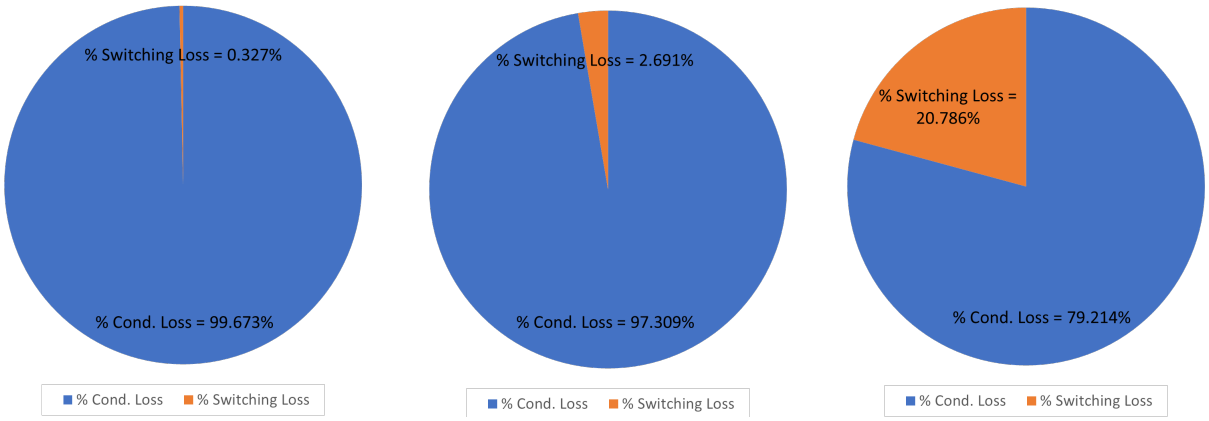
(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

Figure 4.8: Percentage breakdown of the semiconductor loss at various switching frequencies for case C: SiC MOSFET + Si diode.



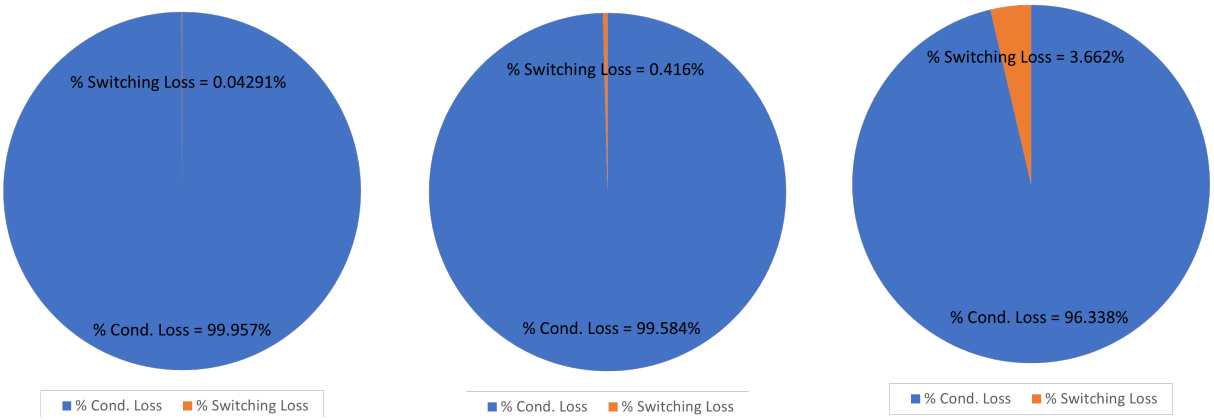
(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

Figure 4.9: Percentage breakdown of the semiconductor loss at various switching frequencies for case D: SiC MOSFET + SBD.



(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

Figure 4.10: Percentage breakdown of the semiconductor loss at various switching frequencies for case E: Dual SiC MOSFET.



(a) f_{sw}=1080Hz. (b) f_{sw}=10080Hz. (c) f_{sw}=100080Hz.

Figure 4.11: Percentage breakdown of the semiconductor loss at various switching frequencies for case F: GaN Solution.

to A and B comes from the use of the SiC MOSFET. For case D the maximum efficiency is 97.983% and the loss slope is 0.273 mW/Hz. Notice the maximum efficiency of case C is higher than case D due to the increased voltage drop of the SBD, however case D is more resilient to increasing switching frequency. Case E's maximum efficiency is 98.186% and has a loss slope of 0.525 mW/Hz. The loss slope is higher than case C and D due to the increased reverse recovery of the SiC MOSFET body diode. When observing Fig. 4.12, it can be noted that in the range of 1 kHz to 30 kHz, case E has higher efficiency (or less loss) than case C. Although, after that, there is a dip in efficiency and case E and C remain almost the same with increasing f_{sw} (40 kHz - 100 kHz). This is due to the variation in a few different loss mechanism from case E. First, the switching frequency increasing will cause a linear increase in all related switching loss mechanisms and a decrease in the duty cycle of the 3^{rd} quadrant conduction channel of the lower SiC device. Therefore, in the region of 1kHz to 30kHz, the decrease in the conduction loss of the lower switch is able to keep up with the increase in switching loss since it is very low in this region.

However, once the switching frequency is greater than 30k Hz, the switching loss grows by Watts and the decrease in the 3^{rd} quadrant conduction channel is in mW causing a non-constant slope over the entire switching frequency range. In a sense, the decrease in the 3^{rd} quadrant conduction loss cannot keep up with the switching loss growth. Continuing, case F has the worst maximum efficiency at 95.157% but is the most constant over the considered switching frequency region with a loss slope of 0.228 mW/Hz.

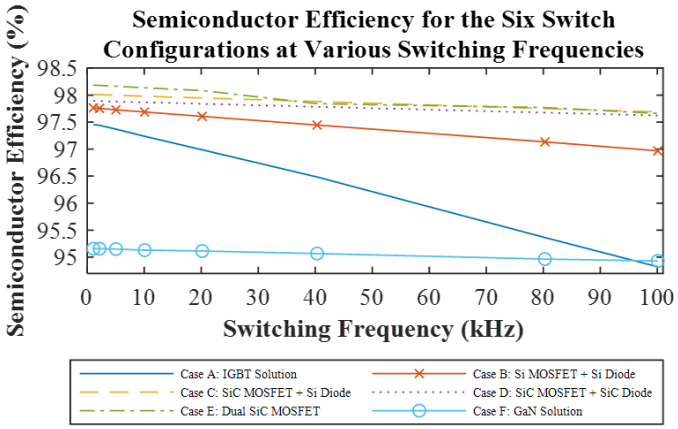


Figure 4.12: Semiconductor efficiency versus switching frequency ($T_j = 125°$C).

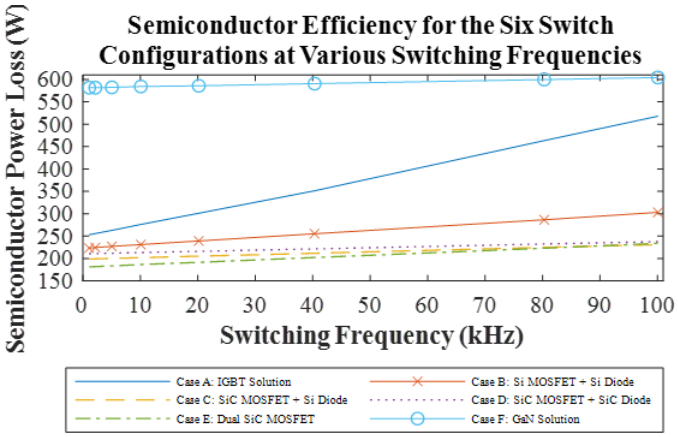


Figure 4.13: Power loss versus switching frequency ($T_j = 125°$C).

Table 26: Maximum semiconductor efficiency and loss slope of CSI deploying each switch configuration.

Configuration	***Max. Semiconductor Efficiency (%)***	***Loss Slope (mW/Hz)***
Case A: IGBT + IGBT Body Diode	97.45	2.674
Case B: Si MOSFET + Si Diode	97.765	0.8064
Case C: SiC MOSFET + Si Diode	98.01	0.3278
Case D: SiC MOSFET + SiC SBD	97.983	0.273
Case E: Dual SiC MOSFET	98.186	0.525
Case F: GaN Solution	95.157	0.228

4.1.2 Total Loss & Optimum Switching Frequency

This section analyzes the efficiency of a CSI deploying each switching configuration considering the semiconductor losses and the passive component losses computed in Chapter 3 (DC-link inductor and filter parts). Fig. 4.14 provides the loss distribution of the CSI between passive components and semiconductor loss at each switching frequency using the loss values from Table 9 and 18. By observing Fig. 4.14, it can be seen that at low switching frequency, the passive component loss is about equal to the semiconductor losses for cases A-E. As the frequency increases, the passive component losses become more negligible as discussed in Chapter 3 and semiconductor losses, of course, increase. Fig. 4.15 shows the efficiency curves for each switch configuration. From this, the optimum switching frequency range is recommended for each configuration in Table 27. For Case A, the optimum switching frequency range is 5 kHz to 10 kHz with the efficiency being relatively constant at its peak value of 97.01%. For Case B, the range is increased to 10 kHz to 20 kHz with an efficiency of 97.54%. Case C shows that replacing the Si MOSFET with a SiC MOSFET increases the optimum switching frequency to the range of 20 kHz to 40 kHz. The efficiency in this region varies from 97.81% to 97.84%. For Case D, the optimum range rem-

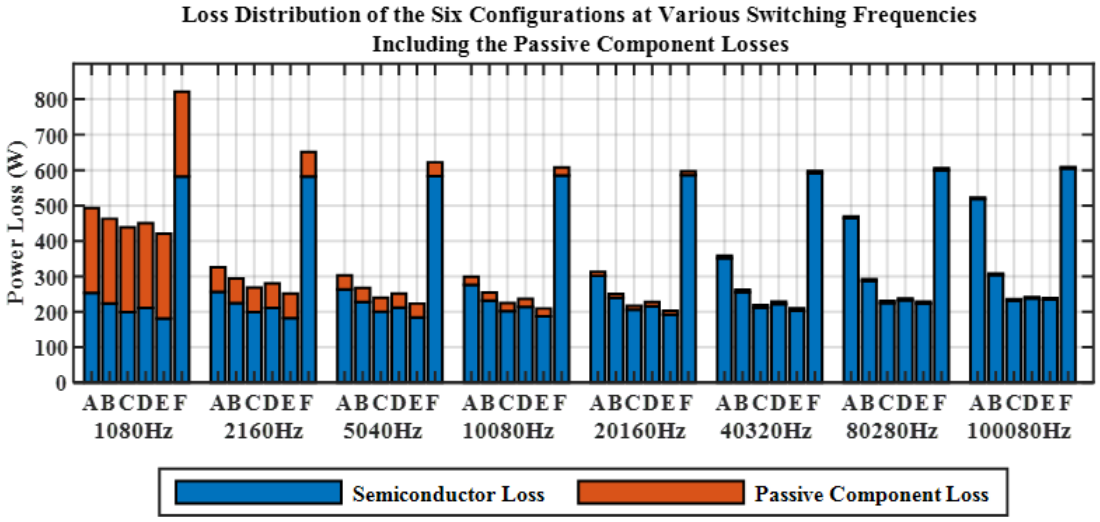


Figure 4.14: Power loss versus switching frequency including semiconductor and passive component losses ($T_j = 125°C$).

ains the same as the prior case, but the efficiency is decreased to 97.73% - 97.71% due to the higher conduction loss of the SiC diode. Case E provides the highest efficiency at 98.01% when $f_{sw} = 20$ kHz. The optimum switching frequency being from 10 kHz (97.908%) to 30kHz (97.907%). The GaN solution shows relatively constant efficiency across all switching frequencies greater than or equal to 10 kHz at 94%. Realistically, it is suitable for operation in the entire tested range, it is the passive components, specifically the electrolytic filter capacitor at f_{sw}=1080 Hz that degrades the efficiency. As previously mentioned, $R_{ds(on)}$ of the GaN switch is over two times that at room temperature at the operating current

and junction temperature making the efficiency much lower than other solutions. Finally, it should be noted that these curves are not absolute. Meaning, they will vary with selected passive component's loss performance, semiconductors, temperature, and operating power. Overall, case E provides the best efficiency followed by cases C, D, B, A, and F. It is worth mentioning that when comparing the pure Si case (case B) to SiC solutions such as case C, D, and E, a small increase is seen. Of course this can be contributed to loss parameters discussed throughout the section but also SiC will enable other advantages such as a smaller sized cooling systems, more power density due to the decrease in passive component size, and higher reliability when exposed to higher junction temperatures.

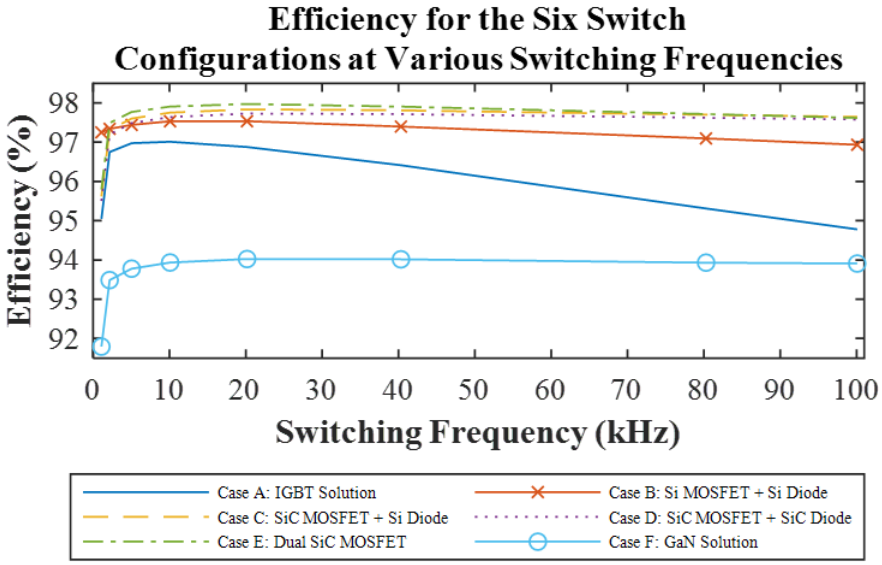


Figure 4.15: Efficiency versus switching frequency including semiconductor and passive component losses ($T_j = 125°C$).

Table 27: Maximum efficiency and optimum switching frequency range of CSI deploying each switch configuration.

Configuration	***Maximum Efficiency (%)***	***Optimum Switching Frequency (kHz)***
Case A: IGBT + IGBT Body Diode	97.01	5-10
Case B: Si MOSFET + Si Diode	97.54	10-20
Case C: SiC MOSFET + Si Diode	97.84	20-40
Case D: SiC MOSFET + SiC SBD	97.73	20-40
Case E: Dual SiC MOSFET	98.01	10-30
Case F: GaN Solution	94.0	10-100

4.1.3 Comparison with Calculations

This section compares the results of the loss calculations using methods discussed in Chapter 3 to the simulation results presented in the prior section. First, Table 29 compares the conduction loss results of each switch configuration at the mentioned ambient temperature under full load conditions. Equations (17)-(21) are used where applicable. The results show less than 5% relative error. Since the conduction

loss for the lower switch in Case E is frequency dependent, the values simulated and calculated at each switching frequency value are provided in Fig. 4.16. The function below is the method used to calculate the conduction loss based on (20), (21), and the characteristics of the C3M0025065K SiC MOSFET. The forward voltage of the body diode is 4 V while the voltage drop of the 3^{rd} quadrant conduction channel is 1.1 V. Under full load conditions the value for I_{DC} is 39.22 A. The relative error remains low for all points considered.

$$P_{D,cond,lower} = 4 \times 39.22 \times (60ns) \times f_{sw} \tag{95}$$

$$P_{Q,cond,lower} = 1.1 \times 39.22 \times (\frac{1}{3} - (60ns) \times f_{sw}) \tag{96}$$

Table 28: Comparison between conduction loss calculations and simulation results under full load conditions (T_j = 125°C).

Configuration		***Calculation (W)***	***Simulation (W)***	***R.E (%)***
A	IGBT	22.7476	22.1	2.93
	IGBT BD	19.61	19.69	0.406
B	Si MOSFET	19.13	19.85	3.63
	Si Diode	17.78	17.33	2.59
C	SiC MOSFET	15.97	15.76	1.33
D	SiC SBD	19.1	19.31	1.09
E	Lower SiC MOS	14.38	14.36	0.14
	Lower SiC BD	10.9m	10.85m	0.46
F	GaN E-HEMT	33.65	32.1	4.61
	GaN Reverse Channel	65.3	64.8	0.93

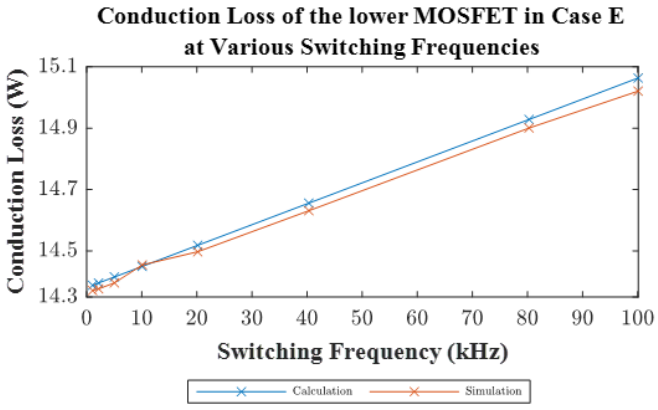


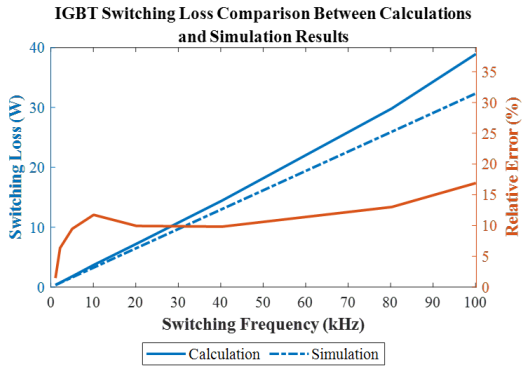
Figure 4.16: Case E (Dual SiC MOSFET) lower switch's frequency dependent conduction loss vs frequency results using simulation and calculation.

Similarly, the switching loss calculation results using (35)-(45) are shown in Table 29 for switching frequency set to 1080Hz. The relative error (R.E) is a bit higher here but since the numeric values are in the mW range, the error truly is minor to the overall CSI loss. Generally, the R.E is less than 18% at this switching frequency. Fig. 4.17 (a)-(h) are provided to compare the results at each switching frequency considered and show more closely the results of the switching loss. Note that the calculations

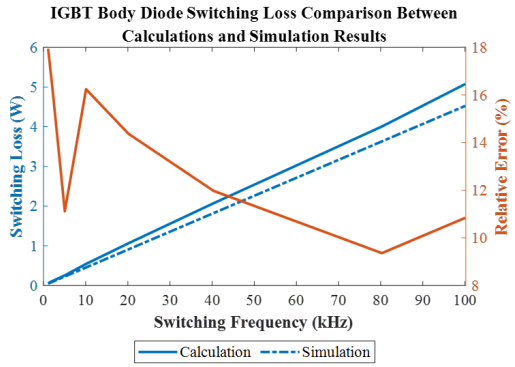
in these figures are carried out by using a linear approximation with the increase in switching frequency. Specifically, this means that the equations are used at f_{sw}=1080Hz and scaled linearly with switching frequency. So the switching loss at f_{sw}=100080Hz is equal to the value at 1080Hz times 100080/1080. By observing Fig. 4.17 (a), there is negligible error for all values of IGBT switching loss values less than 10kHz. After 10kHz the error remains pretty constant at around 15%. For (b), the IGBT body diode reverse recovery loss is shown. The R.E varies from 11% to 18% , with the calculations closely matching the simulated results but just underestimating the loss. For figures (c) and (d), the Si MOSFET and diode switching loss are shown. For the MOSFET, the calculations are carried out using (46)-(55). Again, the switching loss is slightly underestimated with the R.E being low for switching frequencies under 5040Hz and leveling out at about 26% for all other frequencies. For the Si diode, the R.E varies from 13% to 5%, generally decreasing as switching frequency increases. For the SiC MOSFET in (e), the switching loss is closely approximated with R.E remaining below 11% for all cases. This accuracy is mainly due to the wide variety of switching loss data available in the C3M0025065K datasheet. Similar arguments can be made for the remaining plots. Overall, two main points can be made by comparing the calculation results. Realistically, the accuracy of the equations will depend on how close the datasheet testing values are to the application's. This is because there are linear assumptions made between the forward voltage or on-state resistance values with junction temperature, gate resistance, gate-to-source voltage, and in some cases, current. As the results deviate further from the testing values, more error can potentially be introduced. The accuracy will also depend on the amount of data provided to capture accurate scaling with changing conditions. Finally, the linear approximation with switching frequency is just that, an approximation. Since the switching loss in a CSI varies due to different voltages across and ripple currents through the switch, with increasing switching frequency, it is not guaranteed that the switching loss will vary proportionally. The simulation results show that it is close but not exact.

Table 29: Comparison between switching loss calculations and simulation results (T_j = 125°, f_{sw}=1080 Hz).

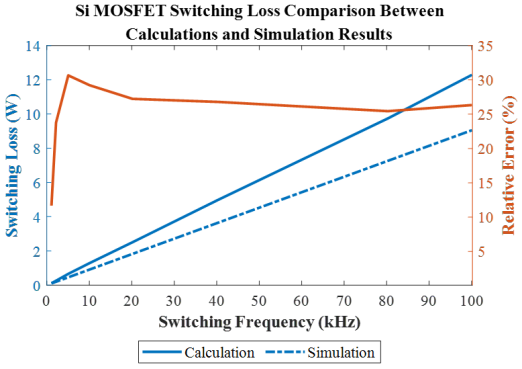
Configuration		***Calculation (mW)***	***Simulation (mW)***	***R.E (%)***
A	IGBT	349.059	354.235	1.46
	IGBT BD	48.84	59.52	17.94
B	Si MOSFET	97.7	110.609	11.67
	Si Diode	9.35	10.77	13.19
C	SiC MOSFET	46.31	48.05	3.62
E	Lower SiC BD	0.36614	0.39521	7.36
	Lower SiC MOS	6.021	6.754	10.85
F	GaN E-HEMT	48.15	41.8	15.2



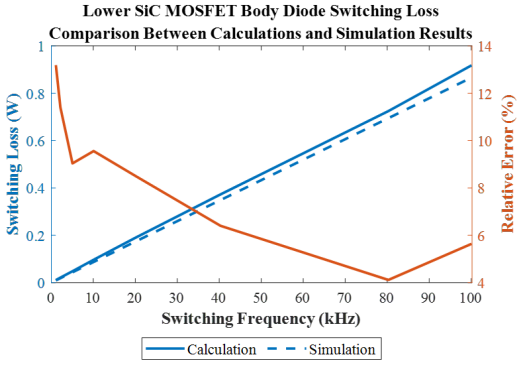
(a) IGBT.



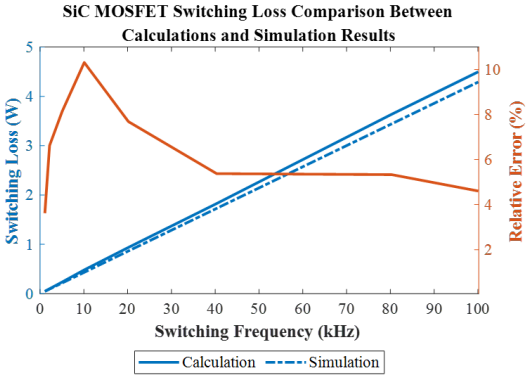
(b) IGBT body diode.



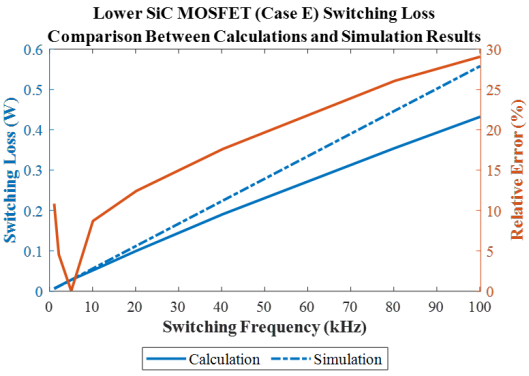
(c) Si MOSFET.



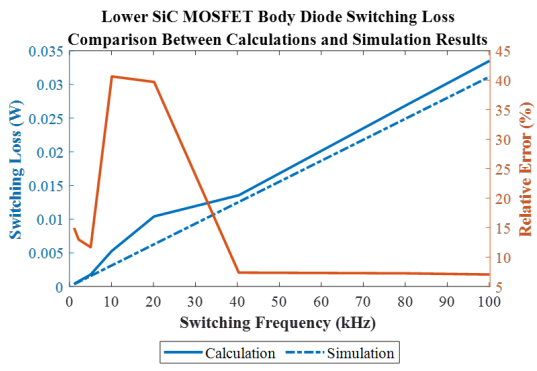
(d) Si diode.



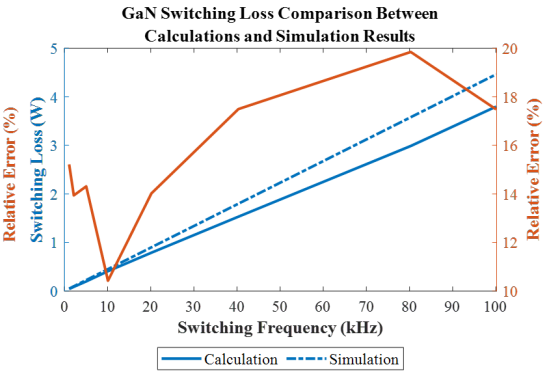
(e) SiC MOSFET.



(f) Lower SiC MOSFET (Case E).



(g) Lower SiC MOSFET body diode (Case E).



(h) GaN E-HEMT.

Figure 4.17: Comparison between switching loss calculations and simulation results for each considered device.

4.2 Efficiency vs Operating Power

Since the power produced by the PV string will vary with environmental conditions, the CSI will operate at different power points. On top of that, a standard way to characterize a solar inverter's efficiency is using weighted efficiency values that include the European efficiency (η_{euro}) and the California Energy Commission (CEC) efficiency (η_{cec}) [102]. These efficiency values are shown in (97) and (98). Practically, there are two main ways to change the CSI's operation in accordance with the varying environmental conditions. First, the DC-link current can be kept constant by varying m_a corresponding to the PV input voltage. This is known as DC-current control for the CSI [4], [103], [104], [105]. Using the power conservation principle in (99) and the definition of the fundamental PWM current $I_{w,1}$ in (100), the required value of m_a based on the input voltage can be determined as shown in (101) [5], [104]. The operating principle of such control scheme is well covered and hence, not discussed further. The only purpose is to provide power loss data at typical operating points.

$$\eta_{euro} = 0.03 \times \eta_{5\%} + 0.06 \times \eta_{10\%} + 0.13 \times \eta_{20\%} + 0.1 \times \eta_{30\%} + 0.48 \times \eta_{50\%} + 0.2 \times \eta_{100\%} \tag{97}$$

$$\eta_{CEC} = 0.04 \times \eta_{10\%} + 0.05 \times \eta_{20\%} + 0.12 \times \eta_{30\%} + 0.21 \times \eta_{50\%} + 0.53 \times \eta_{75\%} + 0.05 \times \eta_{100\%} \tag{98}$$

$$P_{dc} = P_{ac} V_{dc} \times I_{dc} = \sqrt{3} V_{LL} cos(\alpha) \times I_{w,1} \tag{99}$$

$$I_{w,1} = \frac{I_{dc}}{sqrt(2)} \times m_a \tag{100}$$

$$m_a = \frac{V_{in}}{1.5 \times V_{g,peak}} \tag{101}$$

The results of implementing such a control scheme on the inverter efficiency is shown in Fig. 4.18, where the efficiency is plotted versus the operating power as a percentage of the rated power. The switching frequency is kept constant at 10080 Hz since it is a confortable switching frequency for all switch configurations and SQ1 SVM is used. It should be noticed that low efficiency occurs at lower operating powers for any of the switch configurations and the maximum efficiency occurs at rated power. This is because there is no change in the duty cycle with varying m_a as discussed in Chapter 3. This means the loss distribution of the 6 CSI switches does not change at any operating point. Therefore, as per (102), the only variable that changes is P_{in}. So if P_{in} decreases, the numerator becomes small, degrading the efficiency. When comparing the specific switch technologies, no new points that weren't discussed in the prior section can be made since the loss distribution is the same. The efficiency curves considering the passive component loss is provided in Fig. 4.18. The efficiency values are summarized in Table 30.

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \tag{102}$$

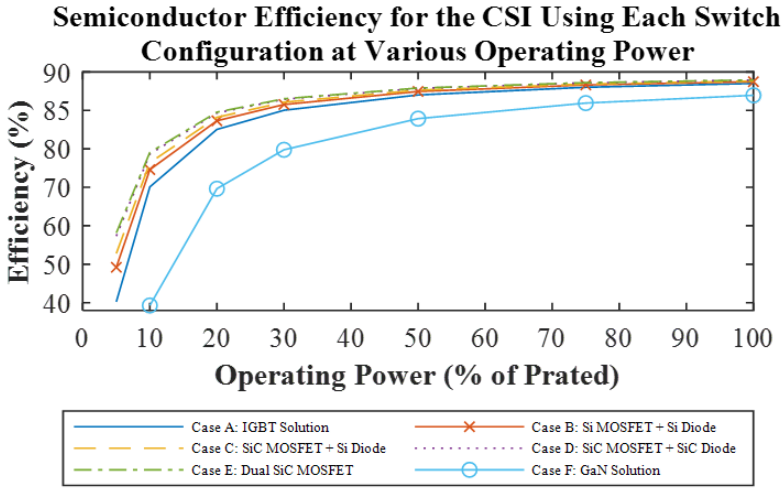
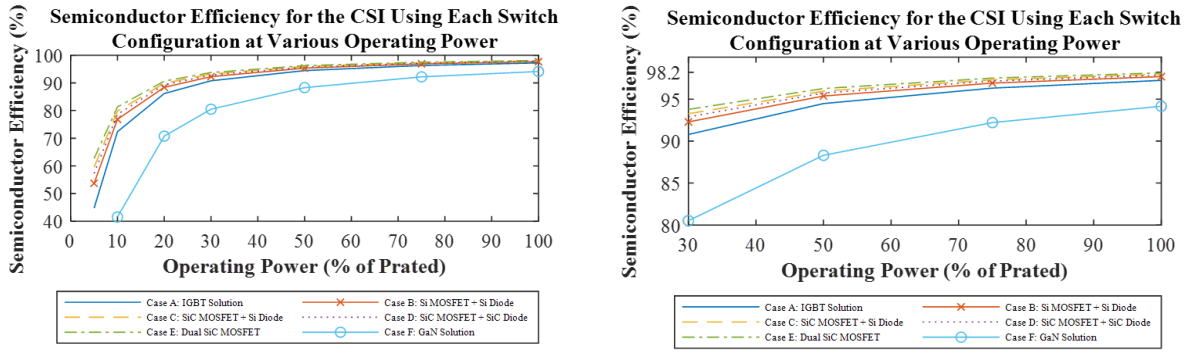


Figure 4.18: Efficiency vs operating power from 5% to 100% with fixed switching frequency, f_{sw} = 10080 Hz and considering passive component loss (using SQ1 SVM) (T_j = 125°C).



(a) 5% to 100% region.

(b) 30% to 100% region.

Figure 4.19: Semiconductor efficiency vs operating power from 5% to 100% with fixed switching frequency, f_{sw} = 10080 Hz (using SQ1 SVM) (T_j = 125°C).

Table 30: Efficiency values for the CSI employing each switch configuration at f_{sw} = 10080 Hz using a constant DC-link current.

Configuration	*Max. Efficiency (w/o Passives) (%)*	*Euro./CEC Efficiency (w/o Passives) (%)*	*Max. Efficiency (w/ Passives) (%)*	*Euro./CEC Efficiency (w/ Passives) (%)*
Case A	97.45	90.764/93.85	97.01	90.01/93.35
Case B	97.765	92.27/94.85	97.54	91.51/94.35
Case C	98.01	93.25/95.50	97.84	92.49/94.99
Case D	97.983	92.87/95.25	97.73	92.11/94.74
Case E	98.186	93.76/95.84	98.01	93.0/95.34
Case F	95.157	80.97/86.99	94.0	79.70/86.48

Another operating principle that can be used for varying the CSI's operating conditions is MPPT control as seen in [4], [105], [106], [107]. Here, the DC-link current and voltage are adjusted according to the PV array characteristics [4], [105]. The modulating index is generally kept constant at 1 (approximately) [106], [107]. Again, such control scheme and PV characteristics are discussed widely in literature and not repeated here. The purpose is to characterize the CSI's loss distribution with varying DC-link current. Therefore, a CSI deploying each switch configuration with varying DC-link current using SQ1

SVM with a switching frequency of 10080 Hz is analyzed in the coming paragraphs.

Based on (97) and (98), the power ratings considered are 500 W, 1000 W, 2000 W, 3000 W, 5000 W, 7500 W, and 10000 W by keeping V_{in} constant at 255 V and varying the DC-link current. The results of the semiconductor losses are shown in Fig. 4.20 and Fig. 4.21. As expected, the loss distribution will change based on the change input current. Of course, a decrease in power loss is to be expected with decreasing DC-link current. See the characteristics discussed in Chapter 1 for further understanding. Note, the duty cycle of the switch still remains equal to 1/3, it is the magnitude of the current through the switch that is changing the loss distribution. The smallest input power considered is 500 W as mentioned, this is at which the peak efficiency occurs for all configurations (when considering just the semiconductor losses), after the input power is reduced further, the efficiency will drop to 0 quickly if plotted. Hence, these points are neglected from the presented data. Note, this data is provided to show detail on the performance of the devices under varying operating conditions. The resulting semiconductor efficiency is provided in Fig. 4.22 and the efficiency considering passive component losses are plotted in Fig. 4.23. To consider the passive components, the loss must be computed at each operating current using the equations covered in Chapter 3. Therefore, the loss of the passive components at each operating power are provided in Table 31. The resulting efficiencies are summarized in Table 32. The results are discussed in more detail in the following section.

Table 31: Passive component loss values with varying power operation, C_f=13.4 uF, L_f=38.98 uH, L_{dc}=366 uH.

Operating Power (W)	***500***	***1000***	***2000***	***3000***	***5000***	***7500***	***10000***
Filter Loss (W)	4.14	4.17	4.29	4.48	5.05	6.13	7.52
DC-Link Inductor Loss (W)	0.0379	0.156	0.641	1.46	4.02	8.87	15.35

Table 32: Efficiency values for the CSI employing each switch configuration at f_{sw} = 10080 Hz with varying DC-link current and V_{in} fixed at 255 V (T_j = 125°C).

Configuration	***Max. Efficiency (w/o Passives) (%)***	***Euro./CEC Efficiency (w/o Passives) (%)***	***Max. Efficiency (w/ Passives) (%)***	***Euro./CEC Efficiency (w/ Passives) (%)***
Case A	98.5	97.83/97.70	97.89	97.59/97.49
Case B	99.38	98.50/98.33	98.81	98.27/98.12
Case C	99.25	98.65/98.51	98.83	98.41/98.3
Case D	99.1	98.56/98.43	98.733	98.33/98.22
Case E	99.65	99.01/98.85	99.27	98.77/98.64
Case F	98.42	96.91/96.59	97.85	96.68/96.38

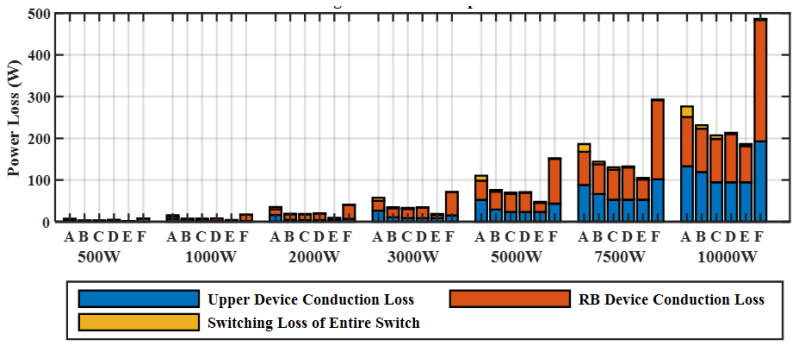
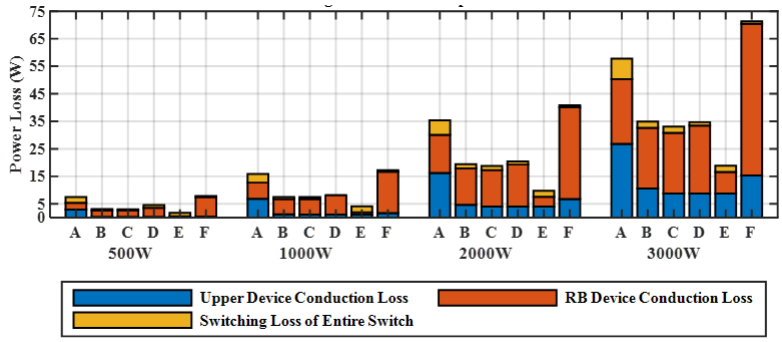
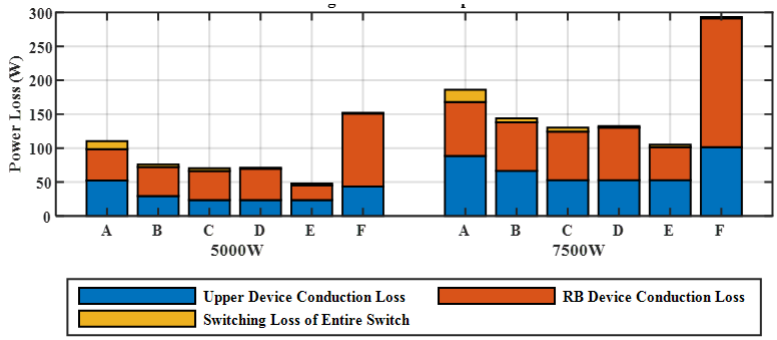


Figure 4.20: Power loss of each switch configuration at various operating power using SQ1 SVM, f_{sw}=10080 Hz (T_j = 125°C).



(a) 5% to 30% results.



(b) 50% and 75% results.

Figure 4.21: Power loss of each switch configuration at various operating power using SQ1 SVM, f_{sw}=10080 Hz, zoomed in versions of Fig. 4.20 (T_j = 125°C).

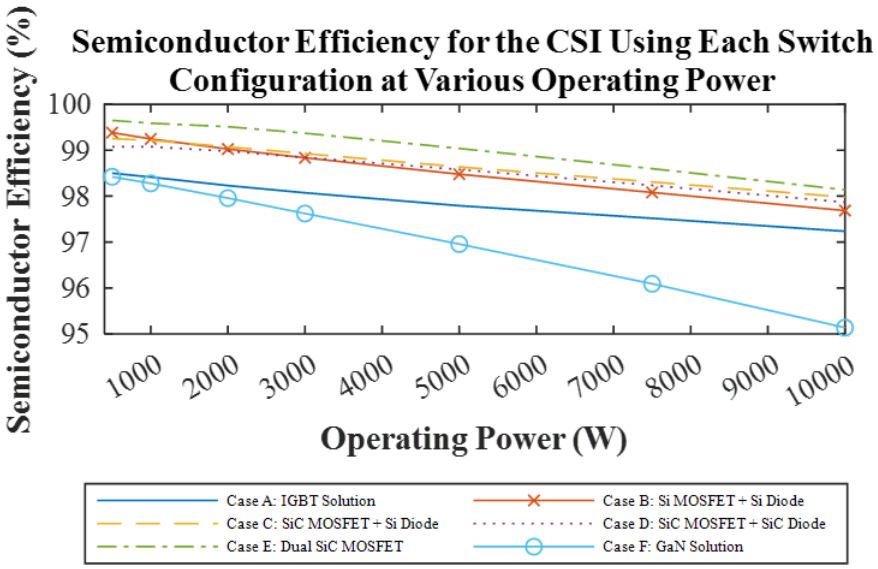


Figure 4.22: Semiconductor efficiency of each switch configuration at various operating power using SQ1 SVM, f_{sw}=10080 Hz, V_{dc}=255 V (T_j = 125°C).

4.2.1 Comparison with Commercialized Products

The following table shows the maximum and European/CEC efficiencies of some commercially available solar inverters with the same parameters as the CSI studied in this report. That is V_{LL}=208

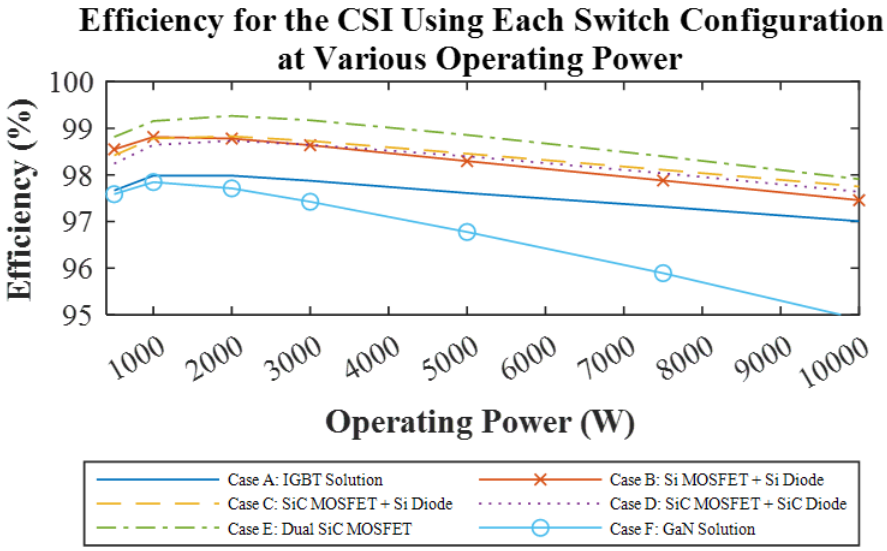


Figure 4.23: Efficiency of each switch configuration at various operating power considering passive components using SQ1 SVM, f_{sw}=10080 Hz, V_{dc}=255 V (T_j = 125°C).

V and P_r=10 kW. Please note, the inverter configurations are not disclosed, but based on the research presented in Chapter 1, it is safe to assume it is VSI-based. It also is not mentioned if any filtering is considered, hence, the results of the semiconductor and overall CSI efficiencies presented in the previous sections are discussed.

First, when keeping the DC-link current constant, the maximum efficiency occurs at full load as shown in Table 30. Case E provides the best maximum efficiency, followed by case C, D, B, A, and F (with or without passive components). Comparing the maximum efficiencies to the commercialized solutions in Table 33, case C (98.01%), D (97.983%), and E (98.186%) are competitive when not considering the losses produced by the passive components. When considering passive components only cases C (97.84%) and E (98.01%) are comparable. However, for any cases the European or CEC efficiencies are not close. Therefore, it would not be recommended to control the CSI in such a manner where the DC-link current is maintained as constant. This is because there will be no change in the semiconductor losses for any operating power, resulting in low efficiency at power ratings below the rated power.

Next, when the input voltage is constant and the DC-link current is varied, the results are more comparable to commercialized solutions. When passive components are not considered, the maximum efficiency of each case is greater than 98.4%. Under such conditions, the maximum efficiency occurs at the lowest input power point considered (500 W or 5% of P_r). Ranking the cases in order from most to least efficient results in case E, B, C, D, A, and F. Case B shows improvements due to the Si devices' superior loss performance at low power operation (as highlighted in the bar graphs in the previous section). The European and CEC efficiencies are competitive and for some cases, beat the commercialized products, aside from the GaN solution and the IGBT CEC efficiency. When the passive components are considered,

the maximum efficiency occurs around 10% to 20% of the rated power for each case. Ranking them by efficiency results in Cases E, C, B, D, A, and F. The European and CEC efficiencies for the GaN and IGBT cases are worse than commercialized products. On the other hand, cases B, C, D, and E all provide efficiency improvements (maximum and European/CEC).

Table 33: Efficiencies for commercialized solar inverters.

Product	***Maximum Efficiency (%)***	***European/CEC Efficiency (%)***
Fronius Symo 10.0-3-M	98.0	97.4
Sunny Boy 10000TL-US	98.3	98.0
Fimer PVS-10-TL	98.4	98.1
Canadian Solar CSI-10k-T400	98.3	97.8
Fimer PVI-10.0-TL-OUTD	97.8	97.1

4.3 Efficiency with Varying Temperature

Of course, the junction temperature will effect the device's loss related parameters. Fig. 4.24 shows the losses of the six configurations with varying ambient temperature from 25°C to 125°C with switching frequency fixed at 1080 Hz. Some interesting points can be made from this graph. Observing case A, the selected IGBT's forward voltage has small variation over the temperature range (see Chapter 1). As a result, the conduction loss of configuration A sees small variation with temperature increments. However, the switching loss increases by 50% over the swept temperatures. Observing the behaviour of the Si devices shows that the power dissipation of the upper switch increases by approximately 2W per device with each temperature step. Contrary, the Si diode forward voltage is inversely proportional to the junction temperature, therefore, a decrease by 2 W per switch is seen with each 25°C increment. The SiC MOSFET shows resiliency to temperature changes, with the power dissipation of a given switch only increasing by 2.74 W over the whole temperature range and the switching loss remaining between 47mW and 48mW. For case E, since the RB device is an SiC MOSFET, the power dissipation grows proportionally with temperature varying from 11.75 W at 25°C to 14.36 W at 125°C. Finally, the GaN forward voltage and reverse conduction channel voltage drop are extremely sensitive to temperature changes. The power dissipation of a given upper switch increases from 13.44W at 25°C to 32.12W at 125°C. For a given lower switch, 40.95W at 25°C to 64.8W at 125°C.

Since all of the simulation results discussed in the previous section are ran at $T_j = 125°$, it is worth mentioning the effect of ambient temperature on the efficiency directly. The semiconductor efficiency is plotted against temperature and shown in Fig. 4.25 under full load conditions. Considering the efficiency at the maximum and room temperature of each configuration will capture the amount the values in the previous sections can vary. For the IGBT configuration, the maximum semiconductor efficiency at 125° is 97.45% as previously discussed and at room temperature, the efficiency is 97.59%. This means the

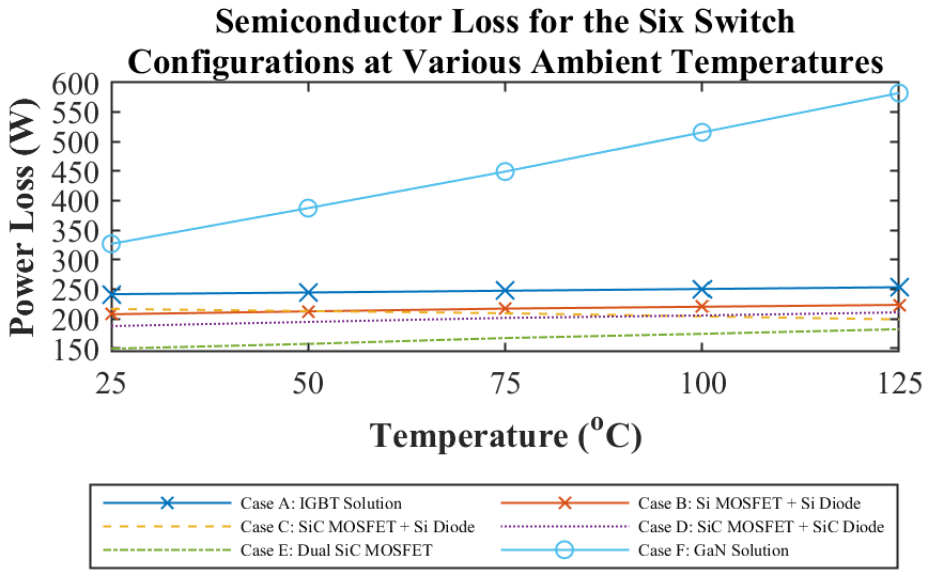


Figure 4.24: Semiconductor loss of each configuration at f_{sw} = 1080 Hz at different ambient temperatures.

maximum variation in the efficiency based on reasonable temperature range operation is 0.14%. Similar arguments can be made for all other switch configurations based on the results presented in Table 34. As previously discussed, the GaN device is very sensitive to variations in temperature and will see the most potential variation from the simulation results presented in the previous sections of the chapter. Also, the efficiency decreases with decreasing temperature for the SiC MOSFET + Si diode case due to the reasons discussed in the previous paragraph, that is, the negative temperature coefficient of the discrete Si diode's forward voltage drop.

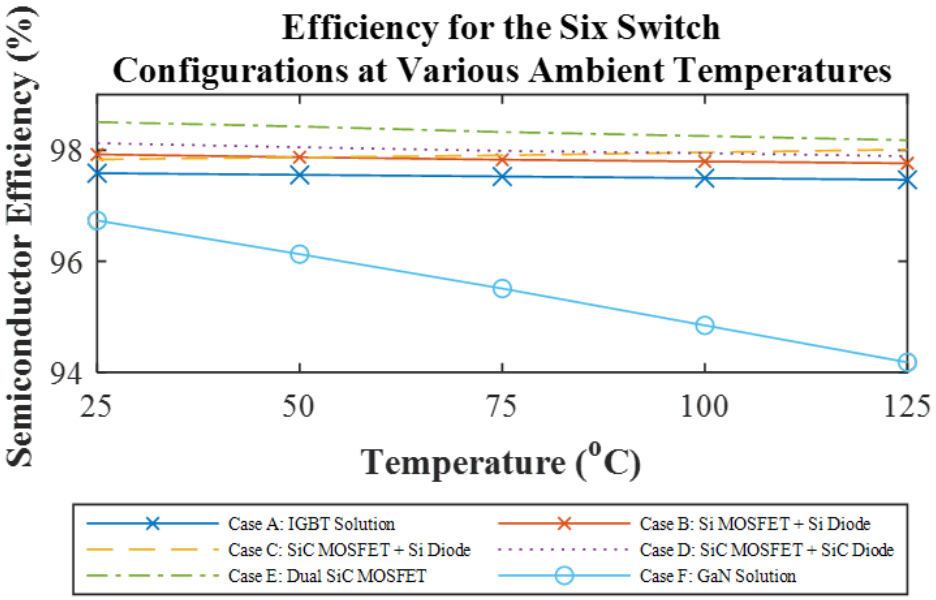


Figure 4.25: Semiconductor efficiency of each switch configuration at various temperatures using SQ1 SVM, f_{sw}=1080 Hz.

Table 34: Efficiency variations with temperature.

Configuration	***Efficiency at*** 25° ***C (%)***	***Efficiency at*** 125° ***C (%)***	***Deviation (%)***
Case A	97.59	97.45	0.14
Case B	97.924	97.765	0.159
Case C	97.835	98.01	0.175
Case D	98.126	97.983	0.143
Case E	98.5	98.186	0.314
Case F	96.734	95.157	1.58

4.4 Efficiency vs SVM Sequence

This section provides a case study on the effect of how the SVM sequence effects the loss distribution with the switching frequency fixed at 10 kHz. For simplicity, only case C is analyzed as varying the sequence will effect all cases in the same manner. Fig. 4.26 shows the loss distribution of the CSI (bar graph) and the CSI efficiency (line). A few points can be made off of this. First, the loss of the semiconductors does not change between sequences. This is because, as discussed in Chapter 3, the duty cycle of the switches do not change. They are fixed to 1/3 no matter the SVM sequence used. This will keep the dominant loss, that is, the conduction losses of the diode (17.33 W per diode) and MOSFET (15.76 W per switch) the same for each case. It can be noted that the switching loss of all configurations is equal, except for SQ3 where the equivalent frequency is reduced by 60Hz due to the pattern (see Chapter 2), causing a decrease from 482mW to 450mW. Note that this is insignificant to the overall efficiency. The real variation in the efficiency comes from the produced passive component losses (filter capacitor + filter inductor + DC-link inductor). These values are taken from Table 12 and 21 and summed. The total loss of the passives for SQ1-SQ6 is 17.41 W, 15.93 W, 23.22 W, 20.86 W, 24.74 W, and 21.55 W respectively. As previously discussed, SQ2 minimizes the DC-link inductor and this results in the best efficiency at 97.82%. Although, the efficiency does not differentiate much between each case. This is because the initial purpose of the SVM sequences in literature was to be applied to low frequency motor drives where the size of the inductor could be reduced or the harmonic performance improved [5], [47]. However, since the switching frequency of this application is much larger (10 kHz compared to 500 Hz), the harmonic content is of less concern and the filter performance between sequences in terms of harmonic suppression and loss is very comparable. Likewise, the DC-link inductor is already quite small as SQ3 presents the maximum of 622 uH while the minimum is 318.5 uH produced by SQ2. This results in low loss variation in the inductor (7.2 W). Overall, the differences between the SVM sequences lessen at higher frequencies, however, efficiency can still be improved minimally by selecting the sequence that minimizes the DC-link inductor. To rank the efficiency, SQ2 is first followed by SQ1 (97.806%), SQ6 (97.765%), SQ4 (97.771%), SQ3 (97.75%), and lastly SQ5 (97.733%).

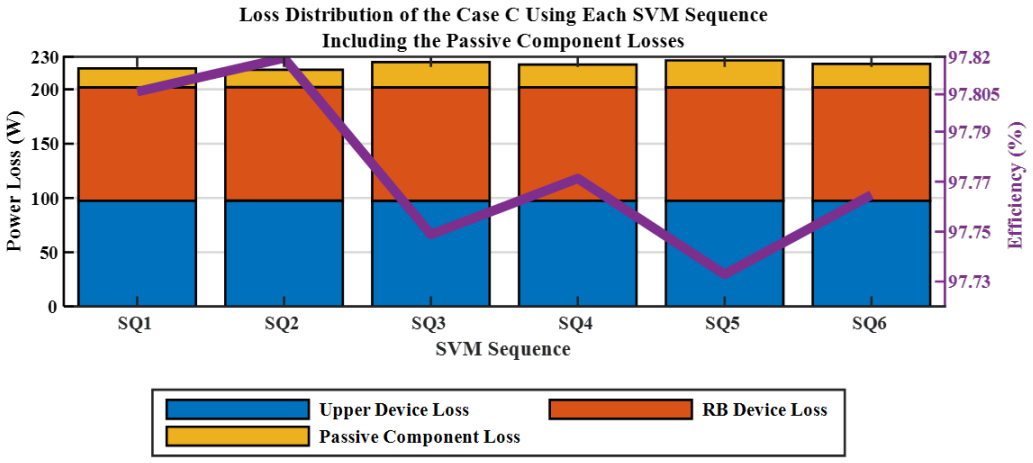


Figure 4.26: Efficiency and loss distribution for case C (SiC MOSFET + Si Diode) switch configuration using various SVM sequences, f_{sw}=10 kHz.

4.5 Cost Comparison

The purpose of this section is compare the cost between the implementations of the CSI with each technology. For fair comparison, the results from section 4.1 are used to determine the switching frequency operation of each configuration. That is, the switching frequency at which maximum efficiency occurs under full load conditions. The selected modulation scheme is SQ1 SVM so that the derived results from Chapter 3 can be used here for simplicity. Tables 35 and 36 show the selected values and corresponding costs of passives and the semiconductors respectively. Note that the costs of the DC-link and AC inductors come from quotes from Micrometals while the costs of the semiconductor components and the filter capacitors come from Digikey or Mouser (the cheapest option). The tabulated values are plotted in Fig. 4.27. It can be noted that solutions implementing WBG semiconductors are able to reduce the costs of passive components, however, not by a magnitude such that costs are comparable to the IGBT case. This is because the efficiency of the WBG implementations is higher, therefore, the delta of the costs is simply the cost to increase the efficiency of the inverter. It is a more fair comparison if the efficiency is held constant across all configurations. However, for cases B-E, this will occur at a switching frequency value outside of the study's range. However, based on Table 36, there will always be an increase in cost when implementing WBG devices. Other savings may be present in the cooling system requirements not considered in this study.

Table 35: Passive component cost comparison between the CSI implementing each switch solution.

Configuration	f_{sw} *(kHz)*	*DC-link Inductor Size (μH)*	*DC-link Inductor Cost (CAD)*	*Filter Capacitor Size (μF)*	*Filter Inductor Size (μF)*	*Filter Cost (C+L) (CAD)*
Case A	5	732	137.56	26.16	76.4	19.89 + 2.66
Case B	10	366	84.76	13.37	38.98	8.39 + 1.25
Case C	20	183	47.31	6.44	19.33	4.33 + 0.9
Case D	20	183	47.31	6.44	19.33	4.33 + 0.9
Case E	30	122	37.14	4.82	14.59	3.84 + 0.63
Case F	40	91.5	31.37	3.20	9.85	1.73 + 0.5

Table 36: Cost of the semiconductor components for each configuration.

Configuration	*Upper Switch Cost (CAD)*	*RB Device Cost (CAD)*	*Total Cost (CAD)*
Case A: IGBT + IGBT Body Diode	7.77	7.77	93.24
Case B: Si MOSFET + Si Diode	41.62	10.78	314.4
Case C: SiC MOSFET + Si Diode	40.50	10.78	307.68
Case D: SiC MOSFET + SiC SBD	40.50	19.21	358.26
Case E: Dual SiC MOSFET	40.50	40.50	486
Case F: GaN Solution	63.60	63.60	763.2

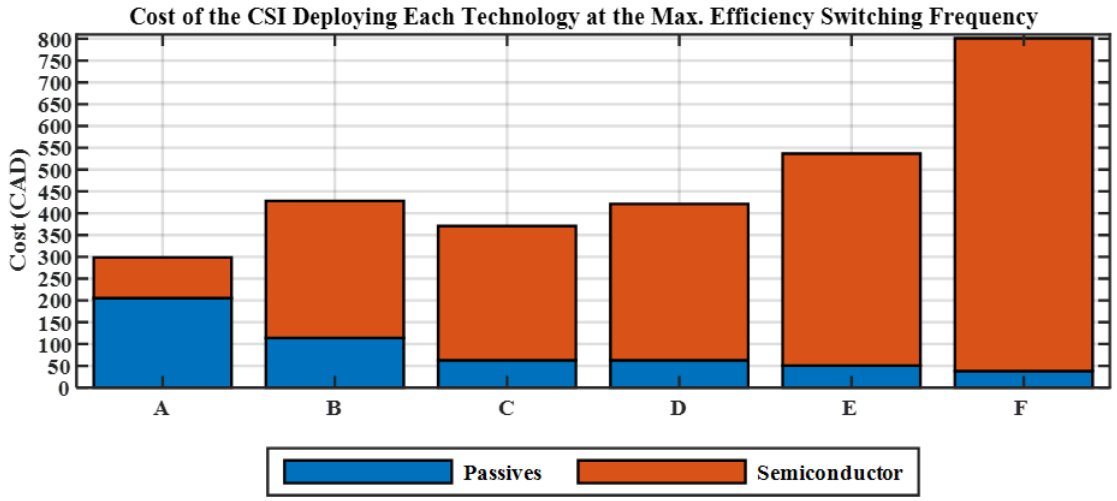


Figure 4.27: Cost comparison based on the data presented in Table 35 and 36.

4.6 Summary

Section 4.1 Efficiency vs Switching Frequency

- Section 4.1.1 compared the losses of each switch configuration with varying switching frequency (1kHz-100kHz).
- The SiC MOSFET provides the lowest conduction loss.
- The GaN-HEMT provides the lowest switching loss but highest conduction loss.
- The maximum semiconductor efficiency was determined for each case:
- Case A (IGBT): 97.45%
- Case B (Si MOSFET + Si Diode): 97.77%
- Case C (SiC MOSFET + Si Diode): 98.01%
- Case D (SiC MOSFET + SiC Diode): 97.98%
- Case E (Dual SiC MOSFET): 98.19%

- Case F (GaN): 95.16%
- The total CSI loss (semiconductor + passive components) was presented and the optimum switching frequency range is defined for each case based on the maximum total efficiency:
- Case A (IGBT): 5-10kHz (97.01%)
- Case B (Si MOSFET + Si Diode): 10-20kHz (97.54%)
- Case C (SiC MOSFET + Si Diode): 20-40kHz (97.84%)
- Case D (SiC MOSFET + SiC Diode): 20-40kHz (97.73%)
- Case E (Dual SiC MOSFET): 10-30kHz (98.01%)
- Case F (GaN): 10-100kHz (94.0%)
- Simulated results were compared with calculation methods covered in Chapter 3 and deemed acceptable.

Section 4.2 Efficiency vs Operating Power

- The CSI power loss was characterized over multiple operating power, with the power points picked based on standard efficiency definitions, η_{euro} and η_{CEC}. The switching frequency was fixed at 10kHz.
- The first method for varying the power was changing the input voltage and m_a corresponding to the power conservation principle, where the DC-link current is kept constant.
- The results showed the maximum efficiencies occurred for all cases at the rated power (with and without passive components). See the results from Table 30.
- Low efficiency occurred at low power operation due to the fact that the loss distribution is kept constant with constant DC-link current and varying m_a. This resulted in low European and CEC efficiency that is not comparable to commercialized products.
- The second method for varying the power was keeping the input voltage constant and varying the input current.
- This resulted in the maximum semiconductor efficiency for each case occurring at the lowest power point (P_{in}=500W):
- Case A (IGBT): 98.5%
- Case B (Si MOSFET + Si Diode): 99.38%
- Case C (SiC MOSFET + Si Diode): 99.25%

- Case D (SiC MOSFET + SiC Diode): 99.1%
- Case E (Dual SiC MOSFET): 99.65%
- Case F (GaN): 98.42%
- When considering passive component loss, the maximum efficiency point shifts to around 10% to 20% of the rated power for each case:
- Case A (IGBT): 97.89%
- Case B (Si MOSFET + Si Diode): 98.81%
- Case C (SiC MOSFET + Si Diode): 98.83%
- Case D (SiC MOSFET + SiC Diode): 98.73%
- Case E (Dual SiC MOSFET): 99.27%
- Case F (GaN): 97.85%
- Section 4.3 discussed the effect of temperature on the efficiency values presented in the previous section. Based on the efficiency at room temperature and at 125^{circ}, the maximum deviation in efficiency values was determined to be:
- Case A (IGBT): 0.14%
- Case B (Si MOSFET + Si Diode): 0.159%
- Case C (SiC MOSFET + Si Diode): 0.175%
- Case D (SiC MOSFET + SiC Diode): 0.143%
- Case E (Dual SiC MOSFET): 0.314%
- Case F (GaN): 1.58%
- Section 4.4 compared the losses of case C (SiC MOSFET + Si Diode) with each SVM sequence with f_{sw} set to 10kHz. The results showed little deviation due to the fact that the duty cycle will remain constant for all cases. Any deviation occured due to the small difference in passive component losses.
- Overall, case E is the recommended configuration due to its superior conduction loss performance. It also enables high switching frequency operation and other WBG device advantages discussed.
- Section 4.5 provided a cost comparison showing that WBG are currently much more costly than conventional device. The delta in costs can be accounted for as the cost in raising the CSI efficiency.

5 Conclusion

5.1 Conclusions & Contributions

5.1.1 Summary

The CSI configuration can offer advantages in PV energy systems such as inherent short circuit protection, natural voltage boosting capabilities, increased reliability, lower inherent switching loss, and increased power density. However, the CSI configuration suffers from large conduction losses and a bulky, costly, and lossy DC-link inductor. With WBG devices available, their characteristics can assist with these two technical challenges. Therefore, this thesis analyzed the CSI efficiency with various switch configurations under numerous operating points (switching frequency, operating power, temperature, and SVM sequence). The switch configuration studied included case A: IGBT switch in series with IGBT body diode, case B: Si MOSFET in series with discrete Si diode, case C: SiC MOSFET in series with Si diode, case D: SiC MOSFET in series with SiC SBD, case E: Dual SiC switch, and case F: Anti-series GaN solution. The passive component sizing methods along with loss computations were presented in depth in order to accurately estimate the overall CSI efficiency. This all provides context to the base CSI's maximum obtainable efficiency.

First, the CSI's efficiency at various switching frequencies (1-100 kHz) was presented. The loss distribution showed that the SiC MOSFET provided the lowest conduction loss providing a 20.6% and 28.7% decrease in loss when compared to IGBT and Si-based solutions. The GaN device showed the best switching loss performance, having relatively constant efficiency over the entire range. However, it suffers from the largest amount of conduction loss and high sensitivity to temperature. Ranking each configuration from highest to lowest maximum semiconductor efficiency for each configuration A-F at rated power is E, C, D, B, A, and F (see Chapter 4 for efficiency values). When considering passive components, the optimum switching frequency of each configuration was recommended. For case A, 5-10kHz, for case B, 10-20kHz, for case C and D, 20-40kHz, for case E 10-30kHz, and case F, 10-100kHz.

Next, the operating power was varied and loss distribution was discussed. With constant DC-link current, the CSI shows poor performance when compared to commercialized solutions at low power operation due to the unchanging loss distribution to that at full load. The maximum efficiency for each case occurred at the rated power. A second method for varying the power was presented, that is, the DC-link current was varied. This resulted in the maximum semiconductor efficiency appearing at 5% of the rated power (the lowest power point) with the same efficiency as the other cases at full load. This resulted in higher European and CEC efficiencies than commercialized solutions for cases B, C, D, and E.

Continuing, the effect of varying temperature and SVM sequence were studied. The temperature's effect on efficiency deviations were presented and determined that the IGBT case had the most resilience to temperature change due to the forward characteristics of the body diode and conduction channel (see Chapter 1). For varying the sequence, little to no change is seen in the loss distribution at higher switching frequency due to the fact that the duty cycle of the switch remains constant for all cases. Any variation observed is due to the difference in the required passive components' generated loss. Lastly, a brief discussion on system costs are discussed.

5.1.2 Conclusions

This section summarizes the main findings from all of the data presented. First, WBG devices are capable of providing a significant reduction to the switching losses. However, the CSI features inherently low switching losses due to low commutation voltage. As a result, the efficiency of the CSI is not improved by a meaningful value due to this factor alone. Next, SiC MOSFETs are able to significantly reduce the conduction losses. This makes the device a prime candidate for implementation in the CSI. Out of all switch configurations, case E is able to provide the best efficiency across all cases. This is due to the fact that the RB device forward voltage is reduced. On top of that, due to the use of WBG devices in case E, the switching frequency can be increased by an additional 10 kHz based on the typical value for this application. This results in downsized passive components further resulting in higher power density and lowered passive costs. The GaN device was shown to provide the highest amounts of conduction loss. Of course, this makes the technology unsuitable for the CSI. The recommended application of the GaN device is low power, low duty cycle, and controlled temperature applications. It can also be noted that the SiC SBD provided higher conduction losses than the Si diode. This is due to the wider bandgap introducing higher voltage drops. Again, this makes the device unsuitable for the CSI. The recommended application is those where reverse recovery losses introduce challenges. When varying the operating power, it was seen that most of the switch configurations are competitive and even improve efficiency characterization when compared with commercialized solutions. However, other factors effect the use of the CSI, including available semiconductor modules and controller response time due to the DC-link inductor. Finally, when varying the SVM sequences at 10 kHz, the results showed that SQ2 produces the lowest DC-link inductor size and best efficiency when applied to the CSI.

5.1.3 Contributions

Overall, a comprehensive case study comparing new WBG semiconductors and conventional Si devices when applied to low power CSIs with varying conditions (switching frequency, operating power, and modulation scheme) was presented. This provides context to efficiency limitations of the CSI using

different technology. Modelled equations and an in depth look at effecting semiconductor loss parameters were also presented, enabling clear reasoning behind sources of loss and potential points for improvements. A method for computing CSI semiconductor losses by applying fundamental loss equations to CSI commutation waveforms was proposed and confirmed with simulations. The losses of passive components, an often overlooked factor in power loss studies, are considered in depth, with equations and methodology for CSI specific considerations highlighted. Specifically, the methodology for sizing the DC-link inductor for each SVM SQ is extended to high frequency applications and supporting equations are derived. Also, the methodology for sizing the CL filter is expanded upon by considering not only the IEEE 519-2014 requirements, but also the desired filter performance. Applying and comparing the different SVM sequences at high switching frequency has not yet been reported in literature.

5.2 Future Work

The following list presents some potential future works based off of the presented results.

1. Experimental results to further support simulations and calculations. This will also provide numerical data for deviation in results caused by assumptions made in the thesis.

2. Investigating a modulation scheme that can reduce the duty cycle. Using SHE type calculations, the duty cycle of the switch can be minimized. Specifically, the duty cycle could be reduced from 0.33 to 0.31 at the expense of worse harmonic performance. For this application this would result in approximately a 1 W power loss reduction for the SiC MOSFET conduction loss, improving efficiency further.

3. Continue to monitor the state of commercialized WBG device performance. 4th generation SiC devices by ROHM improve on previous iterations by a significant margin [108]. Ratings include 650 V, 750 V, 1200 V with current ratings ranging 30-80 A.

4. CSI requires fast switching device that can achieve RB in a single stage. There is already development of a RB GaN device with very low conduction loss that can achieve such operation but is not yet commercially available [46].

5. Investigate further into new hybrid CSI and switch configurations that can reduce the conduction loss further.

6. As mentioned in [56], the delay time in the response of PQ and MPPT control in the CSI is a challenge due to the large DC-link inductor. With the proven ability of SiC MOSFETs to reduce the DC-link inductor size, an investigation into the response time at higher switching frequencies should be conducted and compared to commercialized VSI-based inverters.

7. Carry out cost comparison of the CSI deploying each switch configuration at equal efficiency.

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A Generalized Harmonic Content of SVM Sequences 2-6

Table A1: Dominant harmonics for SQ2 SVM expressed in terms of m_f (m_a=1).

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental***
$m_f - 13$	0.6
$m_f - 11$	0.17
$m_f - 7$	1.7
$m_f - 5$	0.62
$m_f - 1$	12.8
$m_f + 1$	26.5
$m_f + 5$	25.6
$m_f + 7$	10.4
$m_f + 11$	2.6
$m_f + 13$	0.6
$m_f + 17$	1.4
$m_f + 19$	11

Table A2: Dominant harmonics for SQ3 SVM expressed in terms of m_f (m_a=1).

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental***
$m_f - 13$	4.5
$m_f - 11$	4.6
$m_f - 7$	4.5
$m_f - 5$	5
$m_f - 1$	18.1
$m_f + 1$	19
$m_f + 5$	23
$m_f + 7$	12
$m_f + 11$	1.2
$m_f + 13$	3.2
$m_f + 17$	11.4
$m_f + 19$	6.5

Table A3: Dominant harmonics for SQ4 SVM expressed in terms of m_f (m_a=1).

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental***
$m_f - 13$	19.3
$m_f - 11$	19.3
$m_f - 7$	27.6
$m_f - 5$	27.8
$m_f - 1$	14.92
$m_f + 1$	3.5
$m_f + 5$	8.5
$m_f + 7$	3.5
$m_f + 11$	8.3
$m_f + 13$	3.7
$m_f + 17$	4.2
$m_f + 19$	13.1

Table A4: Dominant harmonics for SQ5 SVM expressed in terms of m_f (m_a=1).

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental***
$m_f - 13$	5.6
$m_f - 11$	12
$m_f - 7$	27.5
$m_f - 5$	20.2
$m_f - 1$	13.25
$m_f + 1$	17.9
$m_f + 5$	11
$m_f + 7$	9.4
$m_f + 11$	14.8
$m_f + 13$	3
$m_f + 17$	1.4
$m_f + 19$	8.2

Table A5: Dominant harmonics for SQ6 SVM expressed in terms of m_f (m_a=1).

Dominant Harmonic Numbers as an Expression of mf	***Maximum Magnitude as a Percentage of the fundamental***
$m_f - 13$	4.3
$m_f - 11$	2.5
$m_f - 7$	22.1
$m_f - 5$	36.9
$m_f - 1$	2.9
$m_f + 1$	6.3
$m_f + 5$	2.8
$m_f + 7$	39.8
$m_f + 11$	14.1
$m_f + 13$	6.5
$m_f + 17$	18.8
$m_f + 19$	1.5

B Power Loss Computations for the Filter Capacitor

Table B1: Power loss due to each harmonic component of the filter capacitor current m_f=36, ma=1, C_f = 390μF, ESR = 0.475Ω.

Harmonic Number	***Power Loss (W)***
fund.	209.475
23	1.91m
25	2.06m
29	13.6m
31	5.66m
35	54.4m
37	2.1
41	1.86
43	408m
47	23.3m
49	22.4m
53	57.4m
55	717m
59	33m
61	128m
65	270m
67	182m
Total Loss From Harmonics	7.03W (3.25% of total loss)