A Single-Phase H-Type Five-Level Current Source Inverter

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Abstract

Current Source Inverters (CSIs) have drawn growing attention in modern energy conversion systems due to their inherent voltage-boosting capability, reliable short-circuit protection, and smooth output current profiles. This dissertation investigates single-phase multilevel CSIs and systematically reviews the evolution of three-level, five-level, and seven-level topologies. The advantages and limitations of different five-level CSI configurations are further analyzed, and the trade-off between output current quality, circuit complexity, and efficiency indicates that the five-level CSI provides a suitable balance for practical applications. However, conventional five-level CSIs suffer from dc current imbalance, which necessitates complicated active balancing control schemes.

Although a recently developed single-phase X-type five-level CSI successfully achieves inherent current balancing without complex external controllers, it requires significantly large DC inductors, which inevitably leads to increased system volume, higher manufacturing costs, and degraded efficiency. To overcome these limitations, this dissertation presents a novel single-phase H-type five-level CSI. The proposed topology retains the self-balancing capability for inductor currents while significantly reducing the required DC inductance across its full operating range.

The operating principle, modulation scheme, passive component design, inductor current self-balancing, switch voltage stresses, and power losses of the proposed inverter are investigated. A comparative analysis is performed between the proposed H-type and X-type five-level CSIs in terms of required dc inductance, peak voltage of switches, semiconductor device count, and efficiency. Finally, the performance of the proposed inverter is verified through MATLAB/Simulink simulations and lab-scale experiments.

Acknowledgments

I sincerely thank my supervisor, Dr. Qiang Wei, for his invaluable guidance, thoughtful critiques, and continuous support throughout this project.

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Symbol	Meaning
C_f	filter capacitor
D	duty cycle
D_1	diode
f_{sw}	switching frequency
I_{dc}	DC current
i_L	inductor current
i_w	PWM output current
i_s	output sinusoidal current
L_{dc}	DC inductor
L_f	load inductor
m_a	modulation index
R	load resistor
S_1-S_7	switches
Δt	dwell times
V_{in}	input voltage
E_{on}	turn-on energy
E_{off}	turn-off energy
V_{L_max}	maximum voltage across the inductor

List of Abbreviations

Abbreviation	Meaning
CSI	current source inverter
CSR	current source rectifier
EV	electric vehicle
GCT	gate-commutated thyristor
GTO	gate turn-off thyristor
IGBT	insulated gate bipolar transistor
LCC	line-commutated converter
MFT	medium-frequency transformers
MMC	modular multilevel converter
MOSFET	metal-oxide-semiconductor field-effect transistor
MV	medium voltage
PV	photovoltaic
PWM	pulse width modulation
SCR	silicon-controlled rectifier
SGCT	synchronous gate-commutated thyristor
THD	total harmonic distortion
VSI	voltage source inverter

Chapter 1 Introduction

Current Source Inverter (CSI) technology [1-3] has been widely accepted in the drive industry, primarily categorized into Pulse Width Modulation (PWM) inverter [4-7] and Load-Commutated inverter (LCI) [8][9]. The Silicon-Controlled Rectifier (SCR)-based LCI [10-12] is suitable for very large synchronous motor drives, while the PWM current source inverter is a preferred choice for most industrial applications. The parallel PWM CSI is composed of two or more single-bridge inverters connected in parallel for super-high-power applications. These PWM inverters employ switching devices with self-extinguishable capability, such as symmetrical gate-commutated thyristors (GCTs) [13] or gate turn-off thyristors (GTOs) [14], alongside with larger dc-link inductors that establish a nearly constant input current. By applying PWM techniques, the inverter synthesizes a sinusoidal output current with controllable amplitude and frequency while maintaining the dc-link current nearly constant. Characterized by the simple converter topology and reliable short-circuit protection, the PWM CSI has become one of the widely used converter topologies for the MV drives [15-17].

This chapter presents a comprehensive literature review of single-phase multilevel PWM Current Source Inverters, with particular emphasis on the technological evolution from conventional three-level topologies to advanced five-level and higher-level configurations [18-21]. The review begins with conventional single-phase three-level CSIs, highlighting its structural simplicity alongside key drawbacks such as limited Total Harmonic Distortion (THD) performance, heavy passive component requirements, and vulnerability to open-circuit faults [22][23]. To improve voltage boosting capability and system reliability, impedance-network-based three-level CSI has been proposed [24-26]. Although these approaches enhance specific performance characteristics, their output waveform remains fundamentally constrained by the limited number of current levels.

To achieve better power quality, single-phase five-level CSIs are then reviewed [27-29], which are categorized into multi-source and single-source topologies. Compared with three-level inverters, five-level CSIs provide superior output current quality, reduced harmonic distortion, lower filter requirements, and improved voltage stress distribution across semiconductor devices [30][31]. Nevertheless, existing five-level topologies introduce new challenges, including higher circuit complexity, more components, and dc-link current balancing issues.

To further enhance waveform quality, single-phase seven-level CSIs are also reviewed. While these converters can achieve additional reductions in THD and output current ripple, they generally require substantially more semiconductor devices, increased conduction losses, more complicated overlap-time commutation strategies, and higher implementation cost. Consequently, considering the trade-off among harmonic performance, efficiency, reliability, and circuit complexity, five-level CSIs are widely regarded as a more practical solution for medium- and high-power applications.

Based on this analysis, that chapter identifies the remaining limitations of existing single-source five-level CSIs, particularly the dc-link current imbalance, the requirement for large dc inductors, and the use of series-connected power switches. These challenges motivate the development of the proposed single-phase H-type five-level CSI presented in this thesis. The proposed topology achieves inherent dc-link inductor current self-balancing while significantly reducing the required dc inductance. Furthermore, it eliminates the need for series-connected switches, enabling the use of low-voltage semiconductor devices to reduce voltage stress, power losses, and implementation cost, while improving the overall converter performance.

1.1 Single-Phase Three-Level Current Source Inverters

This section reviews the development of single-phase three-level CSI, focusing on the conventional H-bridge topology and impedance-network-based topology, including

the Z-source CSI. For each topology, the circuit configuration, operating principle, advantages and limitations are discussed.

1.1.1 Conventional H-bridge Three Level CSI

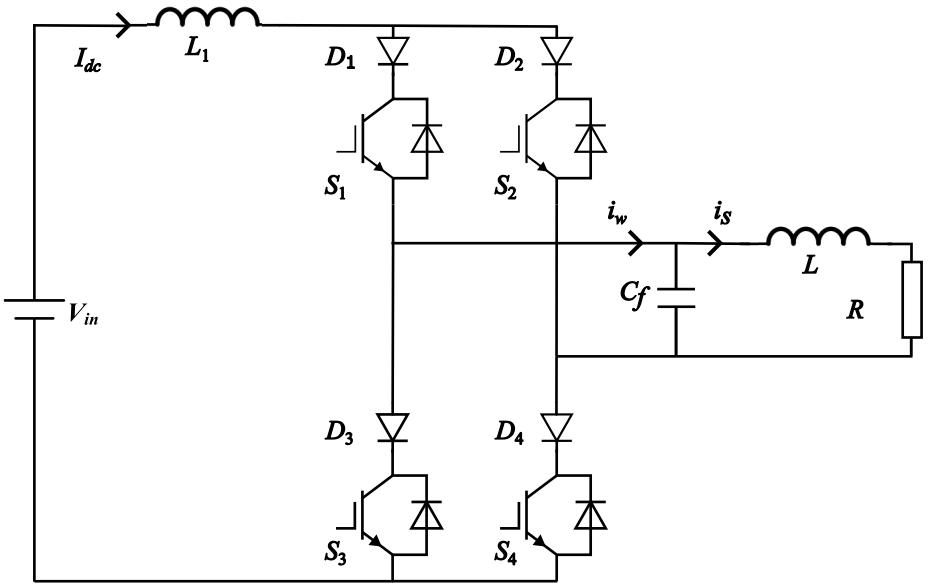
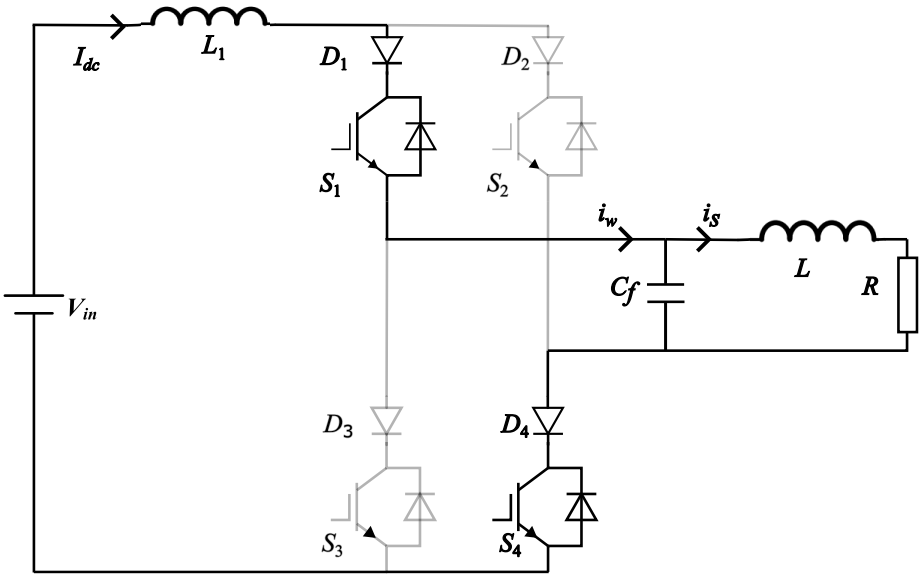


Fig. 1 - 1 Single-phase conventional H-bridge three-level CSI

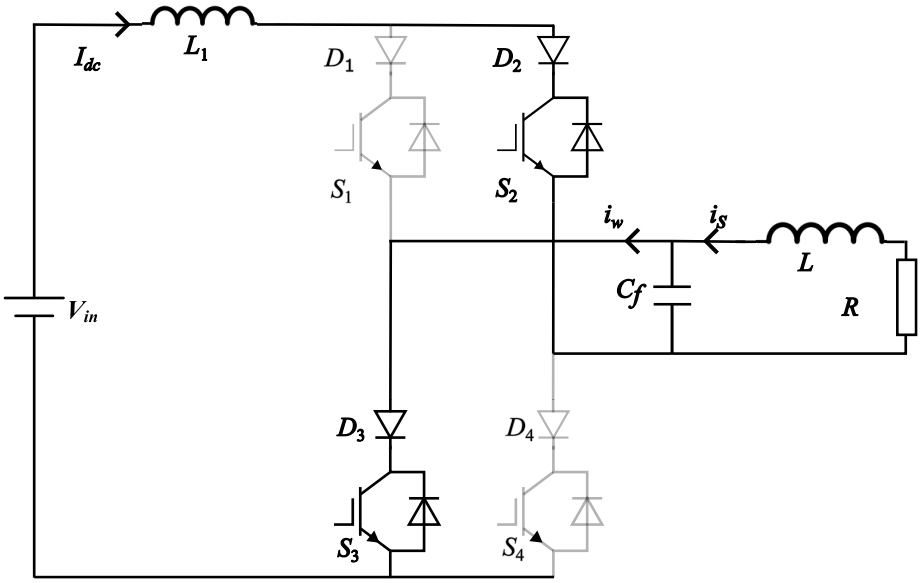
A single-phase conventional H-bridge three-level CSI is shown in Fig. 1-1. The inverter is composed of four switching devices (S_1-S_4), series-connected with four diodes, with a reverse voltage blocking capability. And each of them can be replaced by two or more series devices for medium voltage applications. The inverter produces a defined PWM output current i_w.

In this current source inverter, the dc current source is realized by voltage source V_{in} connected in series with a dc inductor L_1. This dc choke serves as an indispensable energy storage element, suppressing current ripple to maintain a smooth, continuous dc-link current I_{dc}. And the current source inverter requires an ac capacitor C_f at its output for switch commutation and harmonic filtering. When switch S_1 turns off, the capacitor provides a path for the inductive current, preventing dangerous high-voltage spikes ($L\frac{di}{dt}$) as the PWM output current i_w rapidly drops to zero; without this path, these

voltage spikes would damage the switching devices. Additionally, the capacitor acts as a low-pass filter, smoothing the output load current waveforms.



(a) Mode 1



(b) Mode 2

Fig. 1 - 2 Operation principle of conventional H-bridge three-level CSI

As shown in Fig. 1-2, the inverter turns on switches S_1 and S_4, turns off switch S_2 and S_3 (Mode 1), it routes current through the load in the positive direction to generate the + I_{dc} level. To produce the -I_{dc} level, the inverter turns on switches S_2 and S_3, turns off switches S_1 and S_4 (Mode 2), which reverses the load current direction while

maintaining unidirectional dc link flow. The inverter creates the zero-current output level by turning on both switches in a single leg, which forms an internal freewheeling path that bypasses the load. To prevent open-circuit faults during commutation, the inverter enforces an overlap time during switching transitions, ensuring that incoming switches turn on before outgoing switches turn off to maintain a continuous dc current path and suppress inductive over-voltage spikes.

The conventional single-phase H-bridge three-level current source inverter benefits from structural simplicity, inherent short-circuit protection and no d_v/d_t issue, but this inverter requires a bulky dc link chock to smooth the input current and exhibits high vulnerability to open-circuit failures caused by electromagnetic interference (EMI) or gating misfires. To resolve these limitations, the impedance-network-based three-level CSI family such as Z-source CSI was introduced [32-35].

1.1.2 Impedance-Network-Based Three Level CSI

As shown in Fig. 1-3, the impedance-network-based three-level CSI, commonly realized using the classic Z-source topology, integrates a two-port passive impedance network composed of inductors (L_1 and L_2) and capacitors (C_1 and C_2) in an X-shaped configuration between the dc power source and the inverter bridge.

The dc source can be a battery, diode rectifier, thyristor converter, fuel cell, and inductor, a capacitor, or a combination of those. The main bridge of the inverter is composed of four switching devices (S_1-S_4), each connected in series with a diode to provide reverse voltage blocking capability. And the impedance network inductors (L_1 and L_2) can be configured as two separate inductors or integrated into a single coupled inductor. The Diode D in series with the input source V_{in} is usually needed for preventing reverse current flow.

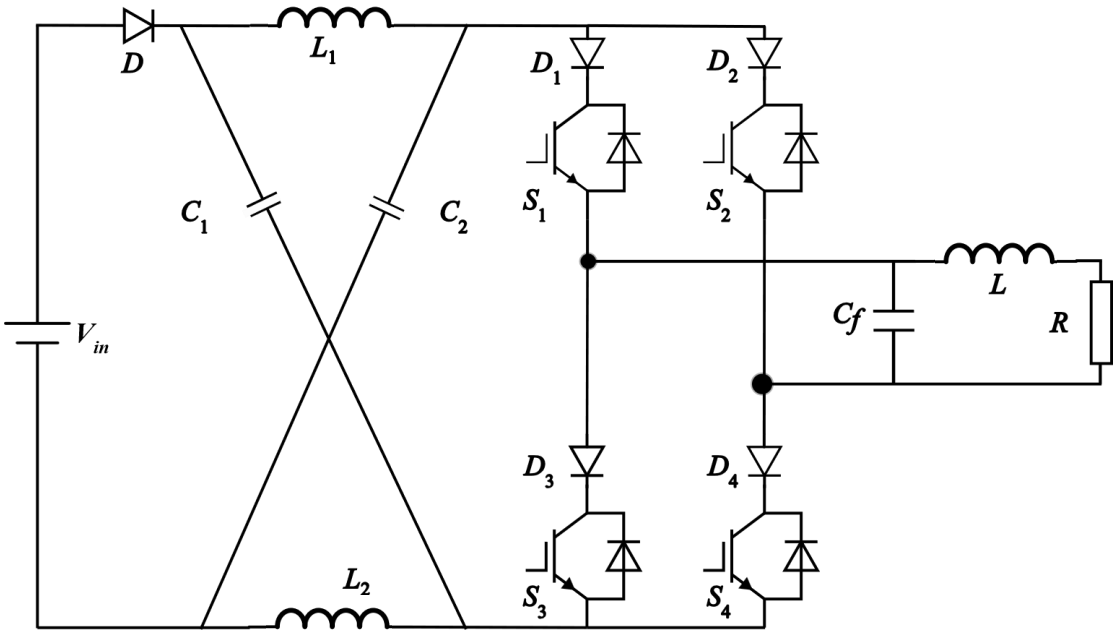
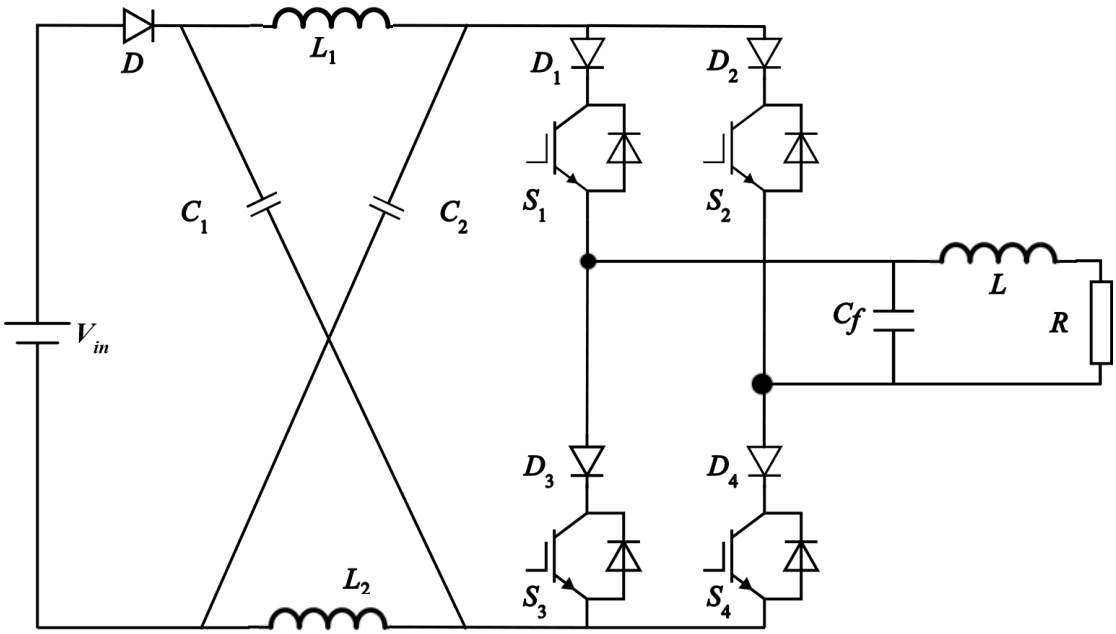
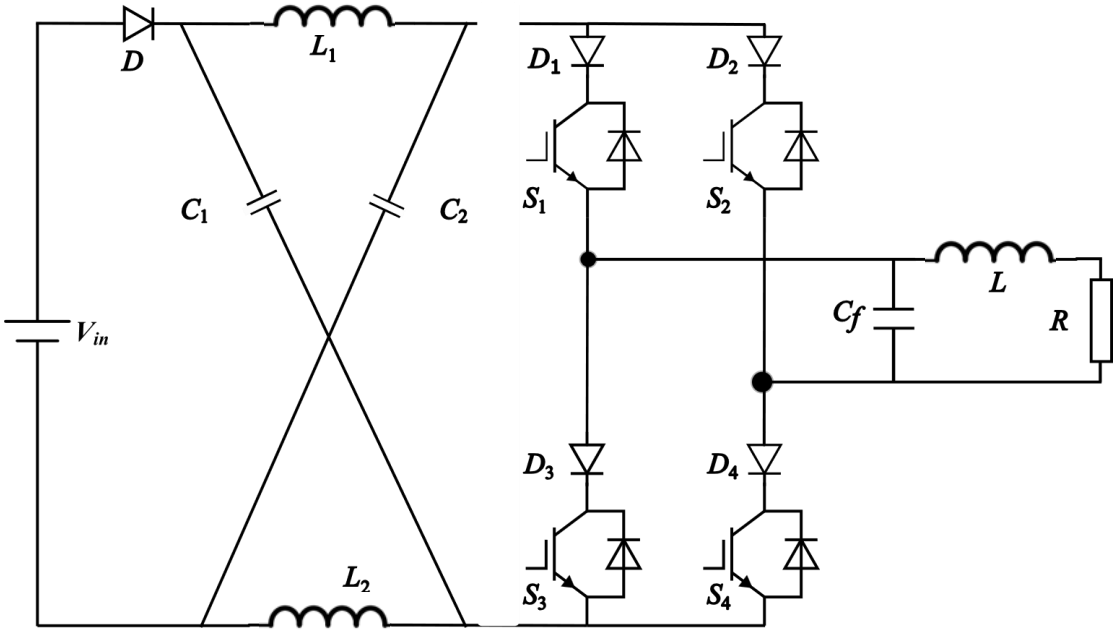


Fig. 1 - 3 Z-source three-level CSI

The operation principle of Z-source CSI can be separated in two modes, non-shoot-through switching state and shoot-through zero state, as shown in Fig. 1-4. The non-shoot-through switching state includes non-shoot-through active states (S_1, S_4 or S_2, S_3 conducting) and conventional freewheeling zero states (S_1, S_3 or S_2, S_4 conducting). During these states, the front-end diode (D) remains forward-biased, allowing the dc source and impedance inductors (L_1 and L_2) to supply current through the inverter bridge while charging the Z-network capacitors (C_1 and C_2). Conversely, during the shoot-through zero state, an open-circuit condition is deliberately created across the dc terminals of the bridge by turning off upper switches (S_1 and S_2) or lower switches (S_3 and S_4), or all four switches. The open circuit forces the front-end diode (D) into reverse bias, causing the Z-capacitors to discharge into the inductors and store energy in their magnetic fields.



(a) Non-shoot-through switching state



(b) Shoot-through zero state

Fig. 1 - 4 Equivalent circuit of the Z-source inverter

The modulation scheme of the Z-source inverter extends conventional PWM schemes by maintaining standard switches on and off once per switching cycle, thereby preserving the fundamental ac output performance. By strategically replacing a portion

of the conventional zero states with shoot-through zero states, the total active state duration remains untouched while enabling dc link voltage boosting. By applying inductor volt-second balance over a switching period T, the peak dc-link current boost factor is derived as $B = 1/(1-2D_{st})$, where D_{st} represents the shoot-through duty ratio, thereby achieving flexible buck-boost power conversion and inherent open-circuit fault protection.

Furthermore, due to the distribution of shoot-through zero states within each switching cycle, the equivalent ripple frequency experienced by the Z-source network becomes three times the fundamental switching frequency of the main inverter ($f_{eq} = 3f_{sw}$). This elevated equivalent operating frequency significantly reduces the AC volt-second burden on the inductors, thereby allowing a reduction in the required Z-source inductance L.

The single-phase Z-source three-level CSI presents significant advantages over conventional CSIs by providing single-stage buck-boost capability, inherent open-circuit fault protection, and reduced inductance. Despite these structural and functional improvements, the Z-source three-level CSI still inherits critical hardware limitations inherent to three level architectures. The three three-level CSI is limited to three discrete output current levels, resulting in relatively higher harmonic distortion. By increasing the number of current levels, five-level CSIs can achieve improved output current quality and lower THD under comparable modulation and switching conditions.

1.2 Single-Phase Five-Level Current Source Inverters

The single-phase five-level CSI has emerged as a compelling evolution over three-level CSI for medium-to-high power applications. While a standard 3L-CSI synthesizes an ac output current using only three steps ($+I_{dc}$, 0, $-I_{dc}$), the 5L-CSI introduces five current levels ($+2I_{dc}$, $+I_{dc}$, 0, $-I_{dc}$, $-2I_{dc}$). The multi-step synthesis produces a smoother, near-sinusoidal output waveform, substantially lowering THD. Based on their structural current-synthesis mechanisms, single-phase five-level CSIs are classified

into multi-source topologies and single-source topologies.

1.2.1 Multi-Source Five-Level CSI

Multi-source five-level CSIs synthesize five-level current waveforms by combining the output currents of multiple standard three-level H-bridge units.

1.2.1.1 Parallel-Connected H-bridge Five-Level CSI

A single-phase conventional parallel H-bridge five-level CSI is shown in Fig. 1-5. The inverter is composed of two identical conventional H-bridge three-level CSI as mentioned before. The output ac current i_s is synthesized through the instantaneous current summation of the two parallel bridges at the ac output.

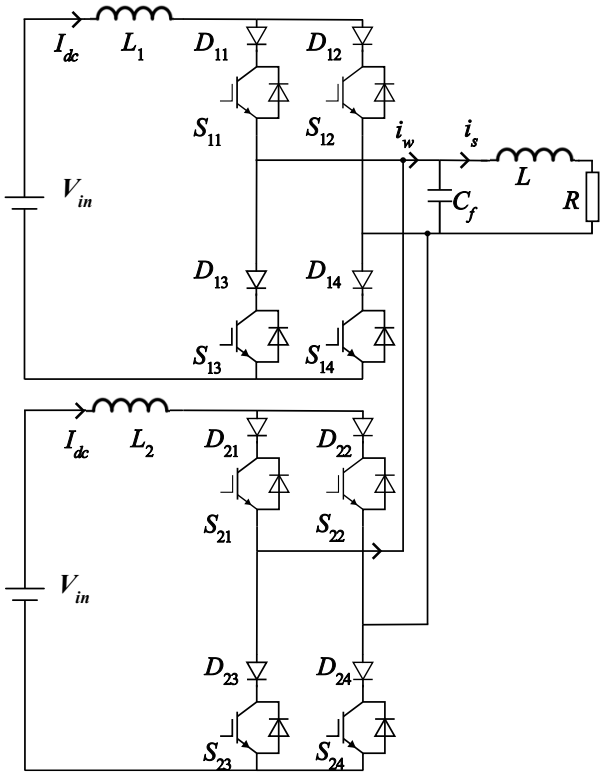
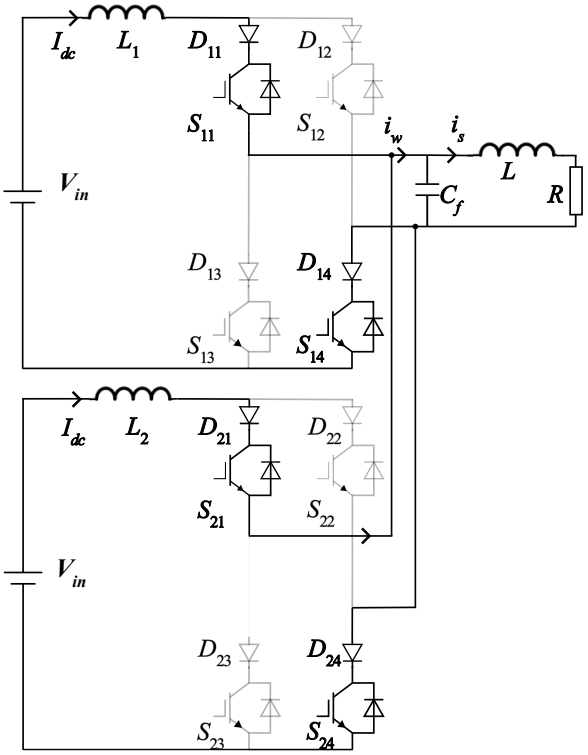


Fig. 1 - 5 Conventional parallel-connected H-bridge five-level CSI

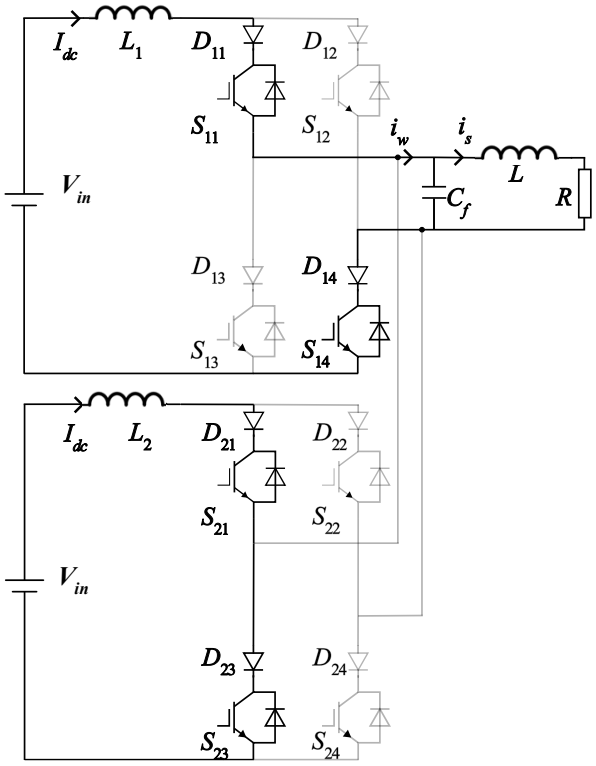
As shown in Fig. 1-6, the operation of the parallel-connected H-bridge five-level CSI relies on two identical and isolated dc voltage source, each supplying an input current of I_{dc} through its dedicated dc link inductor, to feed two standard H-bridge

inverters connected in parallel. Driven by phase-shifted carrier PWM with a 180º phase shift between the carrier signals of the two bridges, each individual bridge generates a standard three-level current waveform (+I_{dc}, 0, -I_{dc}). At the ac output node, the instantaneous currents from both bridges are directly summed, synthesizing a five-level current waveform. By alternating the switching states of the two bridges, the total load current is stepped through five levels (+2I_{dc}, +I_{dc}, 0, -I_{dc}, -2I_{dc}).



(a) $i_w = 2I_{dc}$

(b) $i_w = I_{dc}$



(c) $i_w = 0$

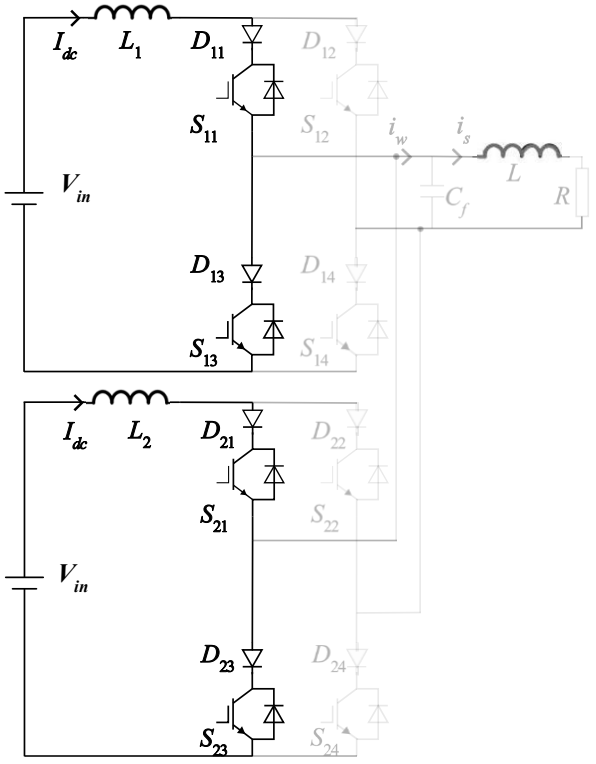


Fig. 1 - 6 Equivalent circuits of the parallel-connected H-bridge five-level CSI

The benefits of conventional parallel-connected H-bridge five-level CSI are reduced THD and lower switch current stress. Because the total load current is equally

split between the two parallel branches, the semiconductor switches in each H-bridge are subjected to only half of the peak output current, facilitating power scaling with lower-rated power devices.

However, it still has some limitations. First, it requires two isolated input source and two H-bridge inverters, increasing overall control and hardware complexity. Furthermore, it suffers from current imbalance issue due to system asymmetries, including unequal on-state voltages of the semiconductor devices, gating signal delays differences, and manufacturing tolerances in dc inductors. Consequently, additional current-balancing control schemes are required, leading to a more complex system and higher costs.

1.2.2 Single-Source Five-Level CSIs

Single-source five-level CSI have attracted considerable attention because they eliminate the need for multiple isolated dc source required by multi-source topologies. Compared with multi-source inverters, single-source configurations offer a simpler power supply structure, and reduced system size, making them more suitable for practical applications. To achieve five-level current generation from a single dc source, additional energy-storage components and auxiliary switching circuits are generally introduced. This section categorizes single-source five-level CSI into two main topological: single-rating inductor five-level CSI and auxiliary switches five-level CSIs (X-type five-level CSI), analyzing their circuit configurations, operating modes, advantages and challenges.

1.2.2.1 Single-Rating Inductor Five-Level CSI

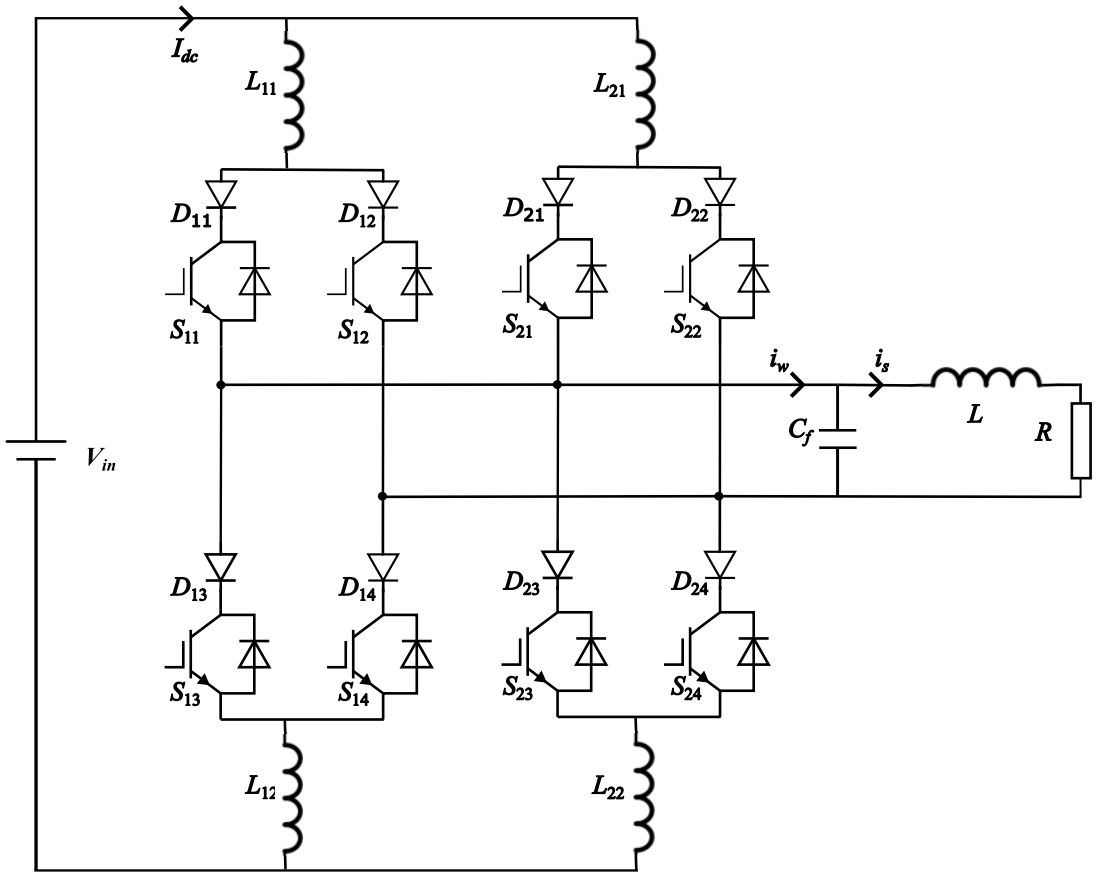


Fig. 1 - 7 Single-rating inductor five-level CSI

As shown in Fig. 1-7, the single-rating inductor five-level CSI is a single-phase, single-source symmetric topology designed to synthesize a five-level ac output current. It has four same current rating inductors, where the top inductors (L_{11} and L_{12}) and bottom inductors (L_{21} and L_{22}) are connected to the dc side. Two inverter bridges are the same as the parallel H-bridge CSI, using reverse-blocking voltage switches.

The primary objective of the single-rating inductor inverter is to divide the total dc current (I_{dc}) into two equal parallel branch streams ($0.5I_{dc}$) and synthesize five output current levels ($+I_{dc}$, $+0.5I_{dc}$, 0, $-0.5I_{dc}$, $-I_{dc}$). For example, when both H-bridges operate in positive conduction mode, the output PWM current sums the two branch currents to produce a maximum positive level of $+I_{dc}$. When one H-bridge conducts in the positive direction while the other switches to freewheeling state, the output PWM steps down to $+0.5I_{dc}$.

By utilizing a single dc source, this topology eliminates the need for multiple power sources, thereby reducing the system size and overall cost. Furthermore, because the four inductors are of the same current rating, contributing to the reduction of the current ripples. However, due to the parasitic parameters in the system, the inductor currents still become imbalanced. To overcome this limit, researchers introduced auxiliary switches five-level CSIs.

1.2.2.2 X-Type Five-Level CSI

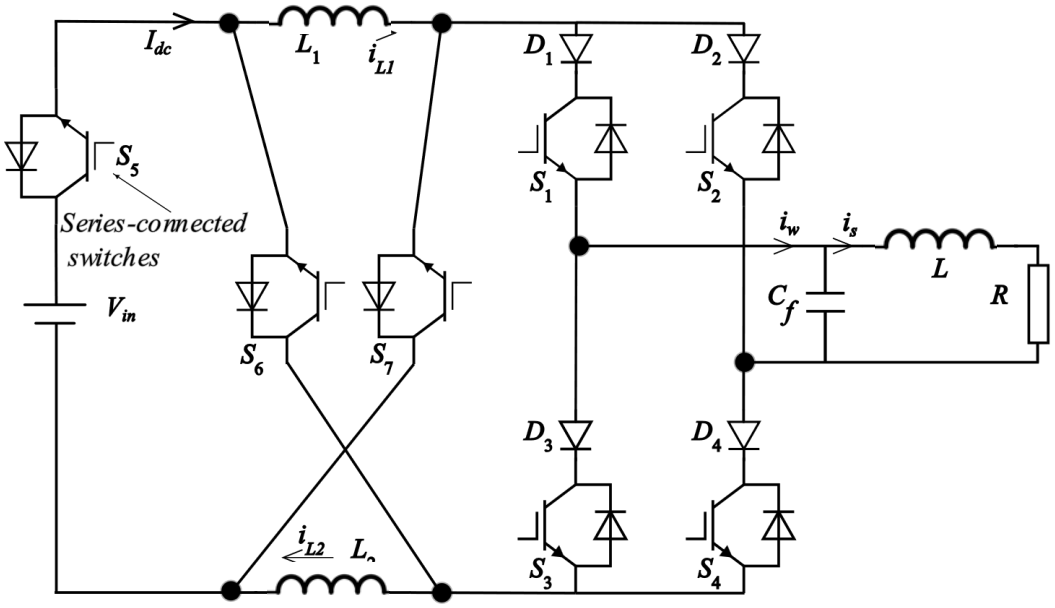
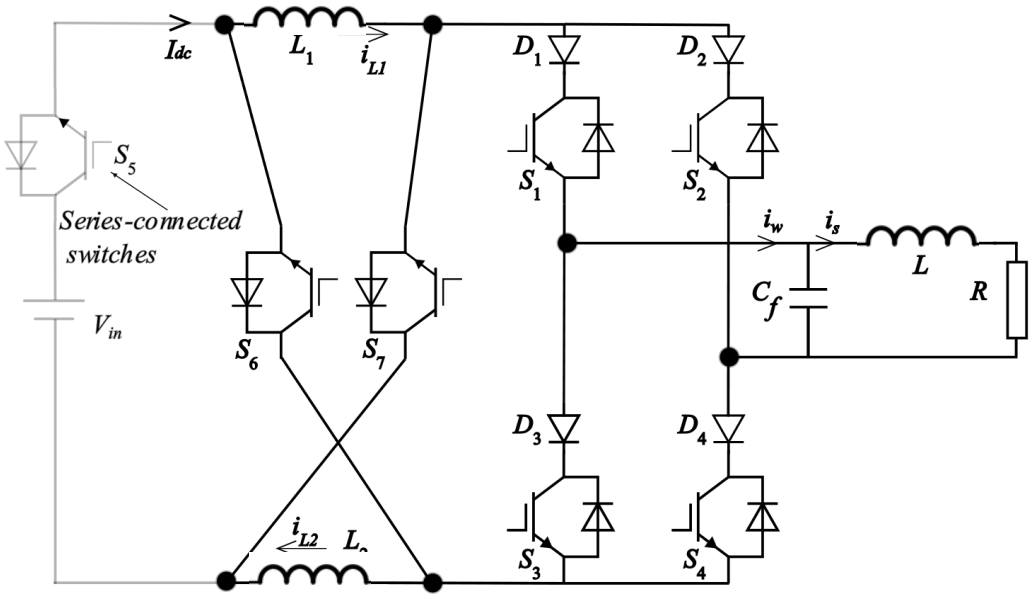


Fig. 1 - 8 X-type five-level CSI

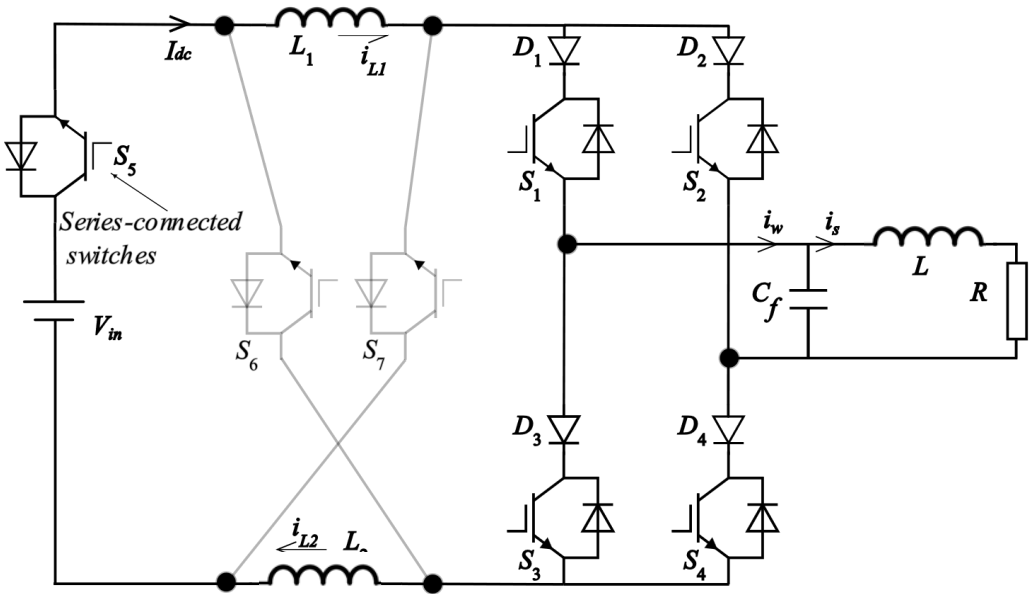
The single-source X-type five-level CSI was introduced to achieve inherent current balancing, thereby eliminating the need for complex balancing control schemes. As shown in Fig. 1-8, this topology consists of an H-bridge CSI (S_1, S_2, S_3, and S_4), the auxiliary switches (S_5, S_6, and S_7), inductors L_1 and L_2. The H-bridge of inverter also use these switches (S_1-S_4) with reverse voltage blocking capabilities [36].

The operation principle of X-type five-level CSI has two modes: mode 1 and mode 2, as shown in Fig. 1-9. Under mode 1, the series-connected auxiliary switches S_5 are turned off, while switches S_6 and S_7 are turned on. This connects the two dc inductors in parallel, combining their currents (I_{dc}) to synthesize an output PWM current of i_w =

$2I_{dc}$. In mode 2, auxiliary switches S_5 are on, whereas switches S_6 and S_7 are off. Consequently, the two dc inductors operate in series, enforcing their currents to be equal (I_{dc}). Therefore, the output PWM current i_w can achieve 5 levels. Due to the operation in mode 2, the series-connected inductors to achieve inductor current balancing.



(a) Mode 1



(b) Mode 2

Fig. 1 - 9 Operation principle of the auxiliary switches X-type five-level CSI

The dc inductors are essential for sustaining the operational modes of the X-type inverter, and their sizing directly determines dc current ripple. But, during mode 1, the X-type CSI disconnects the input source from the dc inductors causing the inductors

to operate as independent current sources. During this interval, the inductors must sustain the dc-link current by themselves, and the resulting current variation is determined primarily by the inductance and the duration of this operating state. Therefore, the X-type CSI requires a relatively large dc-link inductance to maintain the desired current continuity and limit the current ripple.

The peak voltage across the H-bridge switches (S_1-S_4) is equal to the peak capacitor voltage V_{C_peak}. Based on KVL analysis of the corresponding operating states, the peak voltage stress across switch S_5 is given by $V_{in}+V_{C\_peak}$, while the peak voltage stress across switches S_6 and S_7 is $0.5(V_{in}+V_{C\_peak})$. Therefore, the dc side switches, particularly S_5, are subjected to significantly higher voltage stresses than the H-bridge switches. Therefore, series-connected switches in dc side are required to share the voltage stress.

Consequently, the larger dc-link inductance and additional series-connected dc-side switches increase the component count, hardware cost, and associated power losses of the X-type CSI. Consequently, these additional passive and semiconductor losses contribute to a lower overall system efficiency.

In summary, the X-type five-level CSI provides inherent dc-link inductor current self-balancing without an additional balancing control scheme. However, this advantage comes at the cost of a larger required dc-link inductance and series-connected dc-side switches. These limitations increase the topology cost and power losses, thereby reducing the overall system efficiency.

1.3 Single-Phase Seven-Level Current Source Inverters

Single-phase seven-level CSIs have been proposed to further improve the output current quality beyond five-level topologies. Most existing seven-level CSIs are developed by extending existing multilevel current-source structures with additional switching cells or cascaded inverter modules. By increasing the number of output current levels, these topologies are able to generate a current waveform that more

closely a sinusoidal waveform [37-40].

The operating principle of a seven-level CSI is similar to that of other multilevel CSIs. By appropriately controlling the switching states, the output current is synthesized from several discrete current levels. The additional current levels provide smoother current transitions and lower output current ripple. Appropriate PWM strategies and commutation control are required to ensure safe current transfer during switching transitions.

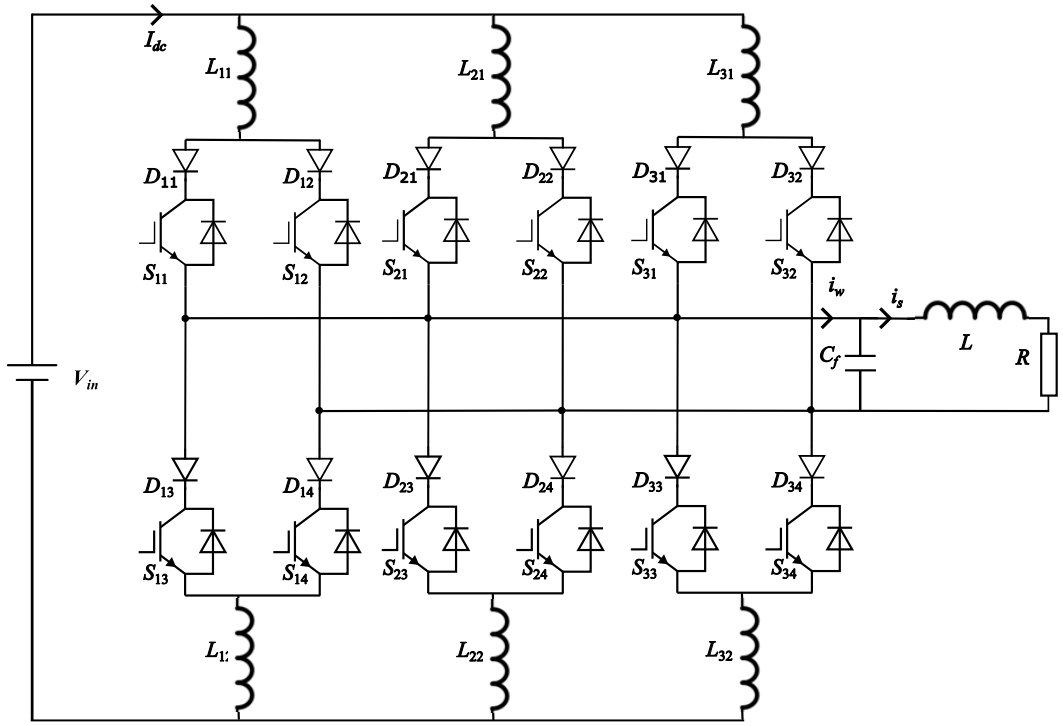


Fig. 1 - 10 Single-phase seven-level CSI

Compared with three-level and five-level CSIs, seven-level topologies provide lower THD and improved output current quality. The increased number of current levels reduces the output current ripple and the filter requirement.

Despite these advantages, seven-level CSIs also have several limitations. First, the increased number of semiconductor devices, gate driver circuits, and passive components results in higher inverter cost, larger physical size, and increased conduction losses. Second, the larger number of switching states increases the complexity of modulation and overlap-time commutation control. As a result, the

improvement in harmonic performance is achieved at the expense of increased circuit complexity and implementation cost.

Therefore, recent research has focused on improving five-level CSIs, aiming to achieve a better balance between harmonic performance, inverter efficiency, implementation cost, and system reliability. This trend motivates the development of the proposed H-type five-level CSI presented in this paper.

1.4 Research Gap and Research Objectives

This chapter reviewed the development of single-phase multilevel PWM current source inverters, including three-level, five-level, and seven-level topologies. The characteristics, operating principles, advantages, and limitations of representative topologies were discussed. The evolution of multilevel CSIs demonstrates that increasing the number of output current levels effectively improves output current quality and reduces harmonic distortion.

The literature review shows that five-level CSIs provide a better balance between harmonic performance, circuit complexity, and implementation cost than both three-level, multi-source and seven-level inverters. Multi-source five-level inverters require multiple isolated dc current sources, while existing single-source five-level inverters generally require additional switching circuits or passive components, leading to increased circuit complexity and control requirements.

Based on the literature review, although existing auxiliary-switch X-type CSI can achieve inductor current balancing, they still require a large dc inductor. A new converter will be proposed to address the problem of the large dc inductance, while retaining the inherent dc inductor current self-balancing capability.

Chapter 2 Proposed Single-Phase H-type Five-Level Current Source Inverter

Based on the literature review presented in Chapter 1, single-source five-level current source inverters provide a better trade-off between output current quality, circuit complexity, and implementation cost than both three-level and seven-level topologies. Although existing single-source five-level CSIs have addressed several limitations of conventional multilevel inverters, they still rely on a relatively large dc inductor and series-connected power switches. To overcome these limitations, a novel single-phase H-type five-level current source inverter is presented in this chapter. The proposed topology achieves inherent dc-link inductor current self-balancing, reduces the required dc inductance, and eliminates the need for series-connected switches.

This chapter first presents the inverter topology and operating principle, followed by the modulation scheme and passive component design. The inherent inductor current self-balancing mechanism, switch voltage stresses, and converter efficiency are then analyzed. Finally, a comparison with existing five-level CSIs is provided, and the effectiveness of the proposed inverter is validated through simulation and experimental results [41].

2.1 Technical Challenges of X-type CSI

The X-type CSI retains the main advantages of conventional five-level CSIs, and it features an inherent DC-inductor self-balancing capability, which prevents inductor current mismatch and simplifies active control. These features make it the most relevant baseline for performance comparison. However, the X-type CSI has two major limitations: require Large DC Inductance and need Series-Connected DC Switches, as shown in Fig. 2-1. These structural drawbacks increase component cost, overall volume, and conduction losses, ultimately lowering system efficiency.

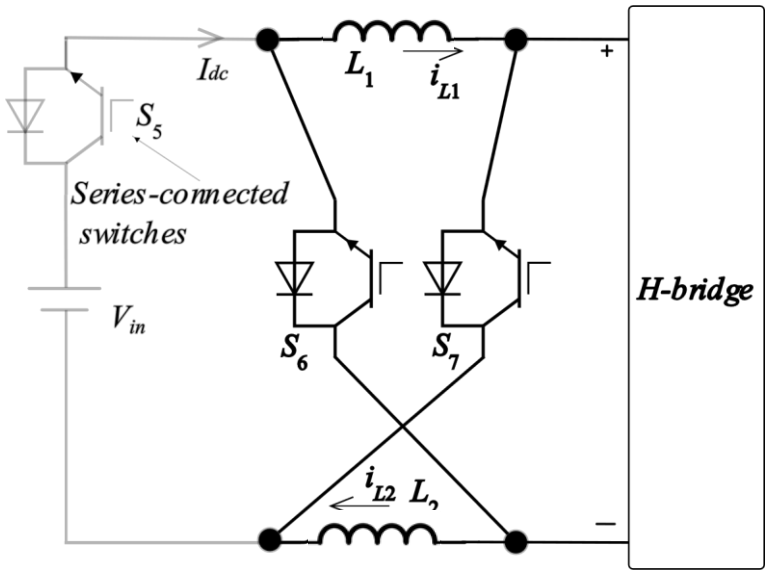


Fig. 2 - 1 Equivalent circuit of the X-type CSI

To overcomes these limitations while retaining the inherent dc inductor current self-balancing capability of the X-type topology, a new single-phase five-level is proposed in this chapter.

2.2 Inverter Topology and Operation Principle

Fig. 2-2 illustrates the proposed single-phase H-type five-level CSI. The inverter consists of three main parts: the dc-side auxiliary switching network, the H-bridge inverter, and the ac output filter. On the dc side, the auxiliary network is composed of three auxiliary switches (S_5, S_6, and S_7), a diode (D) and two inductors (L_1 and L_2). As the main energy storage element, inductors maintain continuous input current (I_{dc}). Switches S_5-S_7 require forward voltage blocking capability, realized using IGBTs or MOSFETs, to establish the two variable dc current levels.

Switches S_1-S_4 are configured as a conventional H-bridge CSI, utilizing switches with reverse voltage blocking capability, such as symmetric gate-commutated thyristors (SGCTs) or insulated-gate bipolar transistors (IGBTs) connected in series with a diode.

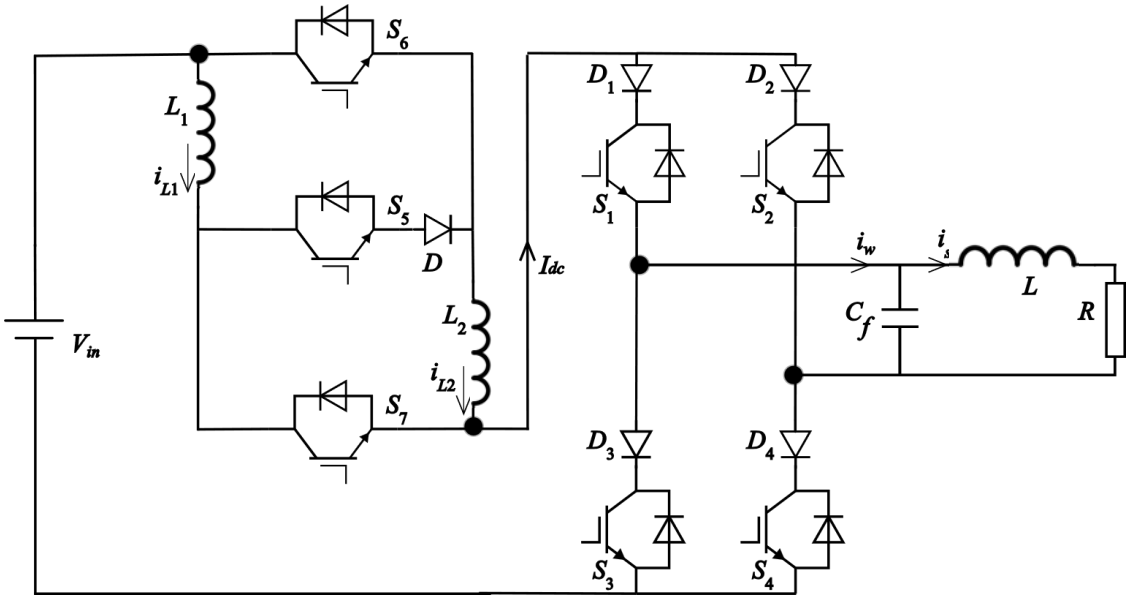
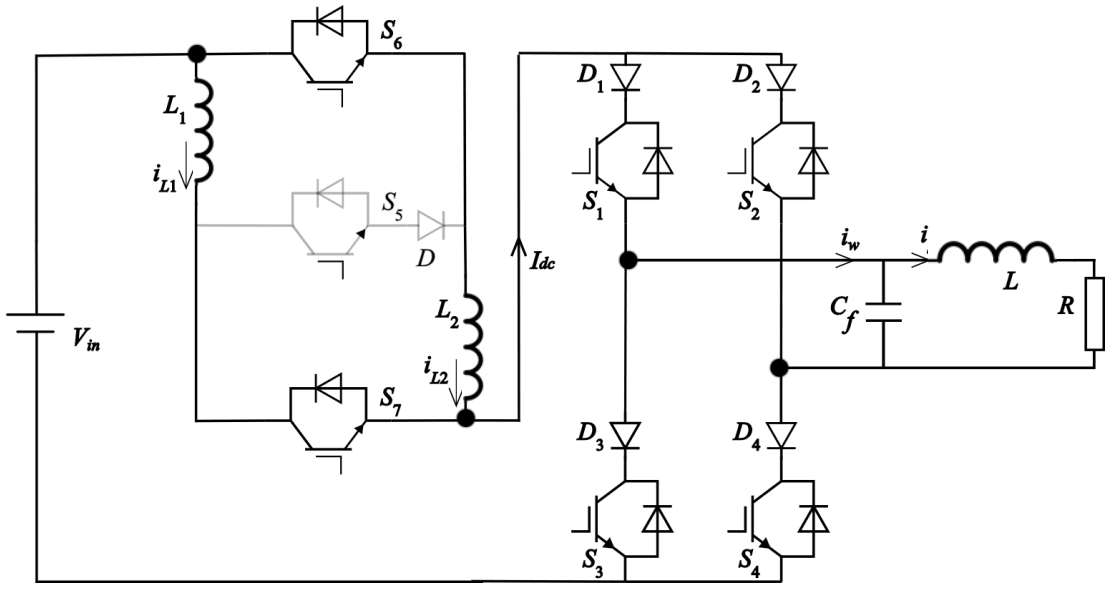
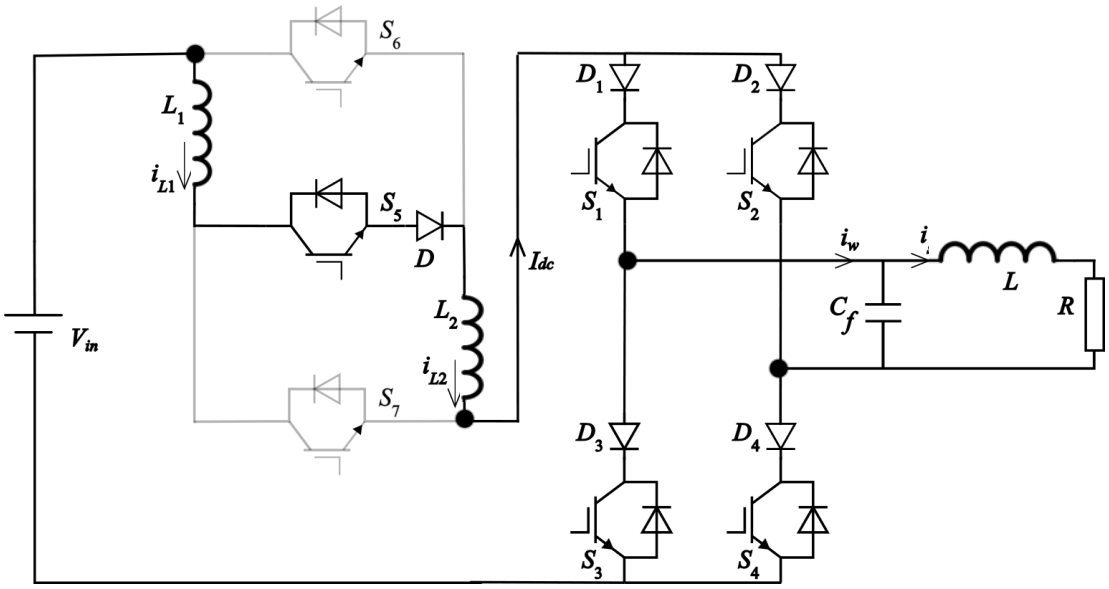


Fig. 2 - 2 Proposed single-phase H-type five-level CSI

Mode 1: As shown in Fig. 2-3 (a), S_6 and S_7 are activated while S_5 is deactivated. Inductors L_1 and L_2 are identical and they are parallel connected. The currents flowing through both inductors are identical ($I_{L1} = I_{L2} = 0.5I_L$), and their combination forms the input current of H-bridge CSI ($I_{dc} = 2I_L$). The output PWM current of this mode has three levels: $2I_L$, 0 and $-2I_L$.



(a) mode 1



(b) mode 2

Fig. 2 - 3 Operation principle of proposed H-type CSI

Mode 2: As shown in Fig. 2-3 (b), switches S_6 and S_7 are deactivated, and S_5 is activated. Inductors L_1 and L_2 are configured in series to enforce the two inductor currents to be equal ($I_{L1} = I_{L2} = I_{dc}$), thereby achieving inherent current balance. The output PWM current. The output PWM current of this mode has three levels: I_L, 0 and $-I_L$.

Due to the series-connected of two inductors in *Mode* 2, the inherent inductor current balancing is established. The inverter achieves a five-level output current by alternating between operation modes. For example, when switches S_1, S_4, S_6 and S_7 are turned on, the output current i_w is equal to $2I_L$. And when switches S_1, S_4, and S_5 are turned on, the output current i_w is equal to I_L. Table 2-1 provides the switching states and corresponding output PWM currents.

2.2 Modulation Scheme

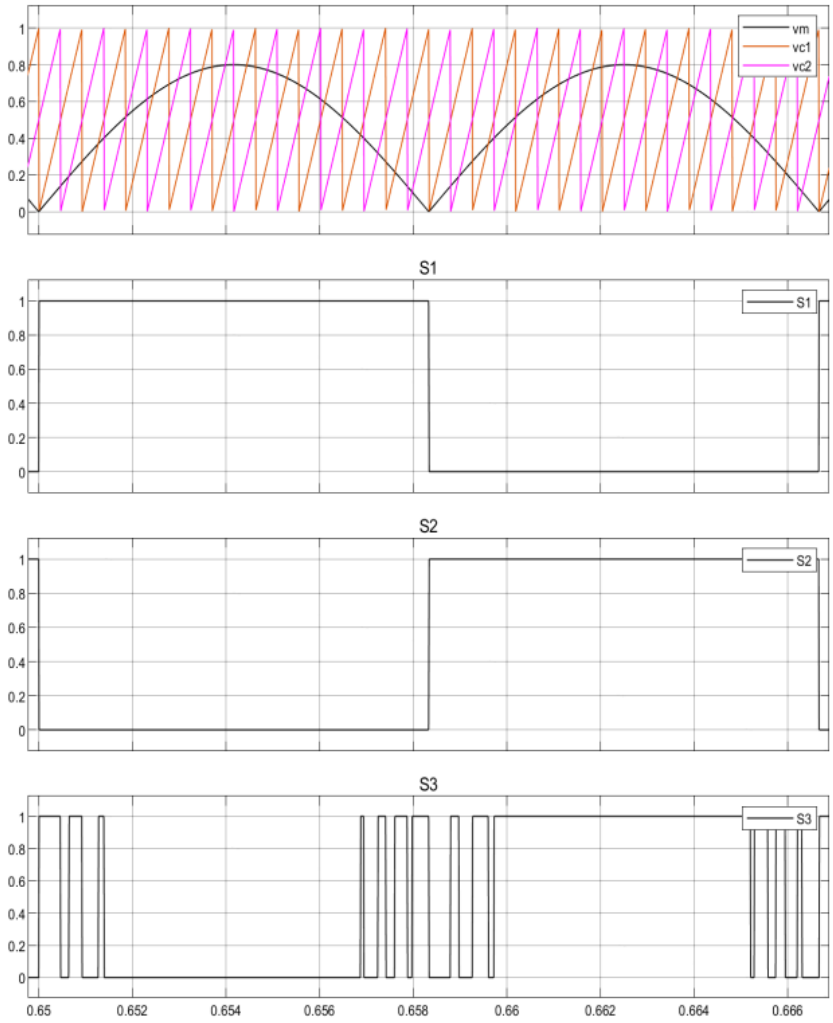
The switching pattern design for the CSI satisfies two conditions: (a) the dc current I_{dc} should be continuous, and (b) the inverter PWM current i_w should be defined [1]. According to this, the switching states and corresponding output PWM currents are designed as shown in table 2-1. The 7 switches are divided into three complementary

groups: S_1 and S_2; S_3 and S_4; S_5 and S_6/S_7.

Table 2 - 1 Output PWM current level and switches states

Switching states						Output PWM Current i_w
H-bridge				DC side switches		
S_1	S_2	S_3	S_4	S_5	S_6/S_7	
1	0	1	0	1	0	0
0	1	0	1	1	0	0
1	0	0	1	1	0	I_L
				0	1	$2I_L$
0	1	1	0	1	0	$-I_L$
				0	1	$-2I_L$

The principle of the phase-shifting sinusoidal pulse-width modulation (SPWM) scheme for proposed inverter is illustrated in Fig. 2-4, where v_m is a sinusoidal modulating waveform, v_{c1} and v_{c2} are sawtooth carrier waves with the same frequency and peak amplitude, but phase shift of 180º. In the proposed modulation scheme, a 60 Hz fundamental reference wave and two 1080 Hz sawtooth carriers (frequency ratio N = 18) were selected. The carrier ratio of N = 18 provides an optimal trade-off between semiconductor switching losses and AC output harmonic performance. Moreover, due to the 180º phase shift between the carriers, the effective output switching frequency is doubled to 2160 Hz, which significantly attenuates low-order harmonics and reduces the required AC filter size while keeping individual switch thermal stress low.


vm
vc1
vc2
S1
S1
S2
S2
S3
S3
0.65
0.652
0.654
0.656
0.658
0.66
0.662
0.664
0.666

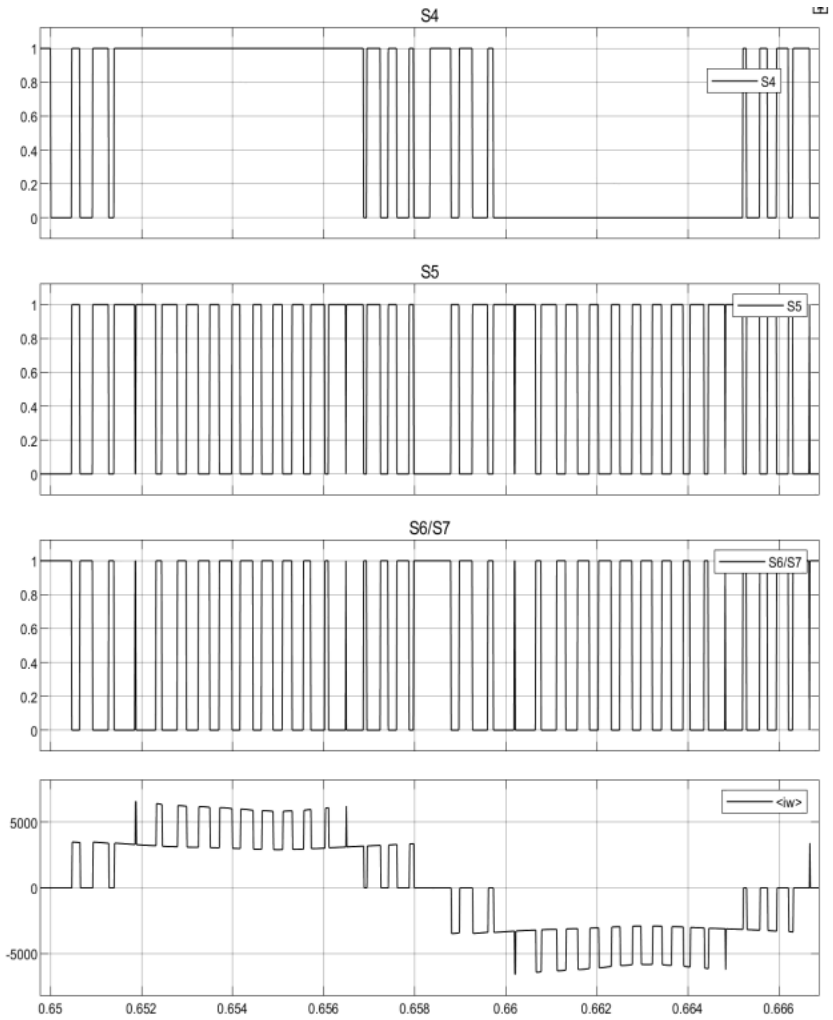


Fig. 2 - 4 Phase-shifting sinusoidal pulse-width modulation

The H-bridge switches S_1 and S_2 are modulated at the fundamental frequency. By comparing the sinusoidal waveform v_m with a zero-level threshold, S_1 remains active during the positive half-cycle, while S_2 is engaged during the negative half-cycle. By comparing v_m with v_{c1} and v_{c2}, the output PWM current level can be determined. Specifically, the output PWM current i_w is equal to $2I_L$ when v_m is greater than both v_{c1} and v_{c2}; it equals 0 when v_m is less than both carriers. When v_m lies within the interval bounded by v_{c1} and v_{c2}, the output current i_w is equal to I_L.

2.3 Passive Component Design

The sizing of passive components plays a crucial role in determining the power

density, efficiency, and transient response of the CSIs. This section will focus on the size of passive components in proposed H-type CSI.

DC Inductor Sizing: The dc inductors are essential for sustaining the operational modes of the proposed inverter, and their sizing directly determines dc current ripple. To maintain a smooth and continuous dc current (I_{dc}) with a ripple of less than a certain value (15%, for example), the minimum required inductance value (L_{dc}) is shown in Equation (2-1):

$$L_{dc} = \frac{V_{L\_max}\Delta t}{15\% I_{dc}} \tag{2-1}$$

where V_{L_max} means the maximum voltage across the inductor, and Δt represents the corresponding dwell times.

The output current of the H-type CSIs features a five-level waveform when the modulation index $m_a > 0.5$, which is limited to three-level when $m_a \leq 0.5$. To investigate the optimal operating range of the proposed five-level inverter, the required dc inductance L_{dc} under different modulation index ($m_a > 0.5$) is calculated and verified through simulations. The minimum L_{dc} required by the proposed H-type CSI shows a linear increase with m_a, peaking at 4.3 per unit when $m_a = 1$. The H-type CSI remains a continuous connection to the input source, eliminating the need for its dc inductors to discharge and function as independent current sources during all operation modes.

AC Output Filter Sizing: The ac output LC filter absorbs high-frequency switching harmonics produced by the PWM current waveform (i_w) to supply a clean sinusoidal current (i_s) to the load. The capacitor (C_f) provides a path for switching ripple current. C_f must be large enough to filter high-frequency switching noise, yet small enough to avoid drawing excessive reactive current at the fundamental frequency(f_1). To avoid excessive fundamental reactive power drawn by the filter capacitor, C_f is sized as below equation 2-2,

$$C_f \leq \frac{\alpha \cdot P_n}{2\pi f_1 V_{s,rms}^2} \tag{2-2}$$

Where P_n is the rated power of the inverter, $V_{s,rms}$ is the rms value of the fundamental

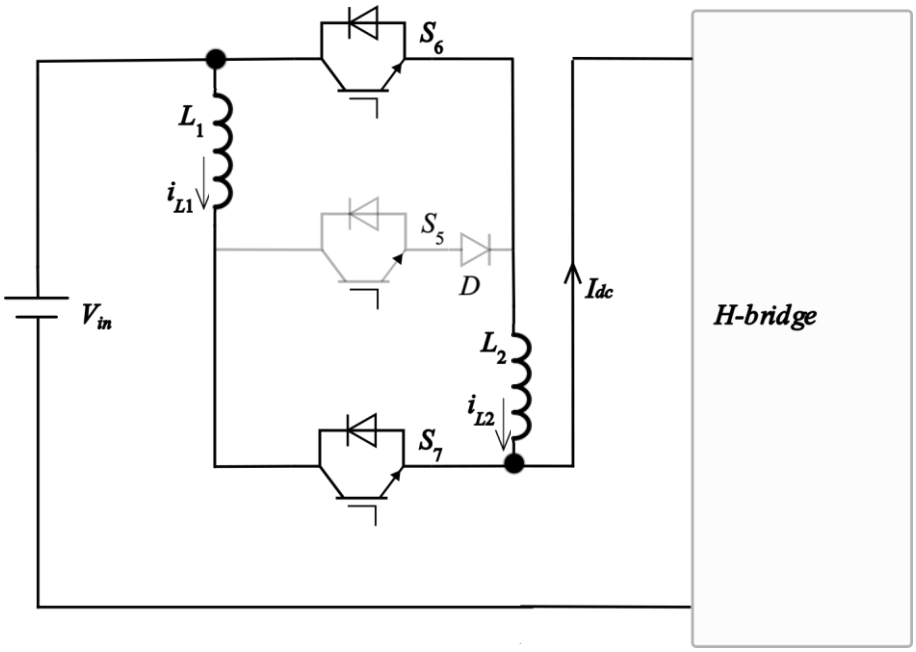
output voltage, and α is the reactive power constraint factor (typically set to $\alpha \leq 5\% \sim 10\%$).

The filter inductor (L_f) smooths out the ac load current (i_s). Once C_f is selected, the L_f is designed based on the desired cutoff frequency (f_c) of the second-order LC filter, which is chosen well above the fundamental frequency (f_1) and well below the switching frequency (f_{sw}).

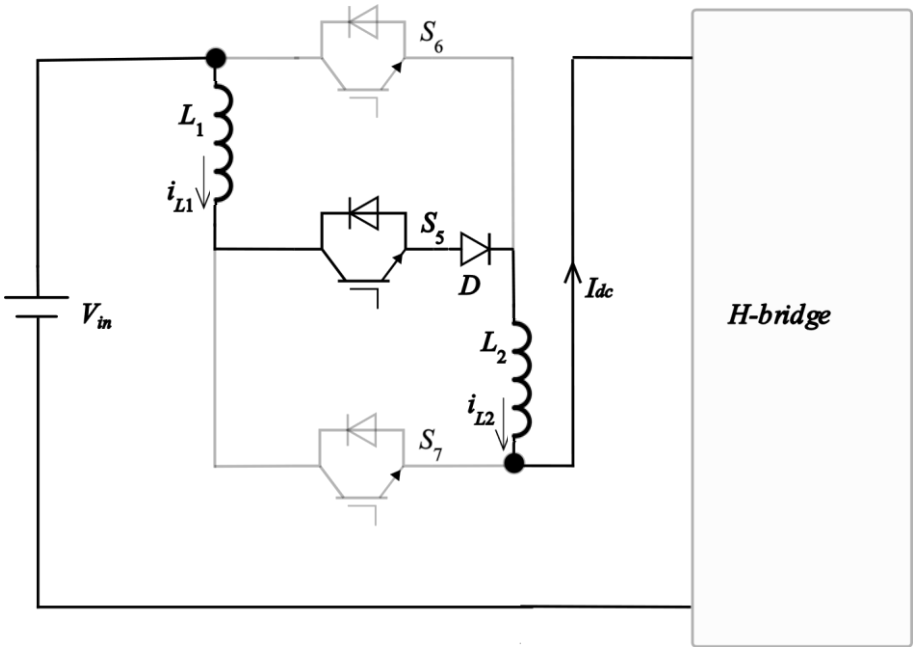
$$f_1 \ll f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \ll f_{sw} \tag{2-3}$$

To ensure power quality compliance at the grid interface, the output LC filter parameters derived above are selected to strictly fulfil international grid codes, such as IEEE std 519-2022. Specially, the primary design target requires the THD of the output current i_s to remain below 5%.

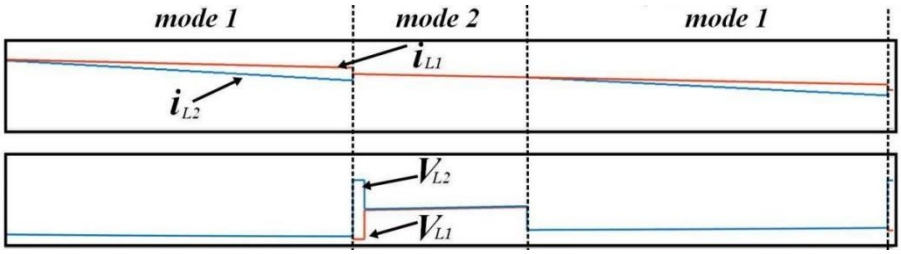
2.4 Inductor Self-balancing



(a) Mode 1



(b) Mode 2



(c) Inductor self-balancing

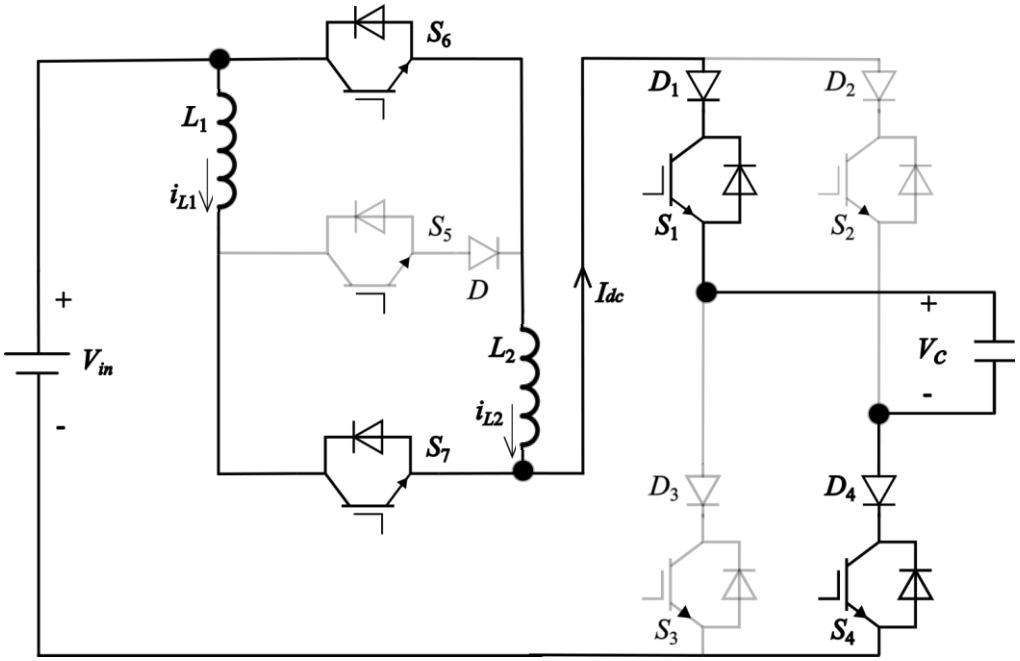
Fig. 2 - 5 Inductor current and voltage self-balancing

In practical applications, manufacturing tolerances inevitably lead to parameter mismatches between the two dc inductors (L_1 and L_2). As shown in Fig. 2-5, during mode 1, L_1 and L_2 are connected in parallel, resulting in equal inductor voltage ($V_{L2} = V_{L1}$,). And these parameter mismatches tend to cause an imbalance between the inductor currents i_{L1} and i_{L2}. Upon transition into mode 2, L_1 and L_2 are configured in series, forcing i_{L1} and i_{L2} to remain equal. This periodic series-connection mode inherently guarantees the self-balancing capability of the dc inductor currents without requiring active balancing controls.

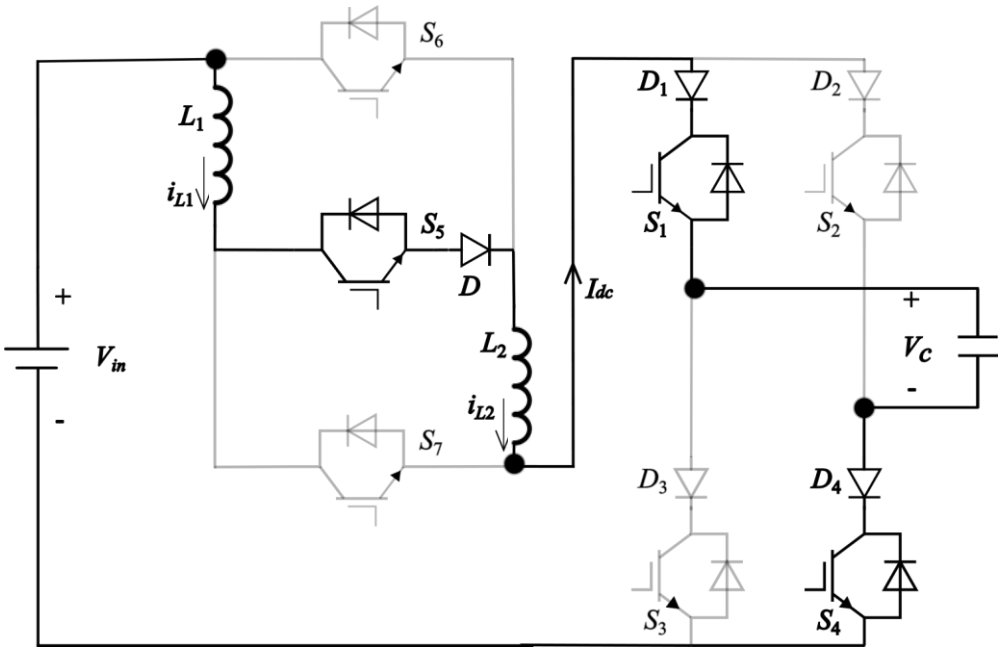
During mode transitions, the near-instantaneous switching action usually induces high d_i/d_t rates, which can potentially cause severe voltage spikes across the inductors.

In the proposed inverter, this over-voltage is suppressed by the anti-parallel diodes integrated within S_7 and S_9. As a result, the proposed inverter eliminates the need for auxiliary voltage-clamping circuits or oversized semiconductor devices, ensuring high power density and enhanced reliability.

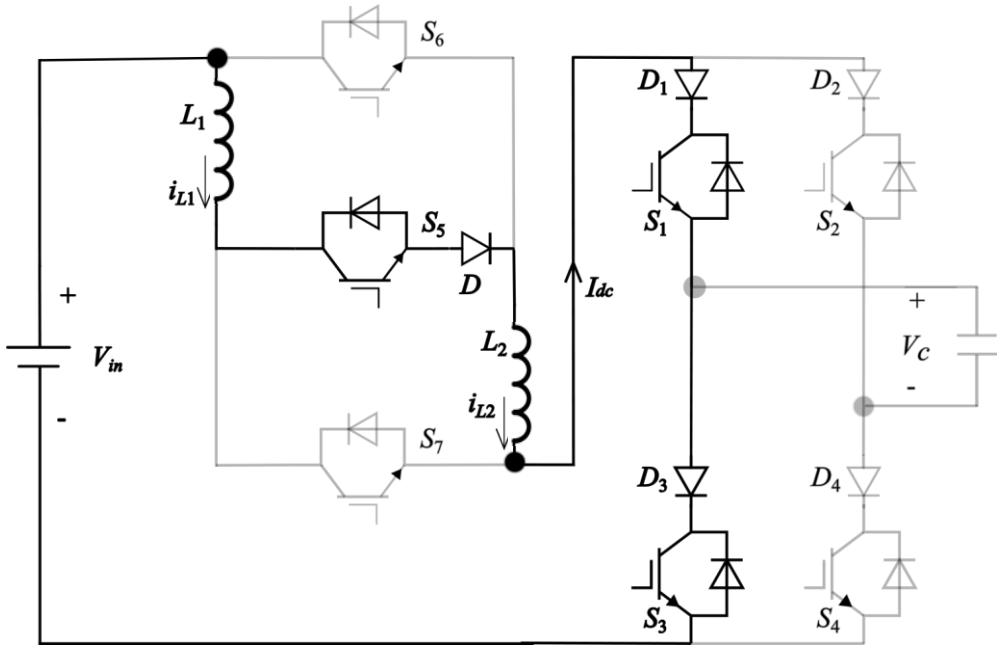
2.5 Switch Voltage Stresses



(a) Mode 1 of the H-type CSI



(b) Mode 2 of the H-type CSI



(c) Freewheeling state

Fig. 2 - 6 Equivalent circuit of the H-type CSI

The peak voltage stresses of the H-type are summarized in Table 2-2. In the proposed H-type CSI shown in Fig. 2-6, the peak voltage across the H-bridge switches

(S_1-S_4) is equal to the peak capacitor voltage V_{C_peak}. The voltage stresses of the auxiliary switches S_5-S_7 are determined based on the corresponding operating states.

In More 1, the H-bridge operates in an active state, where either S_1 and S_4 or S_1 and S_4 are turned on depending on the output current direction. In this mode, S_5 is turned off, while S_6 and S_7 are turned on. Applying KVL to the corresponding circuit gives the peak voltage stress across switch S_5 is V_{C_peak}-V_{in}.

Table 2 - 2 Switch peak voltage of the H-type CSI

$V_{S1\text{-}S4\_peak}$	V_{C_peak}
V_{S5_peak}	V_{C_peak}-V_{in}
$V_{S6\text{-}S7\_peak}$	max {0.5(V_{C_peak}-V_{in}), 0.5(V_{in})}

In more 2, the H-bridge remains in the active state, while S_5 is turned on and S_6 and S_7 are turned off. From the corresponding KVL relationship, the peak voltage stresses across switch S_6 and S_7 are 0.5(V_{C_peak}-V_{in}).

During the freewheeling state, the H-bridge is bypassed. For example, S_1 and S_3 are turned on while S_2 and S_4 are turned off. In this state, the peak voltage stress across switches S_6 and S_7 are 0.5(V_{in}).

So, the dc side switches in the H-type CSI always experience lower voltage stresses than the CSI side switches, making the series connection of DC switches unnecessary. Nominally, the H-type CSI requires 7 switches and 5 diodes. In summary, this structural advantage of the proposed H-type CSI eliminates the need of series-connected switches, which ultimately reduces the total switch count, switching losses, lowers hardware costs.

2.6 System Efficiency

Power losses in the CSI topology arise from the semiconductor devices and the inductors. The semiconductor loss of the converter is dominated by the conduction losses and switching losses of the active switches and diodes. The inductor loss can be broken down into two components: core loss and copper loss.

2.6.1 Semiconductor Loss

The semiconductor losses consist of conduction loss and switching loss. The conduction loss is determined from the on-state voltage and current of each semiconductor device, while the switching loss is obtained from the turn-on and turn-off energy of the devices. Therefore, the total semiconductor loss can be expressed as

$$P_{semi} = P_{cond} + P_{sw} \tag{2-4}$$

Where P_{cond} and P_{sw} represent the total conduction and switching losses, respectively.

2.6.1.1 Conduction Loss

During the conduction state, each semiconductor device exhibits a nonzero on-state voltage. The conduction loss (P_{cond}) is therefore determined by the device voltage drop and the current flowing through the device. For the k-th semiconductor device, the average conduction loss can be expressed as

$$P_{cond,k} = \frac{1}{T}\int_0^T v_{on,k}(t) i_k(t) dt \tag{2-5}$$

Where $v_{on,k}$ and i_k are the on-state voltage and current of the k-th device, respectively, and T is the fundamental period.

The conduction loss of the IGBT and Diode can be expressed as

$$P_{cond,IGBT} = V_{CEO} I_{avg} + R_{CE} I^2_{rms} \tag{2-6}$$

$$P_{cond,Diode} = V_{FO} I_{avg} + R_F I^2_{rms} \tag{2-7}$$

Where V_{CEO} and V_{FO} are the threshold voltage component of IGBT and Diode, respectively. And R_{CE} and R_F are the equivalent on-state resistance of IGBT and Diode, respectively. I_{avg} and I_{rms} are the average and rms currents of the device, respectively. The total conduction loss of the inverter is obtained by summing the losses of all conducting semiconductor devices.

2.6.1.2 Switching Loss

Switching loss (P_{sw}) occurs during the turn-on and turn-off transitions of the semiconductor devices. During these transitions, the device simultaneously sustains voltage and carries current, resulting in energy dissipation.

For an IGBT, the switching energy of the device is given by

$$E_{sw} = E_{on} + E_{off} \tag{2-8}$$

Where E_{on} and E_{off} are the turn-on and turn-off energies, respectively.

The average switching loss is

$$P_{sw} = f_{sw}\,(E_{on} + E_{off}) \tag{2-9}$$

Where f_{sw} is the switching frequency.

For the diode, the switching loss is associated with reverse recovery during turn-off. The reverse-recovery energy can be represented by E_{rr}, and the average diode switching loss is

$$P_{sw\_diode} = f_{sw}\,E_{rr} \tag{2-10}$$

The switching energies specified in a datasheet are normally measured under specific test conditions. Therefore, these values should be scaled to the actual operating conditions of the inverter.

A simplified normalization can be expressed as

$$P_{sw\_IGBT} = f_{sw\_IGBT} \times (E_{on} + E_{off}) \times \frac{V}{V_{nom}} \times \frac{I}{I_{nom}} \tag{2-11}$$

$$P_{sw\_Diode} = f_{sw\_d} \times E_{rr} \times \frac{V}{V_{nom}} \tag{2-12}$$

Where f_{sw_IGBT} represents the switching frequency of the IGBT, whereas V_{nom} and I_{nom} indicate its rated voltage and current, respectively. E_{rr} represents the reverse-recovery energy, f_{sw_d} is the turn-off frequency of diode.

2.6.2 Inductor Loss

The dc-link inductor loss consists mainly of winding losses and core losses. The winding losses include dc winding losses and ac winding losses, while the core losses are associated with the magnetic flux variation in the inductor core. The magnitude of these losses depends on several factors, including the inductor current, winding resistance, winding geometry, operating frequency, and magnetic core material.

In a current source inverter, the dc-link inductor is an essential energy-storage component and normally carries a large dc current. Therefore, the dc winding loss can constitute a significant portion of the total inductor loss. This loss is mainly determined by the dc-link current and the dc resistance of the winding. The required inductance also affects the design of the magnetic component, particularly the number of turns and conductor length, which influence the winding resistance. In general, a larger required inductance leads to a greater number of turns and a longer conductor length, resulting in a higher dc resistance and increased copper loss. Therefore, reducing the required dc-link inductance can reduce the winding resistance and associated copper loss, provided that the other inductor design parameters remain comparable.

At $m_a = 1$, the proposed H-type CSI achieves an overall efficiency of 95.6%, with total power losses bounded at 4.4%, consisting of 2% dc inductor loss, 1.75% conduction loss, and just 0.65% switching loss.

2.7 Comparison

The proposed H-type five-level CSI is compared with the X-type five-level CSI in terms of the required dc-link inductance, semiconductor device count, and overall efficiency.

Comparison of DC Inductance Requirements:

Fig. 2-7 shows the minimum required dc inductance L_{dc} for the five-level CSIs operating under identical modulation and loading conditions. The minimum L_{dc} required by the proposed H-type CSI shows a linear increase with m_a, peaking at 4.3

per unit when m_a = 1. In comparison, the X-type CSI requires a significantly larger dc inductance of 15.5 p.u. at m_a = 1.

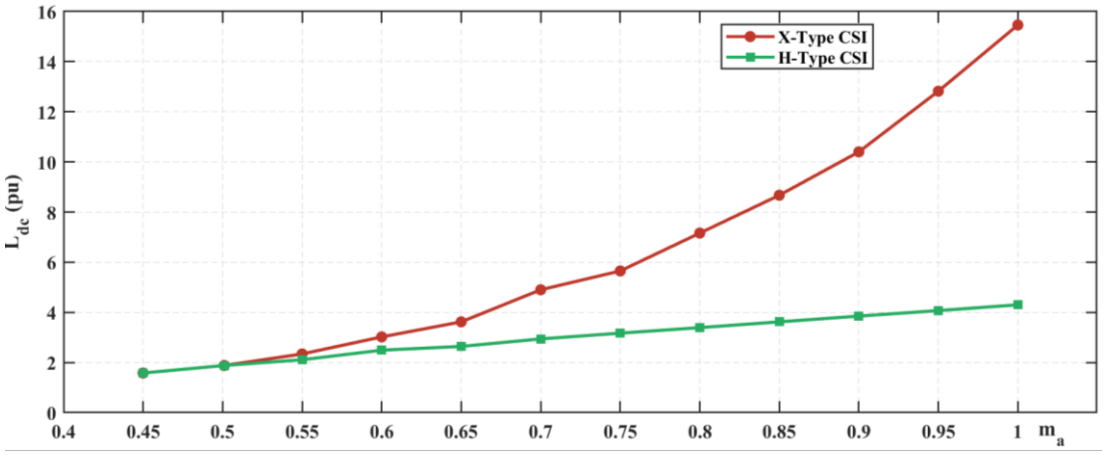


Fig. 2 - 7 Required dc inductance L_{dc} of X-type and H-type CSI

The proposed H-type CSI achieves a smaller required DC inductance compared to the X-type CSI due to differences in their input connection principles. In the H-type CSI, the DC-link inductors remain continuously connected to the input source across all operating modes. This persistent power path enables continuous energy transfer and suppresses inductor current fluctuation. Conversely, in the X-type CSI, the DC inductors are disconnected from the input source during mode 1, forcing them to operate as independent energy stores and causing steep current slopes. As a result, the X-type CSI requires a significantly larger DC inductance, whereas the proposed H-type CSI reduces the required inductance. Overall, this significant reduction in L_{dc} substantially lowers the passive component volume and weight while guaranteeing balanced DC-link inductor currents and satisfying current ripple constraints.

Comparison of Switches Count and Peak voltage Stresses:

The peak voltage stresses of the H-type and X-type five-level CSIs are compared in Table 2-3. In both topologies, the H-bridge switches S_1-S_4 experience a peak voltage stress of V_{C_peak}. However, the dc-side voltage stresses are different. In the X-type CSI, S_5 experiences a peak voltage stress of V_{C_peak}+V_{in}, while the peak voltage stress across S_6 and S_7 is $0.5(V_{C\_peak}+V_{in})$. In contrast, the proposed H-type CSI reduces the peak voltage stress of S_5 to V_{C_peak}-V_{in}, while the stresses of S_6 and S_7 are given by

$max\{0.5(V_{C\_peak}\text{-}V_{in}),\ 0.5V_{in}\}$. Therefore, the proposed H-type CSI achieves lower voltage stresses on the dc-side switches than the X-type CSI. Both the X-type and H-type CSIs are considered under the same boost operating condition, where $V_{C\_peak} > V_{in}$. The blocking-voltage rating of each semiconductor device is assumed to be V_{C_peak}. Under this condition, the proposed H-type CSI requires only one device for each of S_1-S_7, resulting in a total of 7 power switches. For the X-type CSI, S_5 requires two series-connected devices to withstand its peak voltage stress, while S_6 and S_7 can each be implemented with a single device. Therefore, the X-type CSI requires a total of 8 power switches. The proposed H-type CSI thus eliminates one series-connected switch, reducing the semiconductor device count and associated switching losses. The elimination of the series-connected switch reduces the semiconductor device count and the associated switching losses.

Comparison of Power loss and System Efficiency:

The efficiency comparison further demonstrates the advantages of the proposed topology. Under the same operating conditions, the proposed H-type CSI achieves an efficiency of 95.6%, compared with 90.95% for the X-type CSI. The method used for efficiency calculation is a well-used one in industry [42]. The higher efficiency is mainly attributed to the significantly smaller dc-link inductance, which reduces the associated winding loss. Therefore, compared with the X-type CSI, the proposed H-type CSI provides a more compact dc-link design, fewer semiconductor devices, inherent inductor current balancing, and higher overall efficiency, while maintaining the five-level output current capability.

Table 2 - 3 Comparison between X-type and H-type CSI

CSI Topology		X-type	Proposed H-type
L_{dc}		15.5 p.u.	4.3 p.u.
Switch count		8	7
Peak voltage of switch	$V_{S1\text{-}S4\_peak}$	V_{C_peak}	V_{C_peak}
	V_{S5_peak}	$V_{C\_peak}+V_{in}$	$V_{C\_peak}-V_{in}$

	$V_{S6\text{-}S7\_peak}$	$0.5(V_{C\_peak}+V_{in})$	$max\ \{0.5(V_{C\_peak}\text{-}V_{in}), 0.5V_{in}\}$
Need series-connected switch		Yes	No
Diode count		4	5
Efficiency		90.9%	95.6%

These results demonstrate that the proposed H-type CSI achieves a better trade-off among passive component requirement, semiconductor count, current balancing, and conversion efficiency. The reduced dc-link inductance and elimination of the series-connected switch are the key features contributing to the improved performance of the proposed inverter.

2.8 Simulation and Experimental Validation

The performance of the proposed H-type five-level CSI is verified through both simulation and lab-scaled experiments. The main simulation and experimental parameters are listed in Table 2-4. To evaluate the inherent dc-link inductor current self-balancing capability of the proposed inverter, mismatched dc inductors are intentionally employed. The unequal inductance values introduce an initial mismatch between the two dc inductors, allowing the current-balancing capability of the proposed topology to be evaluated under asymmetric operating conditions.

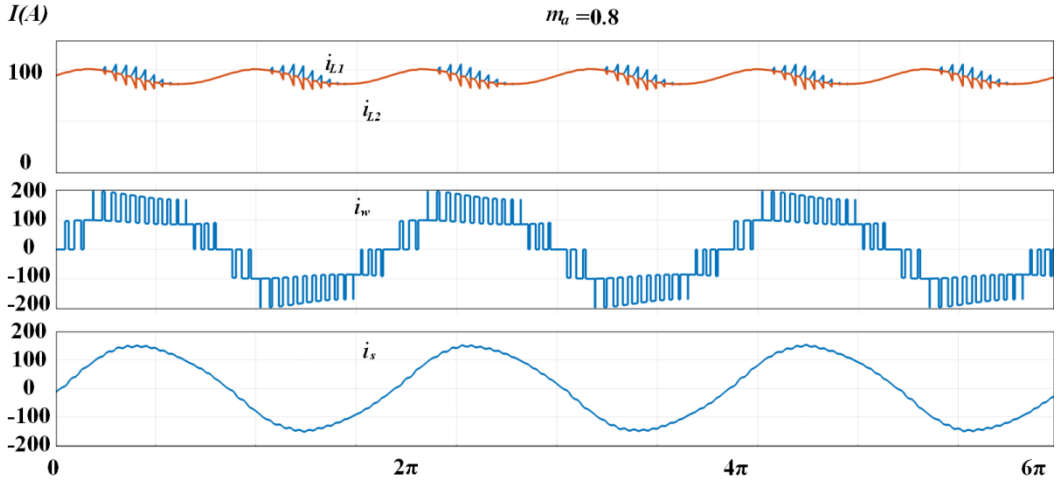
Table 2 - 4 System parameters

Parameters	Simulation	Experiment
Input voltage source	1000 V	V_{in} = 100 V
Fundamental frequency	$f_{S1} = f_{S2}$ = 60 Hz	
Switching frequency	$f_{S3} = f_{S4}$ = 1080 Hz $f_{S5} = f_{S6} = f_{S7}$ = 2160 Hz	
Dc inductance	45 mH, 35 mH	L_1 = 128 mH, L_2 = 123 mH

Filter Capacitor	C_f = 25 uf	C_f = 100 uf
Output load	10 Ω, 5 mH	10 Ω, 20 mH

2.8.1 Simulation Results

A simulation model of the proposed H-type CSI is built through MATLAB/Simulink to evaluate its steady-state performance. The dc inductors are set to 45 mH and 35 mH to represent inductance mismatch. A dc input voltage of 1000 V is employed to the inverter, and the modulation index m_a is set to 0.8 and 0.9. The corresponding simulation waveforms are presented in Fig. 2-8. As shown, the dc inductor currents i_{L1} and i_{L2} converge to the same average value, demonstrating the inherent current self-balancing capability of the proposed topology under the selected operating conditions.



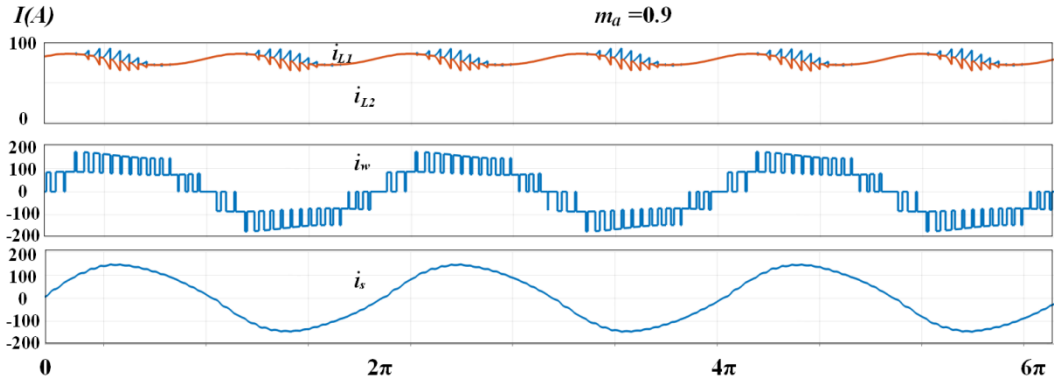


Fig. 2 - 8 Simulated waveforms of the proposed inverter

The output PWM current i_w exhibits five distinct current levels with a symmetrical waveform, while the load current i_s remains approximately sinusoidal. As m_a increases from 0.8 to 0.9, the amplitude of the load current increases accordingly.

The harmonic spectra of the PWM current i_w are presented in Fig. 2-9 for a fundamental frequency of 60 Hz and a switching frequency of 1080 Hz. The measured THD values of i_s are 38.52% and 34.17% for m_a = 0.8 and m_a = 0.9, respectively. In both cases, the dominant harmonic components are concentrated around 2160 Hz, corresponding to the 36th harmonic. This agrees with the characteristic harmonic distribution of the phase-shifting SPWM, in which the dominant harmonic components are located around twice the switching frequency. As m_a increases from 0.8 to 0.9, the dominant harmonic component decreases from approximately 18% to 14% of the fundamental component.

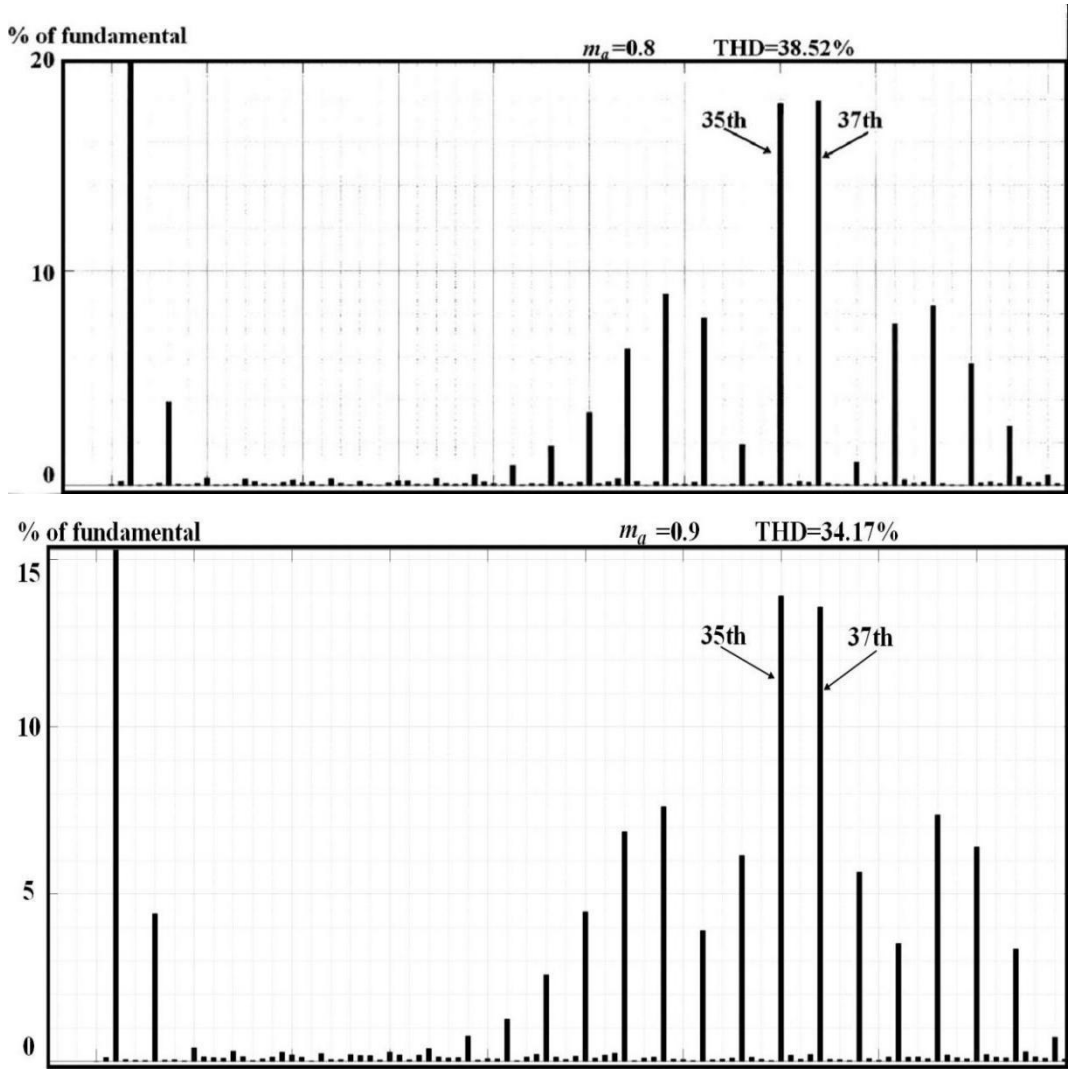


Fig. 2 - 9 Harmonic performance of the proposed inverter

2.8.2 Experimental Results

Lab-scaled experiments are conducted to verify the performance of the proposed H-type CSI. The experimental platform consists of the proposed inverter is shown in Fig. 2-10.

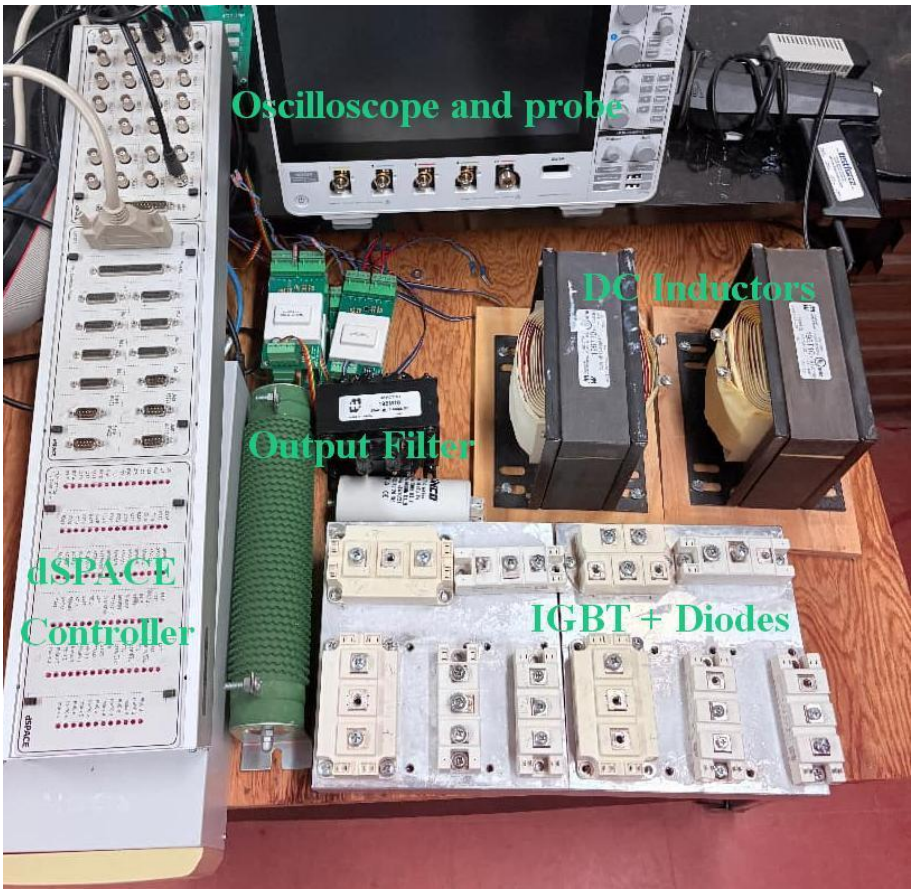


Fig. 2 - 10 Experimental setup of the proposed inverter

The inverter is controlled using a dSPACE-based control system, and the main experimental parameters are listed in Table 2-4. The dc inductors are set to 123 mH and 128 mH to introduce an inductance mismatch. A dc input voltage of 100 V is employed to the inverter, and the modulation index m_a is set to 0.8 and 0.9. In the experimental setup, the minimum overlap time achievable by the dSPACE controller is limited to 2e-5. This limitation causes some narrow gating pulses to be removed, which affects the output current waveforms and harmonic performance.

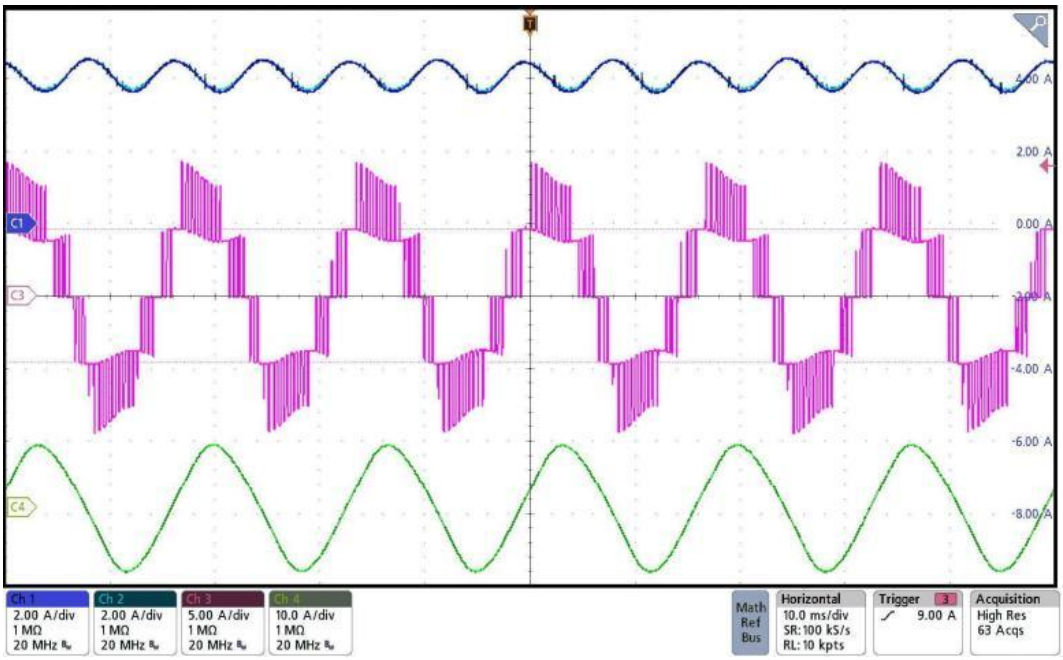


Fig. 2 - 11 Experimental waveforms under steady state and $m_a = 0.8$

CH1 (2A/div): DC inductor current i_{L1}. CH2 (2A/div): DC inductor current i_{L2}. CH3 (5A/div): Output PWM current i_w. CH4 (10A/div): Load current i_s.

Fig. 2-11 shows the experimental waveforms of the proposed H-type CSI under steady-state operation with V_{in} = 100Vand $m_a = 0.8$. The dc-link inductor currents i_{L1} and i_{L2} exhibit switching-frequency ripples while maintaining nearly identical average values, confirming the inherent current self-balancing capability under the intentional inductance mismatch. The output PWM current i_w presents five distinct current levels over one 60-Hz fundamental cycle, verifying the five-level current synthesis. The load current i_s is nearly sinusoidal, demonstrating the effective filtering of the switching components by the output filter. These experimental results agree with the expected operating characteristics of the proposed H-type CSI.

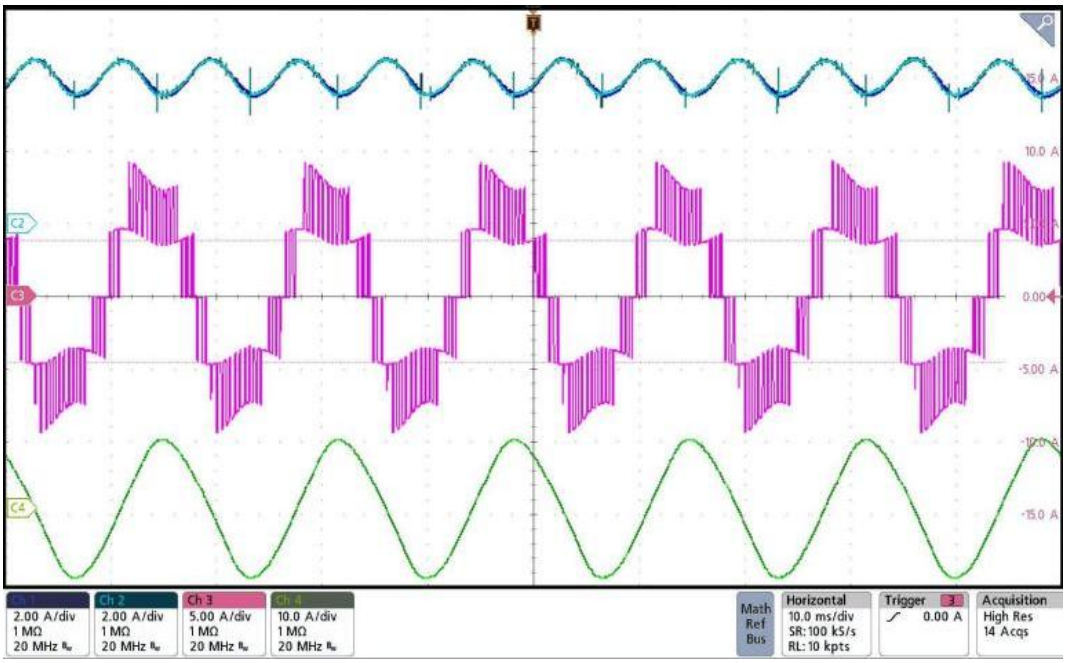


Fig. 2 - 12 Experimental waveforms under steady state and $m_a = 0.9$

CH1 (2A/div): DC inductor current i_{L1}. CH2 (2A/div): DC inductor current i_{L2}. CH3 (5A/div): Output PWM current i_w. CH4 (10A/div): Load current i_s.

Fig. 2-12 shows the experimental waveforms of the proposed H-type CSI under steady-state operation with V_{in} = 100Vand $m_a = 0.9$. The dc-link inductor currents i_{L1} and i_{L2} maintain nearly identical average values despite the inductance mismatch, demonstrating that the inherent current self-balancing capability is maintained at the higher modulation index. Compared with the results at $m_a = 0.8$ shown in Fig. 2-11, the average dc-link current increases as m_a increases, while the two inductor currents remain balanced. The output PWM current i_w maintains five distinct current levels over the 60-Hz fundamental cycle, confirming the five-level current synthesis of the proposed inverter. The amplitude of i_w also increases with m_a, resulting in a higher load-current amplitude. The load current i_s remains nearly sinusoidal, indicating that the output filter effectively attenuates the switching components. Overall, the experimental results at $m_a = 0.9$ agree with those obtained at $m_a = 0.8$, while demonstrating the increased current amplitude associated with the higher modulation index.

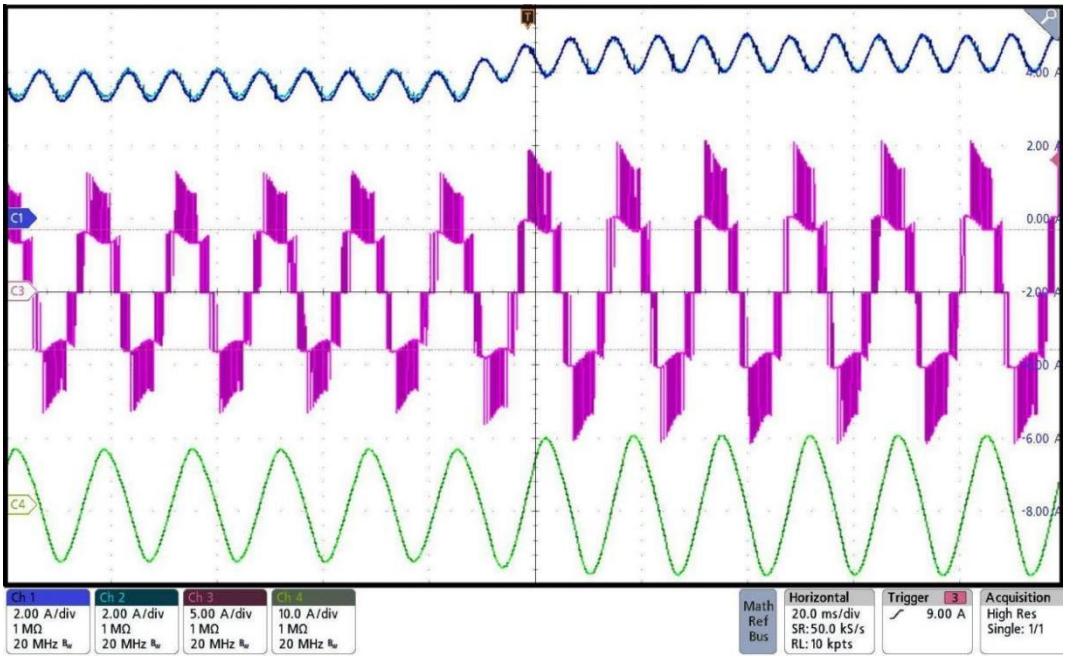


Fig. 2 - 13 Experimental waveforms under dynamic state

CH1 (2A/div): DC inductor current i_{L1}. CH2 (2A/div): DC inductor current i_{L2}. CH3 (5A/div): Output PWM current i_w. CH4 (10A/div): Load current i_s.

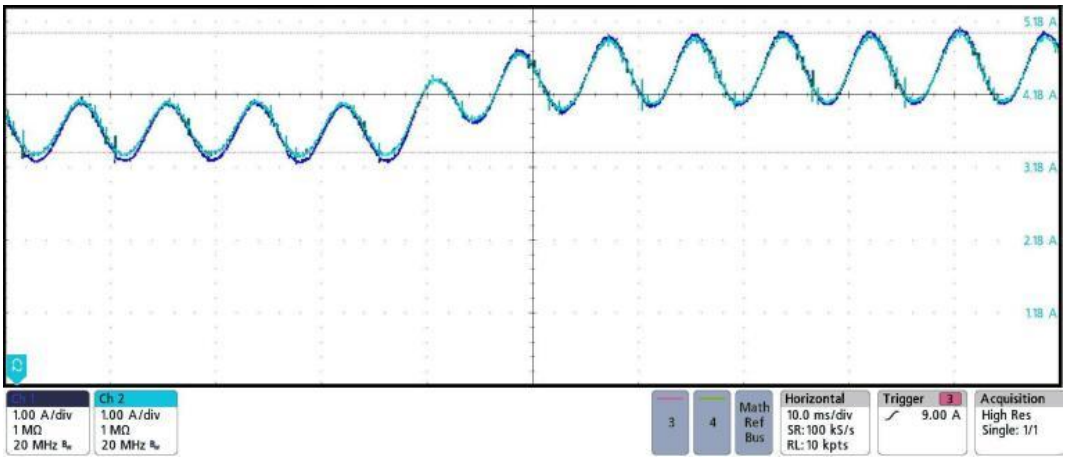


Fig. 2 - 14 Experimental inductor current waveforms under dynamic state

CH1 (1A/div): DC inductor current i_{L1}. CH2 (1A/div): DC inductor current i_{L2}.

Fig. 2-13 and Fig. 2-14 show the dynamic experimental waveforms of the proposed H-type CSI when the input voltage is stepped from 80 V to 100 V. Following the input-voltage step, the dc-link inductor currents i_{L1} and i_{L2} adjust to the new operating condition while maintaining nearly identical average values. This demonstrates that the inherent dc-link inductor current self-balancing capability is

maintained under dynamic state. As shown in Fig. 2-13, the output PWM current i_w continues to maintain the five-level current waveform, while the load current i_s remains nearly sinusoidal. Fig. 2-14 provides a closer view of the dc-link inductor currents and further confirming their balanced response to the input-voltage step. These results demonstrate that the proposed H-type CSI maintains stable operation and inherent inductor current self-balancing under a dynamic input-voltage condition.

2.9 Summary

A new single-phase H-type five-level current source inverter (CSI) is proposed in this paper. Unlike conventional five-level CSIs that require additional current-balancing control, the proposed inverter achieves inherent dc-link inductor current self-balancing through its circuit structure, eliminating the need for an additional control loop. Compared with the existing X-type five-level CSI, the proposed inverter significantly reduces the required dc-link inductance, from 15.5 p.u. to 4.3 p.u., while maintaining the current ripple performance. In addition, the proposed topology eliminates the series-connected auxiliary switch required in the X-type CSI, reducing the total number of switches from eight to seven. These features reduce the passive component requirement and associated semiconductor and inductor losses, resulting in improved conversion efficiency. Under the same operating conditions, the proposed H-type CSI achieves an efficiency of 95.6%, compared with 90.95% for the X-type CSI. The operating principle and performance of the proposed inverter are verified through both simulation and laboratory-scale experimental results.

Chapter 3 Conclusions and Contributions

This dissertation investigates single-phase five-level current source inverters, with a focus on the proposed H-type topology, its modulation scheme, and performance evaluation. This chapter summarizes the main contributions of the research and discusses potential directions for future work.

3.1 Conclusions and Contributions

A new single-phase H-type five-level CSI has been proposed and investigated in this thesis. The proposed topology provides inherent dc-link inductor current self-balancing without requiring an additional current-balancing control loop. Simulation and experimental results confirm the inherent self-balancing of the dc-link inductor currents despite the inductance mismatch. The proposed inverter also reduces the required dc-link inductance compared with the X-type five-level CSI. The required dc-link inductance is reduced from 15.5 p.u. for the X-type CSI to 4.3 p.u. for the proposed H-type CSI, which reduces the size and associated loss of the dc-link magnetic components.

The voltage stress of the proposed topology is also lower on the dc side. Under the same boost operating condition, the proposed H-type CSI reduces the peak voltage stress across the auxiliary switches compared with the X-type CSI. With the H-bridge switch voltage rating selected to withstand V_{C_peak}, the proposed topology can be implemented with seven power switches, whereas the X-type CSI requires eight power switches due to the series-connected devices on the dc side. The elimination of the series-connected auxiliary switch reduces the semiconductor device count and avoids the additional switching losses associated with the series-connected device.

The system efficiency of the proposed H-type CSI is further evaluated by considering both semiconductor and inductor losses. Under the selected operating conditions, the proposed H-type CSI achieves an efficiency of 95.6%, compared with

90.95% for the X-type CSI. The higher efficiency is mainly attributed to the reduced dc-link inductance and the elimination of the series-connected switch, which reduce the associated inductor and semiconductor losses. Finally, the proposed inverter is verified through MATLAB/Simulink simulations and laboratory-scale experiments. The experimental results demonstrate stable five-level current generation, nearly sinusoidal load current, and inherent dc-link inductor current self-balancing under both steady-state and changed input-voltage conditions. These results confirm the effectiveness of the proposed H-type five-level CSI in terms of current balancing, passive-component requirements, semiconductor utilization, and overall efficiency.

3.2 Future Work

Future work will focus on investigating the application of the proposed H-type five-level CSI in grid-connected renewable energy systems, with particular emphasis on grid-connected operation and power quality performance.

References

[1] B. Wu, High-Power Converters and AC Drives. New York, NY, USA/Piscataway, NJ, USA: *Wiley/IEEE Press*, 2006.

[2] Bin Wu, S. B. Dewan and G. R. Slemon, "PWM-CSI inverter for induction motor drives," in *IEEE Transactions on Industry Applications*, vol. 28, no. 1, pp. 64-71, Jan.-Feb. 1992.

[3] Hasan Komurcugil, "Steady-state analysis and passivity-based control of single-phase PWM current-source inverters," *IEEE Transactions on Industrial Electronics*, 2010, 57(3): 1026-1030.

[4] N. Prabaharan, Z. B. Salam and K. Palanisamy, "A hybrid multilevel inverter with reduced power electronic components with unipolar trapezoidal pulse width modulation," *2017 IEEE Conference on Energy Conversion (CENCON)*, Kuala Lumpur, Malaysia, 2017.

[5] T. Noguchi, and Suroso, "New Multilevel Current-Source PWM Inverter with Full-Bridge Inductor Cells," *IEE-Japan Trans. on Industry Applications*, vol. 130-D, no. 6, pp. 808-815, Jun. 2010.

[6] P. I. Adamu, D. L. M. Nzongo, C. Lai, A. Anik and K. L. V. Iyer, "Cascaded H-Bridge Converter-Based PMSM Drive: PS-PWM and LS-PWM Modulation Comparison," *IECON 2025 – 51st Annual Conference of the IEEE Industrial Electronics Society*, Madrid, Spain, 2025, pp. 1-6.

[7] S. Laali, K. Abbaszadeh and H. Lesani, "Development of multi-carrier PWM technique for multilevel inverters," *2010 International Conference on Electrical Machines and Systems*, Incheon, Korea (South), 2010, pp. 77-81.

[8] Aarthi K. and S. Sengupta, "Forced commutation technique for current source inverter employed in load commutated inverter drive," *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, 2016, pp. 1-6.

[9] R. Sebastian C and P. P. Rajeevan, "Load-Commutated SCR-Based Current Source

Inverter Fed Induction Motor Drive with Open-End Stator Windings," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2031-2038, March 2018.

[10] R. Sebastian C and P. P. Rajeevan, "Load-Commutated SCR-Based Current Source Inverter Fed Induction Motor Drive With Open-End Stator Windings," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2031-2038, March 2018.

[11] Z. Liu, J. J. Liou, S. Dong and Y. Han, "Silicon-Controlled Rectifier Stacking Structure for High-Voltage ESD Protection Applications," in *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 845-847, Aug. 2010.

[12] I. J. Shapiro, "Silicon-controlled rectifiers, unijunction transistors and tunnel diodes," in *Transactions of the South African Institute of Electrical Engineers*, vol. 55, no. 2, pp. 205-213, June 1964.

[13] N. R. Zargari, S. C. Rizzo, Y. Xiao, H. Iwamoto, K. Satoh and J. F. Donlon, "A new current-source converter using a symmetric gate-commutated thyristor (SGCT)," in *IEEE Transactions on Industry Applications*, vol. 37, no. 3, pp. 896-903, May-June 2001.

[14] M. Hombu, S. Ueda and A. Ueda, "A Current Source GTO Inverter with Sinusoidal Inputs and Outputs," in *IEEE Transactions on Industry Applications*, vol. IA-23, no. 2, pp. 247-255, March 1987.

[15] J. Kim, T. Kim and W. Lee, "Self-Powered Gate Drive for Series Connected SiC MOSFETs in MV Applications," *2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE)*, Philadelphia, PA, USA, 2025, pp. 1-6.

[16] Y. Zhang, Y. Shi and H. Li, "Study of Passive dv/dt Filter and Proposed Active Solution for SiC MV Motor Drive," *2019 IEEE Electric Ship Technologies Symposium (ESTS)*, Washington, DC, USA, 2019, pp. 236-240.

[17] A. Adam and F. Kaçar, "Medium-Voltage (MV) Motor Drives Topologies and Applications," *2022 International Conference on Electrical, Computer and Energy Technologies (ICECET)*, Prague, Czech Republic, 2022, pp. 1-5.

[18] P. G. Barbosa, H. A. C. Braga, M. C. Barbosa, and E. C. Teixeria, “Boost Current Multilevel Inverter and Its Application on Single Phase Grid Connected Photovoltaic

System," *IEEE Trans. on Power Electronics*, vol. 21, no. 4, pp. 1116-1124, Jul./Aug. 2006.

[19] J. Rodiguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverter: A Survey of Topologies, Controls, and Application," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Jul./Aug. 2002.

[20] S. Kwak, and H. A. Toliyat, "Multilevel Converter Topology Using Two Types of Current-Source Inverters," *IEEE Trans. on Industry Applications*, vol. 42, no. 6, pp. 1558-1564, Nov./Dec. 2006.

[21] Y. Shi, B. Liu and S. Duan, "Low-Frequency Input Current Ripple Reduction Based on Load Current Feedforward in a Two-Stage Single-Phase Inverter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7972-7985, Nov. 2016.

[22] D. R. Joca, L. H. S. C. Barreto, D. d. S. Oliveira, P. P. Praça, R. N. A. L. Silva and G. A. L. Henn, "THD analysis of a modulation technique applied for THD reduction," *2013 Brazilian Power Electronics Conference*, Gramado, Brazil, 2013, pp. 177-182.

[23] H. Vadizadeh, N. Farokhnia, S. H. Fathi and D. Rabbani, "Extracting formulas of line voltage THD for 7-level inverter with equal DC sources," *11th International Conference on Electrical Power Quality and Utilisation*, Lisbon, Portugal, 2011, pp. 1-9.

[24] G. Zhang, Z. Wu, S. S. Yu and Y. Zhang, "A Novel Impedance-Network-Based Electric Spring," in *IEEE Access*, vol. 8, pp. 129123-129135, 2020.

[25] P. Kumar and M. Veerachary, "Analysis and Design of Two High Voltage Gain Impedance Network based Boost Converters," *2020 International Conference on Power, Instrumentation, Control and Computing (PICC)*, Thrissur, India, 2020, pp. 1-6.

[26] A. Gond, R. Pariyar, M. Roy and A. Panda, "Design and Analysis of Impedance Network-Based Cascaded Multilevel Inverter," *2025 IEEE 1st International Conference on Smart and Sustainable Developments in Electrical Engineering (SSDEE)*, Dhanbad, India, 2025, pp. 1-6.

[27] F. Faraji and H. Cha, "Single-Rating Multilevel Current Source Inverter With Fault

Tolerance," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 5, pp. 4538-4549, Oct. 2024.

[28] F. Gao, P. Loh, F. Blaabjerg, and D. Vilathgamuwa, “Five-level current source inverters with buck-boost and inductive-current balancing capabilities,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2613–2622, Aug. 2010.

[29] A. Muqorobin, S. Wijanarko, H. P. Santosa and I. D. Irawati, "Input Current Ripple Analysis of Three Phase Modified Buck-Boost Inverter," *2024 11th International Conference on Electrical Engineering, Computer Science and Informatics (EECSI)*, Yogyakarta, Indonesia, 2024, pp. 131-135.

[30] Y. Itoh, S. Kimura, J. Imaoka and M. Yamamoto, "Inductor loss calculation of coupled inductors for high power density boost converter," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, Japan, 2014, pp. 2497-2502.

[31] S. Marihal, B. V. Madiggond and K. Negalur, "A Review on Higher DC-Link Voltage & Reduction of Voltage Stress Across the Switch in Switched Boost Inverters," *2025 4th International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, Tirupur, India, 2025, pp. 292-298.

[32] Fang Zheng Peng and Yi Huang Michigan, “Z-Source Inverter for Power Conditioning and Utility Interface of Renewable Energy Sources,” *IEEE Trans*, Vol. 23, no. 4, 2004.

[33] F. Z. Peng, “Z-Source inverter,” *IEEE Trans. Ind. Applicat.*, vol. 39, pp. 504–510, Mar./Apr. 2003.

[34] S. Yang, F. Z. Peng, Q. Lei, R. Inoshita, and Z. Qian, "Current-fed Quasi-Z-Source Inverter with Voltage BuckBoost and Regeneration Capability," in *IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, San Jose, 2009.

[35] Yi Huang, Miaosen Shen, Fang Z. Peng and Jin Wang, “Z-Source Inverter for Residential Photovoltaic Systems”, *IEEE transactions on power electronics*, vol. 21, no. 6, November 2006, pp.1776-1782.

[36] L. Xing, Q. Wei and R. Y. Li, "A New 5-Level Current Source Inverter with

Inherent Balancing," *2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Shanghai, China, 2023, pp. 30-34.

[37] N. Lekgamheng and Y. Kumsuwan, "Phase-shifted PWM strategy of a seven-level single-phase current source inverter for grid-connection systems," *2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS)*, Kitakyushu, Japan, 2013, pp. 1025-1028.

[38] J. Chen, D. Liu, K. Ding, C. Wang and Z. Chen, "A Single-Phase Double T-Type Seven-Level Inverter," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018, pp. 6344-6349.

[39] I. W. Christopher, J. Parthiban, B. Saravanan, R. Kumar, S. Pallavan and R. Ramesh, "Microcontroller based single-phase simplified seven-level inverter for PV system," *2012 IEEE 5th India International Conference on Power Electronics (IICPE)*, Delhi, India, 2012, pp. 1-6.

[40] Q. Zhang et al., "A Novel Single-Phase Seven-Level Inverter with Its Modulation Strategy," *2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Xi'an, China, 2019, pp. 2260-2265.

[41] Z. Wang, Q. Wei and N. R. Zargari, "H-Type Five-Level Current Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 39, no. 9, pp. 10682-10687, Sept. 2024.

[42] N. R. Zargari, S. C. Rizzo, Y. Xiao, H. Iwamoto, K. Satoh, and J. F. Donlon, “A new current-source converter using a symmetric gate-commutated thyristor (SGCT),” *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 896–903, May/Jun. 2001.