THE DESIGN OF FAST-TRANSIENT CAP-LESS LOW-DROPOUT VOLTAGE REGULATORS

by

Pierre Leduc

A thesis

presented to Lakehead University

in partial fulfillment of the

requirements for the degree of

Master of Science

in the Program of

Electrical and Computer Engineering

Thunder Bay, Ontario, Canada, 2024

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ABSTRACT

Pierre Leduc
THE DESIGN OF FAST-TRANSIENT CAP-LESS LOW-DROPOUT VOLTAGE REGULATORS
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This thesis provides a theoretical and experimental study of cap-less LDO regulators for high speed applications. The three different architectures used in LDO designs are reviewed in detail along with their advantages and disadvantages. Theoretical analysis of each architecture is covered along with a review of state of the art designs. The thesis presents two cap-less designs. The first design uses a dual loop architecture to enable fast transient response and high current capability of which the current loop offers fast transient while the voltage loop provides regulation. The second proposed LDO utilizing a hybrid architecture of which the digital part introduces a fast transient approximation algorithm demonstrating significant speed improvements over traditional algorithms. The design is optimized for low clock frequency applications and high output current. Both LDO designs are manufactured using the TSMC 180 nm technology and demonstrate both simulation and measurement results.

ACKNOWLEDGMENTS

First and foremost, I would like to express my most sincere gratitude to my advisor, Professor Dr. Yushi Zhou, for his kind guidance, helpful discussions and constructive suggestions throughout my study. I could not have completed this work without his support and dedication.

The support and knowledge from Dr. Ximing Fu and Professor Dr. Kamal El-Sankary from Dalhousie University is greatly acknowledged. The technical support for all measurements and PCB population is acknowledged to Dan Vasiliu.

I also thank the other committee members, Professor Dr. Qiang Wei and Professor Dr. Farhan Ghaffar, for their invaluable feedback.

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List of Symbols

ADS	Advanced Design Systems
AC	Alternative Current
ADC	Analog to Digital Converter
BP	Band-Pass
BW	Bandwidth
CAD	Computer-Aided Design
$CFOA$	Current Feedback Operational Amplifier
CL	Current Loop
$CMOS$	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
dBm	Decibel power with respect to 1 Milliwatt
DC	Direct Current
DFF	D Flip Flop
EA	Error Amplifier
ESD	Electrostatic Discharge
FF	(nMOS)Fast-(pMOS)Fast
FoM	Figure of Merit
FS	(nMOS)Fast-(pMOS)Slow

FU	Functional Unit
gm	Trans-conductance
IC	Integrated Circuit
ISO	International Organization for Standardization
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LDO	Low Dropout
LHP	Left Hand Plane
LP	Low-Pass
MiM	Metal Insulator Metal
$NMOS$	n-channel Metal-Oxide Semiconductor
$Opamp$	Operational Amplifier
PCB	Printed Circuit Boards
PDK	Process Development Kit
PM	Phase Margin
$PMOS$	p-channel Metal-Oxide Semiconductor
$PSRR$	Power Supply Rejection Ratio
PVT	Process (supply-)Voltage Temperature
RF	Radio Frequency
RHP	Right Hand Plane
SAR	Successive Approximation Register
SF	(nMOS)Slow-(pMOS)Fast
SoC	System on Chip

SS	(nMOS)Slow-(pMOS)Slow
TT	(nMOS)Typical-(pMOS)Typical
VCO	Voltage-Controlled Oscillator
VI	Voltage to current
VL	Voltage Loop
ZOH	Zero Order Hold

Chapter 1

INTRODUCTION

1.1 Background

Many of the modern technology that surround us such as cellular devices, computers and IoT have become a necessity in our day to day lives. These devices implement sub circuits such as memory, SoC, CPU's and FPGA's that all necessitates a stable voltage supply to function. A voltage regulator is used to achieve the desired voltage regulation. Voltage regulators are available in 2 main types; switch mode voltage regulators and linear voltage regulators. Switch mode voltage regulators uses inductors and/or capacitors to store and release the electrical energy in order to increase or reduce the output voltage. Linear voltage regulators dissipates the extra energy as heat in order to lower the output voltage. Both architectures have their advantages and disadvantages, the linear voltage regulator is most commonly used in IC applications as they exhibit better response time and lower output ripples and don't require bulky inductors to implement. A typical power distribution network is shown in Fig. 1.1 where a switch mode power supply is used to lower the voltage from either the power grid voltage or a battery for portable devices. This DC-DC converter is implemented on a board level design. The voltage is then applied to the IC/SoC device which implements the desired functionality. In order for the functinal units (FU) to operate as intended the voltage must be further dropped, where the linear voltage regulator is used. To maximize the performance and ease of power distribution, the linear voltage regulator is implemented directly on the IC.

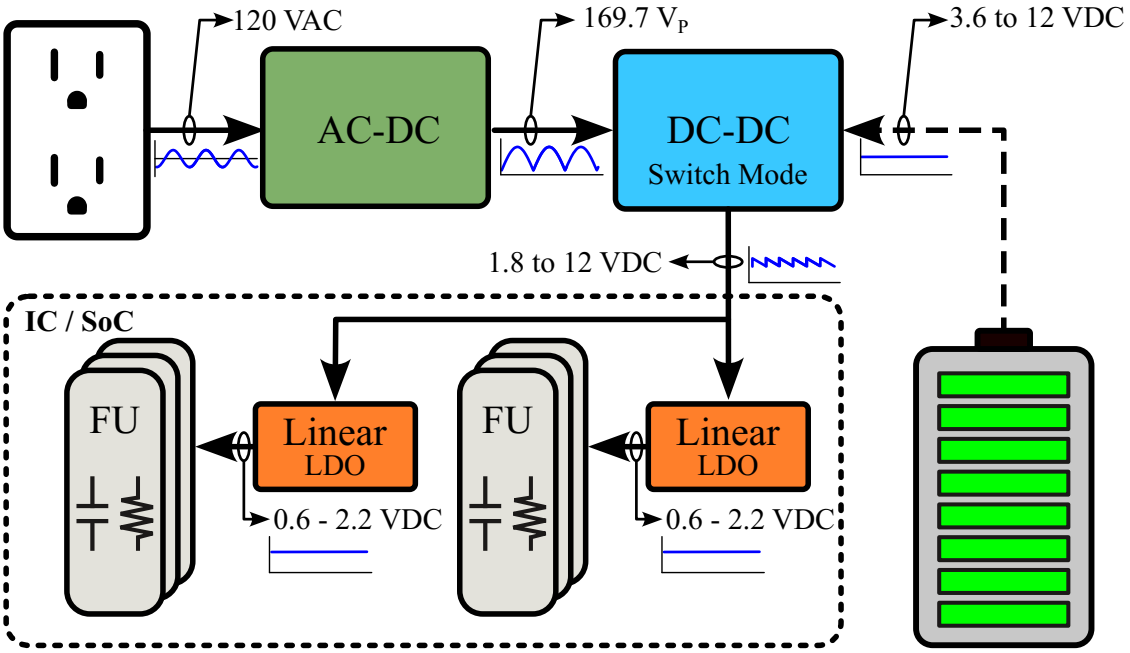


Figure 1.1: Typical power distribution network for IC/SoC devices.

The linear voltage regulator can be characterized based on their performance characteristics. The low dropout voltage regulator is capable of operating with a lower voltage difference between the supply and output voltage. This is referred as their dropout voltage (V_{DO}). This lower voltage is usualy in the range of 50 to 500 mV where conventional regulators have a minimum dropout voltages closer to 3V. This lower dropout voltage also improves the power efficiency of the LDO regulator. The term LDO is used to refrence linear voltage regulators with low dropout characteristics. Some linear voltage regulators require an output capacitor in order to maintain stability and performance, capacitorless voltage regulators omits this output capacitance reducing the area consumption and compensates with a more complex controller design. Regulators that don't require output capacitance to function are designated as capacitor-less (Cap-less) voltage regulators. A linear voltage regulator can be both the LDO and cap-less type at the same time where our main research is focused.

1.2 Motivation

Though the conventional LDO design has been widely used, efficiency, voltage and performance requirements has pushed researchers to develop better topologies in order to improve the performance of the LDO to meet the demand of modern technological trends. Modern electronic devices are increasingly being powered from energy storage devices such as lithium ion batteries. This applies to cellphones, laptop computers and electric cars. Thus improving the power efficiency of the power management system is of crucial importance to increase battery life. For large power devices such as CPU's thermal management is also of critical importance. The power dissipation of the linear voltage regulator is dominated by the voltage drop between the supply and load voltage and can be represented as:

$$P_{diss} = \frac{V_{IN} - V_{Out}}{I_{Load}} = \frac{V_{DO}}{I_{Load}}. \tag{1.1}$$

Where P_{diss} is the power dissipation, V_{IN} and V_{Out} are the input voltage and output voltage respectively. Reducing the dropout voltage increases the power efficiency significantly and also reduces the power dissipation easing the thermal management requirements.

Many trends make it desirable to reduce the supply voltage of microelectronic circuits forcing the LDO to accommodate as well. To reduce the dynamic power of a digital circuit a reduction in supply voltage has a quadratic effect on the power consumption represented by [15]:

$$P_{swtching} = \alpha C V_{dd}^2 f, \tag{1.2}$$

$$P_{static} = (I_{sub} + I_{gate} + I_{junct}) V_{dd}. \tag{1.3}$$

Where $P_{swtching}$ and P_{static} is the switching and static power dissipation of digital circuits. The shrinking size of the CMOS technology is another motivation to reduce the voltage. Modern fabrication process cannot operate at the elevated supply voltages traditionally used in older technology. The current supply voltage for the up coming 3 nm technology offered by TSMC is only 0.75 V. Modern battery technology can also limit supply voltages, where

for some application the voltage of a single cell is all that is available for the design. This means that battery technology with low cell voltage, or a large voltage deviation between charged and discharged requires LDO's to operate at lower voltages. For example, fuel cells have a cell voltage of only 0.4 to 0.7 V. [16]

The maximum droop that a circuit requires to function is also a cause for concern for LDO designers. Some circuits topologies such as RF circuits and volatile memory are unable to function properly if the supply voltage droops below their minimum requirements even for a brief period. During sharp load transients, an LDO regulator must be able to maintain the output voltage for a wide range of current and offer the proper transient speed to compensate for the load current. For example, a digital controller transitioning from sleep mode to active mode will cause a sharp increase in current consumption that the LDO must be able to handle. As the devices operate at higher speeds the transient speed requirements of LDO's keeps increasing.

One of the advantages of linear voltage regulators is its ability to attenuate supply ripple measured as power supply rejection ratio (PSRR). Many applications, especially in RF, requires a very stable supply voltages in order to achieve optimum performance. Most designs contain a switch mode regulator preceding the LDO regulator to achieve better power efficiency as shown in Fig. 1.1. The intrinsic ripple at the output of the switching regulator results in significant ripples for high precision circuits to function as desired. One of the most utilized building blocks in RFICs is the oscillator, whose phase noise plays a pivotal role in meeting the stringent requirements for data rate in wireless communication systems. The design and analysis of low phase noise oscillators have been extensively explored [17, 18, 19, 20, 21, 22, 23, 24] of which the techniques of lowering the phase noise at the output of oscillator were studied. Moreover, digital circuits consume current in a non-linear manner introducing noise to circuits sharing the same supply lines as depicted in Fig. 1.2 The typical approach to reducing the ripple and noise from the supply lines is the use of an LDO regulator with good PSRR performance.

All of these requirements results in the LDO voltage regulator to require many advancement and development to meet the requirements of modern technology.

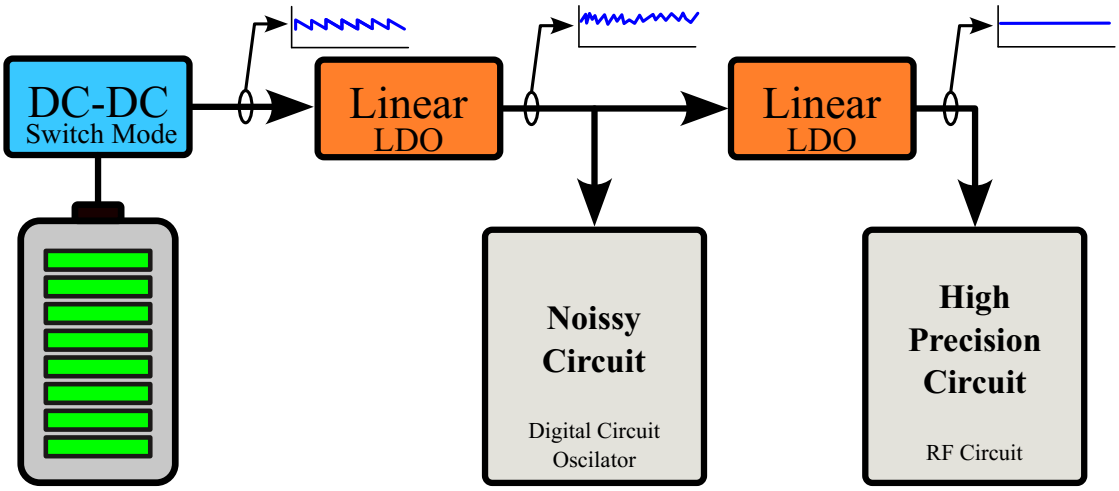


Figure 1.2: Powerline ripple and noise contributions in typical SoC designs.

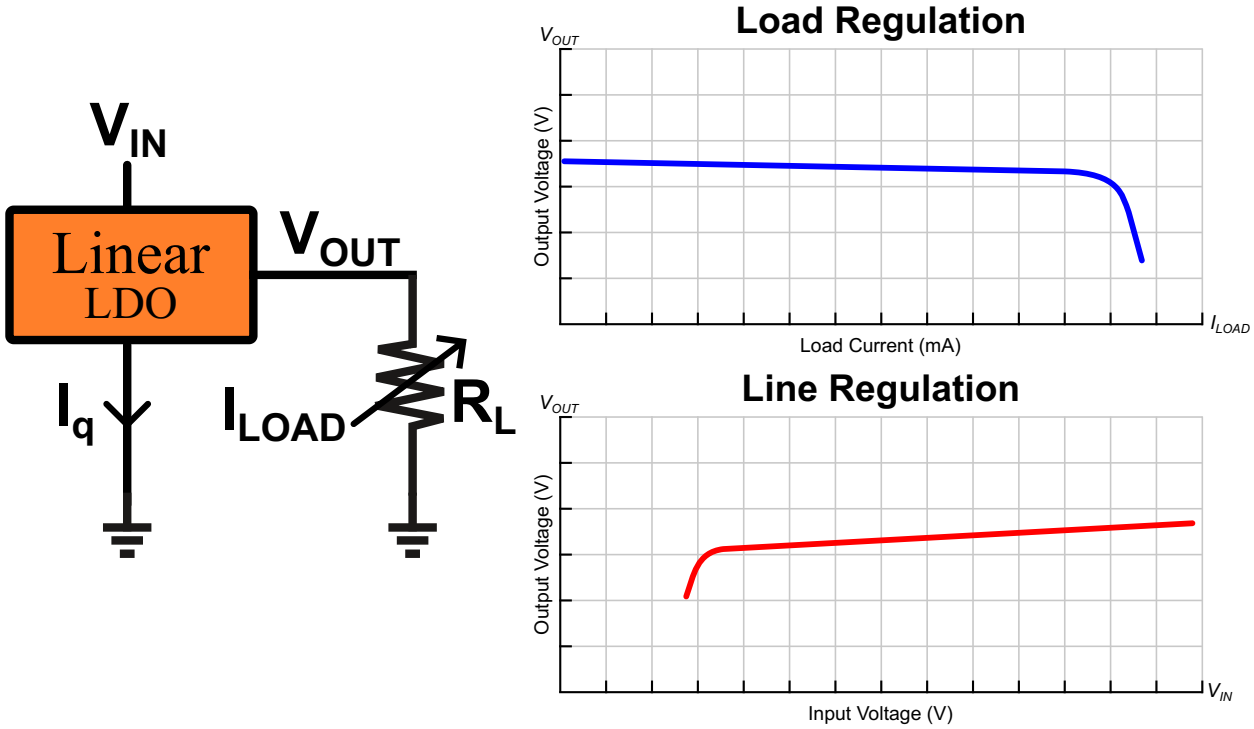


Figure 1.3: Load regulation and line regulation graph.

1.3 Performance Metrics

The LDO regulator can be measured for many performance characteristics in order to determine its viability for a specific application. Load regulation is a measure of the output

voltage precision over the load range of the design. For a fixed voltage reference, the amount of output voltage deviation represents the load regulation. Similarly, the line regulation measure the change in output voltage with fluxuations to the supply voltages. The load and line regulation can be calculated using (1.4) and (1.5) respectively. Lower values of load and line regulation results in better performance. Typical graphs representing the load and line regulation are represented in Fig. 1.3.

$$\textit{Load Regulation} = \frac{V_{out,max} - V_{out,min}}{I_{max} - I_{min}}, \tag{1.4}$$

$$\textit{Line Regulation} = \frac{V_{out,max} - V_{out,max}}{V_{in,max} - V_{in,min}}. \tag{1.5}$$

Dropout voltage, V_{DO}, represents the difference between the input voltage of the LDO and the output voltage. In general, designers are interested in lower values of dropout resulting in better power efficiency. Thus the minimum a design can achieve is always being reported. The dropout voltage can be calculated using:

$$V_{DO} = V_{in} - V_{out}. \tag{1.6}$$

When a load transient is applied to the output of the regulator, a change in voltage occurs at the output. The direction of the voltage change is based on the load transient where an increase in load results in an undershoot situation and a decrease in load results in an overshoot situation. The maximum deviation between the output and desired voltage is known as the the droop voltage. After the maximum droop occurs, the control loop will react in order to return the output voltage to the desired voltage. The time required for the output voltage to return to its initial value is known as the recovery time t_r also called settling time. The load parameters such as the load edge time and maximum current are also crucial as it affects the droop voltage and the settling time of the regulator. Fig. 1.4 shows a typical transient response time with the performance measurements. The quiescent current, I_q, is a measure of current that does not flow through the load of the LDO. This current is not directly being used by the load resulting in a reduction in efficiency. The quiescent current can be used to measure the current efficiency of a linear regulator. Defined

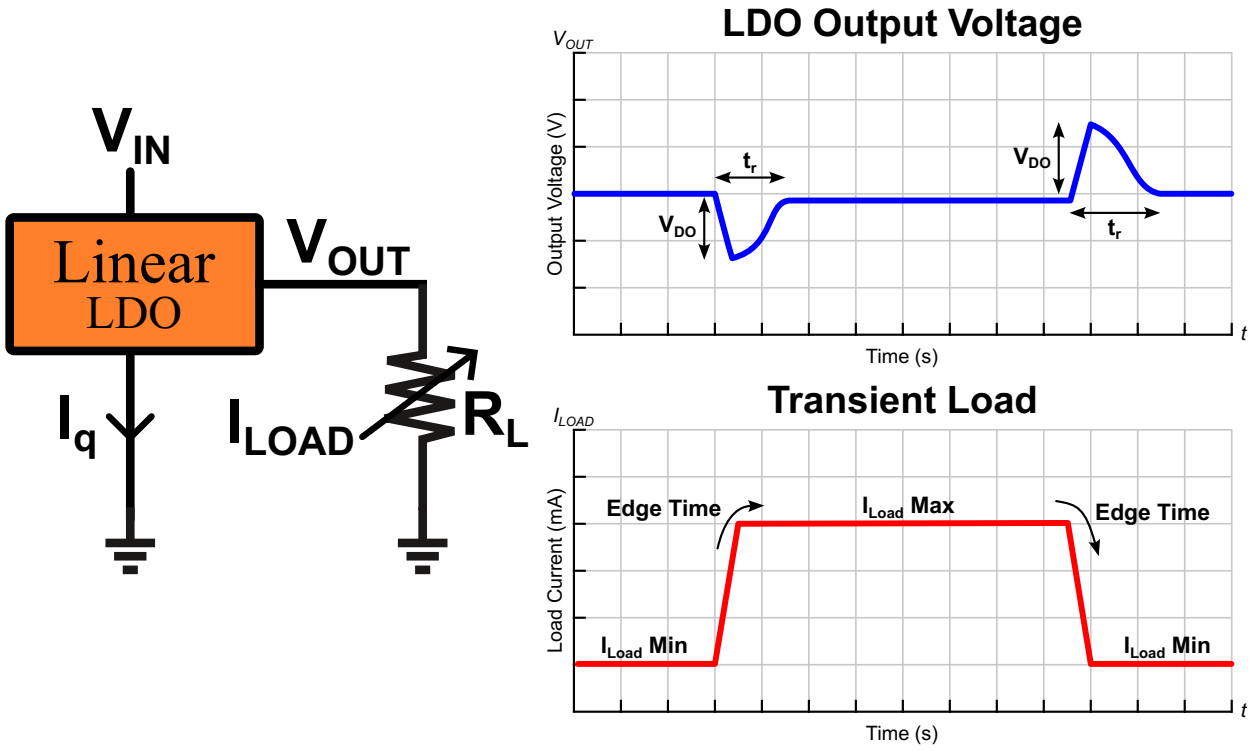


Figure 1.4: Transient load graph of a typical LDO regulator with performance measurements.

using (.1.7), the current efficiency can be calculated using the ratio of the output current to the input current.

$$\eta_I = \frac{I_{OUT}}{I_{IN}} = \frac{I_{Load}}{I_{Load} + I_q} \tag{1.7}$$

PSRR is an important criteria of the linear voltage regulator representing the attenuation factor of ripple and noise from the supply lines. PSRR is measured in dB over a frequency range where a lower dB values means larger attenuation from the supply to the output. The typical frequency range of interest of an LDO regulator is between 10 Hz to 10 MHz depending on its applications. The PSRR can be calculated using [25]:

$$PSRR = 20 \log \frac{V_{INRipple}}{V_{OUTRipple}}. \tag{1.8}$$

Where $V_{INRipple}$ and $V_{OutRipple}$ is the measured supply and output ripple magnitude of the voltage regulator. In order to evaluate the performance of different designs, a figure of merit (FoM) is used to calculate the combined performance of the LDO design. Many different

FoM equations have been developed to measure various design metrics, the most commonly used FoM figures are reviewed. The most common FoM used is represented (1.9) where a smaller number indicates a higher performance [26]. This FoM measure takes in account the droop voltage, output capacitance, quiescent current and maximum current of the LDO.

$$FoM_1 = T_R \frac{I_q}{I_{Max}} = \frac{C_{Out}\Delta V_{Out} I_q}{I_{Max}^2} \tag{1.9}$$

FoM_1 does not take in consideration all the performance criteria of the LDO regulator. In order to include the settling time as part of the metric FoM_2 is proposed [27]. Where it uses the FoM_1 and multiplies it by the achieved settling time shown in Eq. 1.10.

$$FoM_2 = FoM_1 \times t_r = t_r \frac{C_{Out}\Delta V_{Out} I_q}{I_{Max}^2} \tag{1.10}$$

One of the key factors that is not taken in consideration with FoM_1 and FoM_2 is the load edge time. As expected, the edge time of the load has significant effect on droop voltage and settling time of an LDO regulator. FoM_3 is proposed to include an edge time ratio K to compensate for the different edge time of the design comparison [28]. The proposed FoM_3 taking in consideration the edge time, droop voltage, load current and quiescent current is represented as:

$$\begin{aligned} FoM_3 &= K \frac{\Delta V_{Out} I_q}{\Delta I_{Out}}, \\ K &= \frac{t_{Edge} Used}{Smallest\ t_{Edge}\ Used\ among\ comparison\ designs}. \end{aligned} \tag{1.11}$$

As with many IC designs, the process length has an effect on the overall performance of the LDO regulator. The main contributor pertaining to LDO design are the extra parasitic capacitance of the devices. The parasitic capacitance is proportional to $W \times L$ thus for an identical aspect ratio transistor the proposed FoM is multiplied by $\frac{1}{L^2}$ [29]. The resulting FoM_4 is represented as follow:

$$FoM_4 = \frac{t_{edge} V_{Droop} I_q}{I_{Load} L^2}. \tag{1.12}$$

1.4 Current Solutions

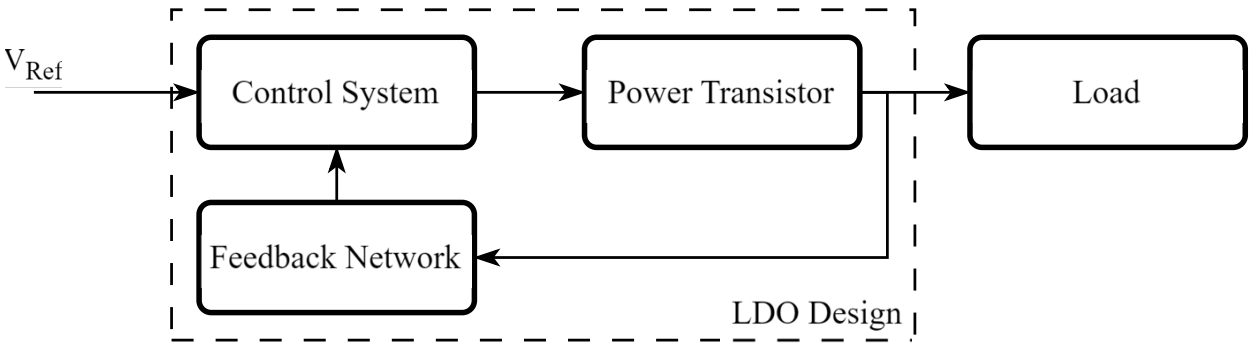


Figure 1.5: Generic architecture of LDO.

Fig. 1.5 shows the basic control system diagram of an LDO regulator composed of a controller stage, power stage and output stage. The conventional LDO contains a voltage feedback loop to regulate the output based on a reference voltage usually provided by a band gap reference circuit. The analog LDO (A-LDO) uses an analog control system and feedback to regulate the output voltage. To improve the performance of the LDO, many techniques such as slew rate enhancements circuits and improved amplifier performance have been adopted. These will be further explored in Chapter 2. In the last decade the digital LDO (D-LDO) has been gaining lots of attention. While it contains some drawbacks, it also has some redeeming features such as higher current density and lower supply voltage requirements which proves difficult to achieve with the A-LDO. The D-LDO consists of a digital controller coupled with a power transistor array. These designs will be further explored in Chapter 3. The final architecture that has been widely developed in academia is the hybrid LDO (H-LDO). This architecture is comprised of an analog and digital LDO to improve the performance. There are many types of hybrid LDOs such as the analog assisted LDO (AAD-LDO) and the digital assisted LDO (DAA-LDO). All the H-LDO architectures aim at improving the characteristics of the LDO by using the assistance of an extra loop in another domain. Although these architectures allow for improved performance, some improvements require further research explored in Chapter 4.

1.5 Issues

As discussed previously, the reduction of supply voltage results in many benefits while also posing an important issues to the traditional A-LDO. The difficulty lies in achieving large proportional gain when supply voltages and node size are small [30]. The low gain results in low voltage regulation and larger error at the output. The driving capabilities of the EA are also reduced with lower supply voltages. The LDO acheiving lower V_{DO}, further complicates the issue as the size of the power transistor must be larger to achieve a smaller equivalence resistance. This results in large gate capacitance further reducing slew rate resulting in large droop voltages at the output. This is an important issue when the maximum current requirement is large resulting in a larger power transistor. The A-LDO also suffers from stability issues further challenging the design of this type of regulator.

The digital LDO deals with some of these issues, digital circuits are able to operate at low supply voltages and have high slew rates. On the flip side, the digital LDO's suffer from high droops as they don't continuously sample the output. D-LDOs also have lower accuracy due to the quantization error introduced by the power transistor array. Due to the quantization error the D-LDO is also unable to regulate the output voltage at low current meaning that D-LDOs have a current range of operation. Due to the quantization and sampling rate, the D-LDO also has poor PSRR. This means that the D-LDO cannot replace the A-LDO for many designs due to its performance issues.

In an effort to improve the performance a natural approach is to combine the A-LDO and the D-LDO. This does allow to fix some of the performance issues such as the minimum current requirement and the quantization error. Some issues that are still present are the low slew rate for the analog device and the supply voltage requirements. There is also a new issue of control complexity relating to the digital and analog LDO's as both must remain stable when controlling the output voltage together.

1.6 Organization

The rest of this document will further explore the advantages and disadvantages of the different architectures presented above along with a review of current LDO designs and techniques. The document ends with a detailed report on our reaserch on the LDO voltage regulator. Chapter 2 will discuss the analog LDOs, Chapter 3 will cover the digital LDOs and Chapter 4 will review the hybrid LDOs. Chapter 5 covers our research on the dual loop LDO and Chapter 6 reviews our reserch on the hybrid LDO using a novel approximation algorithm. The document is concluded in Chapter 7.

Chapter 2

Analog LDO

Over the course of this chapter, the analog LDO design is explored in details including the architecture, design, advantages and disadvantages. A number of state of the art A-LDO's are reviewed at the end of the Chapter.

2.1 Architecture

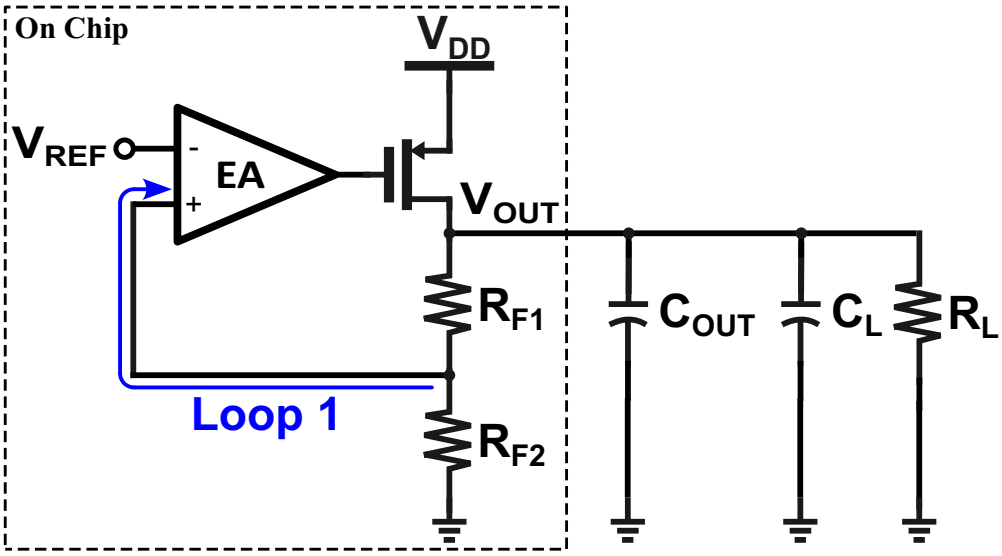


Figure 2.1: A-LDO architecture [1, 2, 3, 4, 5, 6].

Fig 2.1 shows the basic architecture of the analog LDO. The main components are the error amplifier (EA), the power transistor and the resistor feedback network. What makes this an A-LDO is the analog output of the controller in this case the EA. To properly model the LDO, a linear load composed of a resistor and a capacitor are added to the output. In order to ensure that a negative feedback loop is represented, an analysis is conducted. Let's assume that the output is constant and a sharp increase in load current is applied to the output. The load voltage will then reduce as the equivalent resistance of the power transistor remains fixed. This droop in voltage at the output will also reduce the voltage on the feedback resistors. The drop in voltage at the input of the EA is amplified with a positive Gm. This amplification reduces the gate voltage on the power transistor. The $-gm$ of the PMOS increases the current being supplied to the load. The increased current raises the voltage on the load resistor increasing the output voltage. Since the direction is opposite to that of the stimulus then this is a negative feedback system [1, 2, 3].

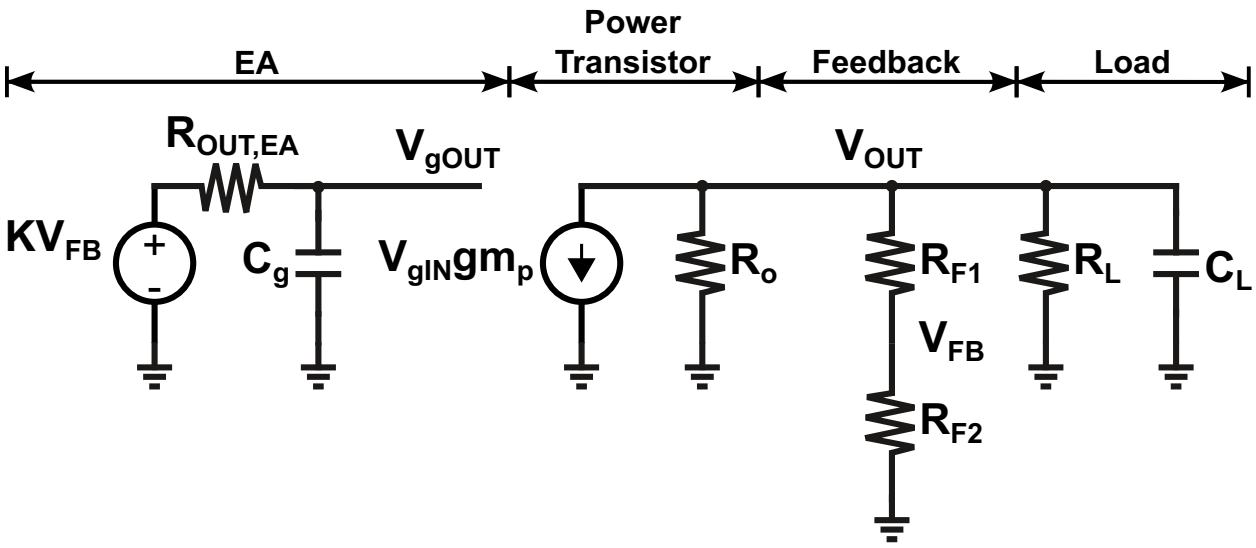


Figure 2.2: ALDO small signal model.

The small signal model of the analog LDO is shown in Fig. 2.2. For the small signal model the main capacitance are located at the gate of the power transistor and the output of the EA represented as C_g and C_L respectively. In order to analyze the open loop transfer function,

the loop must be separated at one point. For this analysis, the control loop is separated at the gate of the power transistor. Based on this small signal model, KCL can be applied to the nodes V_{OUT}, V_{FB} and V_g to obtain the transfer function of the system. The transfer function of the regulator including a single pole model for the EA is represented as:

$$\frac{V_{gOUT}}{V_{gIN}} = \frac{-KR_{F1}R_LR_ogm_p}{(R_{F1}+R_{F2})C_LC_gR_LR_oR_{OUT,EA}s^2} \\ \frac{}{+((R_{F1}+R_{F2}+R_L)R_o+(R_{F1}R_{F2})R_L)C_gR_{OUT,EA}+(R_{F1}+R_{F2})C_LR_LR_os} \\ \frac{}{+(R_{F1}+R_{F2}+R_L)R_o+(R_{F1}+R_{F2})R_L}. \tag{2.1}$$

The transfer function contains a quadratic term in the denominator meaning this system contains two poles. The transfer function can be factorized in order to obtain the pole locations as follows:

$$\frac{V_{gOUT}}{V_{gIN}} = \frac{-KR_{F1}R_LR_ogm_p}{((R_{F1}+R_{F2})CLR_{F2}R_LR_os+R_L+R_o+R_{F2}R_o+R_{F1}R_o+R_{F2}R_LR_{F1}R_L)} \\ \frac{}{(C_gR_{OUT,EA}s+1)}. \tag{2.2}$$

The poles of the transfer function are then represented as follow:

$$\omega_{P1} = -\frac{1}{C_gR_{OUT,EA}} \tag{2.3}$$

$$\omega_{P2} = -\frac{(R_L+R_{F1}+R_{F2})R_o+(R_{F1}+R_{F2})R_L}{(R_{F1}+R_{F2})C_LR_LR_o} \tag{2.4}$$

The first pole of the system is generated at the gate of the power transistor with the output resistance of the EA. The second pole is located at the outout of the A-LDO. The location of this pole varies with the load capacitance and load resistance. If the LDO implemented is capacitor-less then only the paracitic capacitance of the design is introduced at the output. Due to the low capacitance, this pole becomes the non dominant pole as long as $C_g >> C_L$. A load change also affects the pole location where a light load pushes the pole to high frequencies. The minimum load of the LDO is limited by the feedback resistors. At no load,

the output pole of the A-LDO can be represented using:

$$\omega_{P2} = -\frac{R_{F1} + R_{F2} + R_o}{(R_{F1} + R_{F2})C_L R_o}. \tag{2.5}$$

Based on this analysis it can be determined that the main pole contributor of the capacitor less LDO is at the gate of the power transistor and is affected by the controller. It can also be seen that the transient speed of a capacitor-less design is generally faster as it is not limited by the pole located at the output.

2.2 Advantages and Disadvantages

The main advantages of the A-LDO is the good steady state performance. Using an error amplifier with high gain coupled with the continuous analog control of the power transistor, high load regulation and voltage regulation is obtained. This is confirmed from the basic feedback system shown in Fig. 2.3 represented using (2.6). [31, 32]

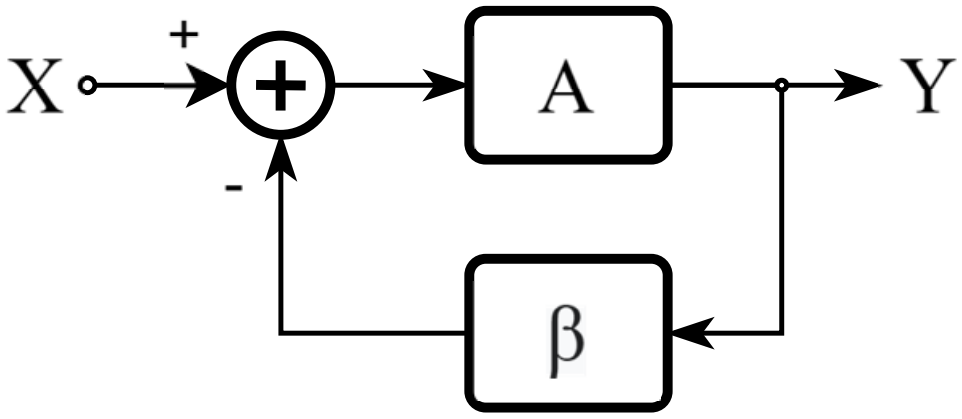


Figure 2.3: Simple feedback network representation.

$$\frac{Y}{X} = \frac{A}{1 + \beta A} \tag{2.6}$$

Where a larger feedback gain β results in less sensitivity to fluctuation in the parameters of A. This can be applied to the A-LDO where the load and power transistor are represented by A and the EA represented by β. The transient performance of the A-LDO very good due to the continuous time operation of the EA. This means that the output is continuously regulated thus an output load change is always compensated as fast as the bandwidth (BW) of the feedback loop. This results in overall lower droop voltages during sharp transient load changes. The excellent transient performance, load regulation and line regulation of the analog LDO also translates to good PSRR performance over a large range of frequencies.

One of the disadvantage of the A-LDO are the high quiescent current consumption. This is caused by the continuous current that is being used by the EA leading to a poor current efficiency. High current designs and low dropout voltage also greatly affects the capability of the A-LDO. The large power transistor required for the high current capability significantly increases the gate capacitance increasing the driving demands of the EA. Similarly, in order to achieve low dropout voltages, the equivalent resitance of the power transistor must be lowered again resulting in a larger power transistor. The increase in power transistor size results in poor transient performance. Furthermore, the shrinking in technology node size has also reduced the intrinsic gain of the transistor and increased the leakage current further limiting the performance of the EA and the A-LDO [31]. In order to improve the performance, a better EA can be used usually at the cost of higher quiescent current. There is then a tradoff between current consumption and transient performance when designing the A-LDO. Due to the analog nature of the A-LDO, it also suffers from instability issues related to the load current and capacitance. As seen from the small signal analysis, one of the pole is reliant on the load current and capacitance resulting in possible stability issues when changing the load current resulting in a more challenging controller design. Since this is an analog design, there is also the disadvantage of scalability. Analog designs do not scale well with process and node changes. This means that the controller design must be modified if the technology node is changed.

2.3 State of the Art Review

In order to improve the performance of the A-LDO a simple approch is to improve the performance of the EA. Increasing the slew rate and bandwidth at the gate of the power transistor results in improved transient response time and lower droop. A common method of improving the performance of the EA while maintaining low quiesent current is to use an adaptive biasing current based on the output error [1, 5, 4, 6]. This enables the EA to have large voltage gain and BW while maintaining low current consumption at light loads. Thus the current efficiency of the A-LDO is improved. When a large load is applied to the A-LDO the biasing current is increased allowing for a faster response and fast settling times. The increased output impedance of the EA at light load results in poor slew rate performance at the gate of the power transistor meaning that a light to high load change will exhibit a larger droop voltage. The adaptive biasing has been further improved using the flipped voltage follower (FVF) reported in [5]. Fig. 2.4 shows the concept of the active biasing EA. The higher gain and BW achieved from the improved error amplifiers also results in

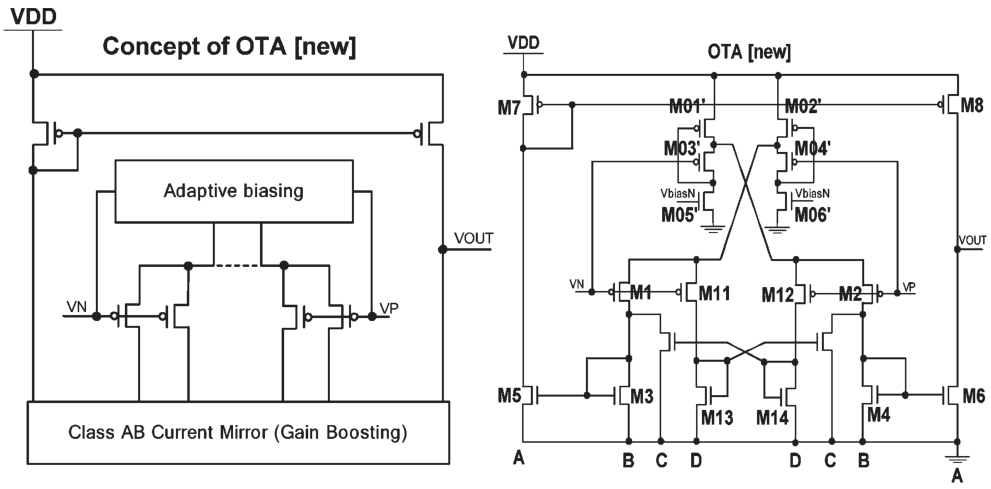


Figure 2.4: Architecture of the actively biased EA using the FVF [5].

an improvement in PSRR performance. The use of an active capacitor to reduce the droop voltage and improve the transient response of the A-LDO has also been explored [3]. The

main advantage of using the active capacitor technique is the reduction of silicon area while obtaining an equivalent large capacitance at the output of the LDO. Significantly reduced transient response and droop has been reported using this technique.

The use of multi-loop topology has been extensively used to improve the transient response [4, 6, 7]. The use of 2 power transistor to enable a light load and high load mode allows for a reduced gate capacitance and improved SR and BW using the same EA architecture and biasing current [4]. The use of a slew rate enhancement circuit to reduce droop and increase the transient response has been extensively explored [7, 4, 5, 6]. In slew rate improvement loops implement an extra derivative path to compensate for sharp changes in the load voltage. In [7], two slew rate enhancement method are used in the form of a super source follower and an extra derivative path using an slew rate enhancement circuit. A current regulation circuit is also added to reduce the droop at the output. The multi loop architecture in [7] is shown in Fig. 2.5.

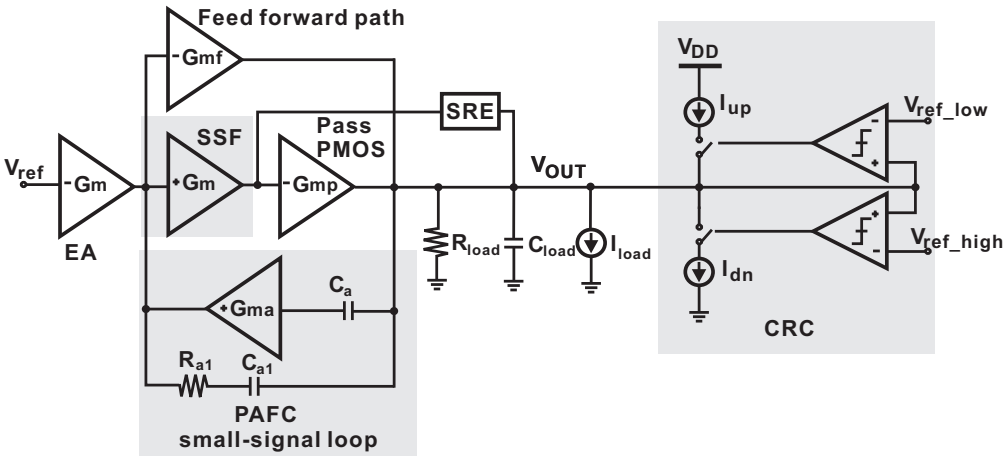


Figure 2.5: Multi loop A-LDO architecture [7].

In order to obtain low droop voltage and fast response time implementing a pole splitting method is utilized such that large bandwidth is achieved while maintaining high slew rate and good stability. Conventional miller compensation can generate a large equivalent capacitor but results in a trade off between stability and bandwidth. The use of an active

capacitor frequency compensation in order to achieve pole splitting while maintaining large bandwidth and good stability has been explored in [7, 6].

The PSRR of an A-LDO can also be improved using different techniques. In [2], relates the cause of PSRR degradation to the gate and parasitic capacitance in the circuit. In order to improve the PSRR, a negative capacitance circuit (NCC) in order to cancel out the gate capacitance of the power transistor is introduced thus isolating the load at high frequencies. This results in the PMOS to be turned off resulting in no path from the supply to the output. The NCC is implemented using an amplifier and feedback resistors. A PSRR of -76 dB at 1 MHz is reported. In [33, 34, 35], the use of a feed forward line filter is used to further improve the PSRR the output. This technique involves the use of a high pass filter to extract the noise information from the supply lines. Then is feed directly to the gate of the power transistor to reduce the effects of supply ripples at the output.

All of these technique are used by state of the art designs to improve the performance of the A-LDO.

2.4 Summary

During this chapter, the analog LDO and its architecture has been explored. The small signal model and generic transfer function have been derived. The advantages of the A-LDO are the excellent line and load regulation along with good PSRR performance. Some of the design challenges of the A-LDO include the high gate capacitance of the power transistors along with the high supply voltages required to obtain large gain. Some of the techniques developed by researchers include the use of improved EA typologies, multiple feedback loops and slew rate enhancement circuits.

Chapter 3

Digital LDO

This chapter discusses the design and architecture of the digital LDO regulators. A review of the D-LDO and an analysis of its controller is presented along with its advantages and disadvantages. Some of the techniques to improve the performance of the D-LDO are reviewed along with state of the art designs.

3.1 Architecture

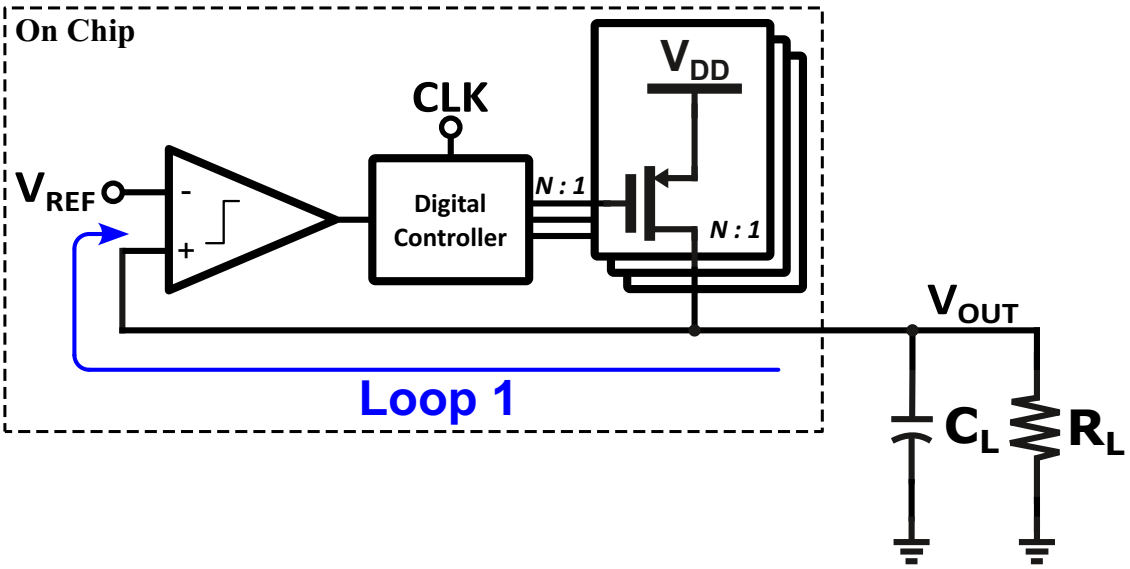


Figure 3.1: D-LDO architecture [8, 9, 10, 11, 12].

Fig. 3.1 shows the basic architecture of the D-LDO. As the name suggests, the digital LDO uses a digital feedback loop to regulate the output voltage. The main components of the basic D-LDO are the voltage comparator, the shift register, and the power transistor array. Similar to the A-LDO, the output load is modeled using a parallel resistor and capacitor. Compared to its analog counterpart the D-LDO can only contol the gate of the power transistor digitally. In order to properly control the output voltage, the power transistor is separated into an array. The control word at the gate of the power transistors determines the number of power transistors activated. Depending on the load, the control word is manipulated such that the output voltage remains close the the desired value. To achieve feedback, a voltage comparator is used to compares the output voltage of the LDO to a reference voltage. At the rising edge of a clock signal, if the output voltage is higher or lower than the reference, the digital controller changes the control word such that the output voltage moves closer to the desired voltage. The process is repeated every clock cycle in order to converge to the desired output voltage. When steady state is achieved, the output voltage cycles above and below the reference voltage. Fig. 3.2 shows a typical D-LDO response simulation where the output voltage starts at 0 V and small load transients change occur. The black dashed lines represent V_{ref} and the target load current. The change in output voltage per transistor is much larger initially compared to when the voltage gets close to V_{ref}. As the output voltage increases, the V_{ds} voltage of the power transistor decreases reducing the current capability of the PMOS transistor, especially when operating in the triode region. The small change in load results in the D-LDO increasing the control word and thus the output voltage. It can be determined that the transient speed is directly proportional to the clock frequency. Increasing the clock frequency can result in higher output ripples.

A general model of the D-LDO feedback can be obtained using the representation shown in Fig. 3.3 [36]. The digital logic is modeled using a gain that samples the output. In the case of a continuous comparator, no gain is achived thus the gain K_D is 1. In the case where an ADC is used to sample the output, the equivalent gain of the circuit can be modeled. In the case where a clocked comparator or ADC is used, an extra Z^{-1} delay may multiply the gain if an extra cycle delay is added. A shift register implements a basic integrator where α represents the gain being applied at each clock cycle. For a basic barrel

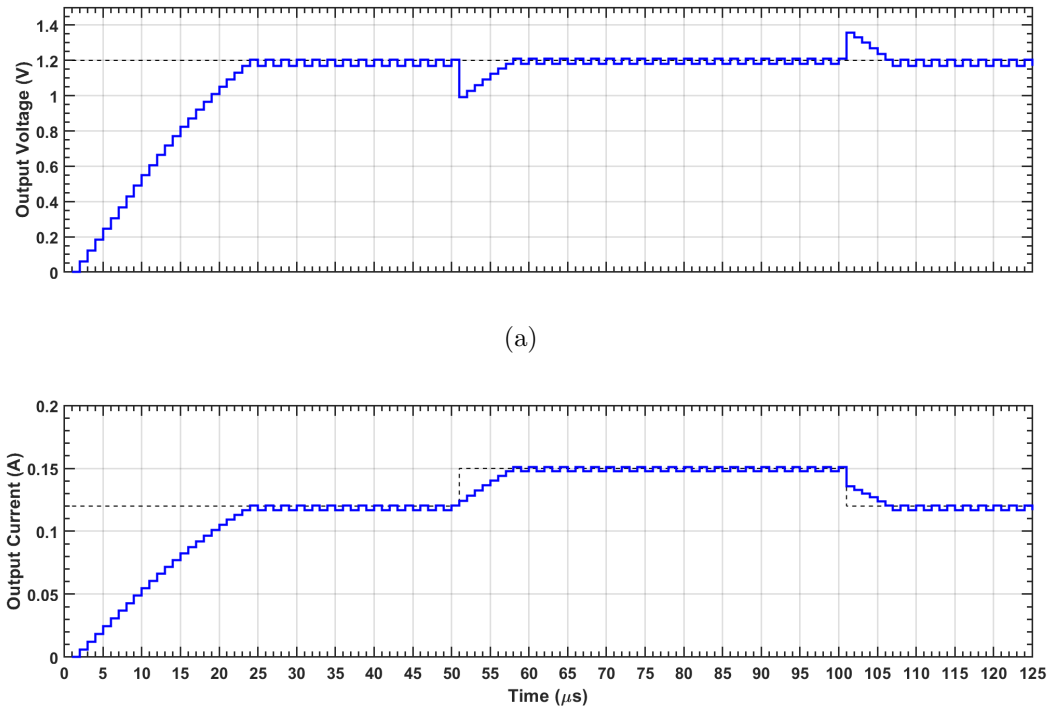


Figure 3.2: D-LDO output waveform using a 1 MHz clock without any C_L a) Output voltage vs time and b) load current vs time.

shift register $\alpha = 1$. The output of the shift register uses a zero order hold (ZOH) to change between output levels. Finally, the power transistor array and the load is modeled using a first order function represented by the load resistance R_L, the load capacitance C_L and the equivalent resistance of all the power transistors R_p. It is assumed that the power transistors are operating in the deep triode region which is often the case for D-LDOs. The shift register transfer function $S(z)$ is represented using:

$$S(z) = \frac{z}{z + \alpha}. \tag{3.1}$$

In order to analyze the transfer function of the D-LDO, the transistor array and the load must be converted from the s domain to the z-domain using the bilinear transform. The z

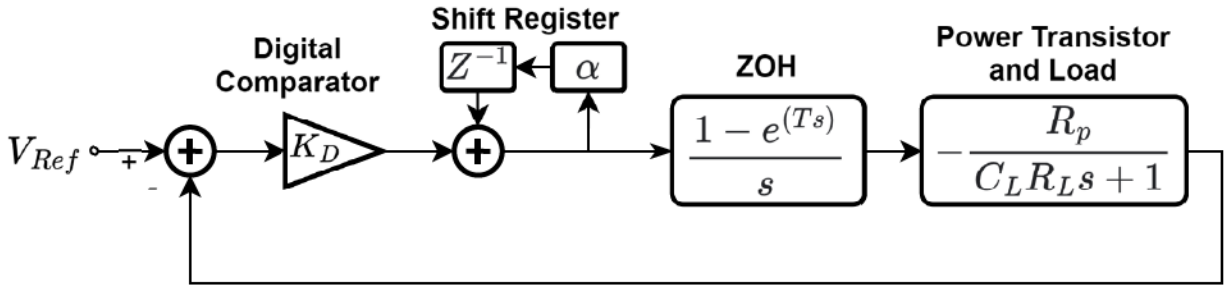


Figure 3.3: D-LDO feedback system using discrete controller representation with a continuous time load.

domain transfer function is represented using:

$$P(z) = R_p C_L R_L \left(e^{\frac{T}{C_L R_L}}\right) \left(\frac{1}{z - e^{\frac{T}{C_L R_L}}}\right). \tag{3.2}$$

The complete transfer function can then be written as the following:

$$G(z) = K_D R_p \left(1 - e^{\frac{T}{C_L R_L}}\right) \frac{z}{(z-\alpha)\left(z - e^{\frac{T}{C_L R_L}}\right)}. \tag{3.3}$$

Where T is the sampling period equal to $T = \frac{1}{f_{CLK}}$. The discrete time pole of the system can be represented using:

$$z_{P1} = \alpha, \tag{3.4}$$

$$z_{P2} = e^{\frac{T}{C_L R_L}}. \tag{3.5}$$

Since this is a discrete time representation of the feedback, the poles must be located on or within the unity circle. Using these equations, the stability of the D-LDO can be investigated based on the design parameters.

3.2 Advantages and Disadvantages

The D-LDO has a few key advantages compared to the A-LDO. First, the D-LDO allows a higher current density compared to the A-LDO. This is the digitally controlled power transistors. When active, they offer superior trans-conductance per unit area compared to a biased transistor such as in the A-LDO. Since the gate of the power transistor is digitally driven, the slew rate due to the large capacitance is no longer an issue as the driving capability can be easily increased without increasing the quiescent current. This allows the digital power transistor array to be switched at much higher speeds. Both of these advantages mean that a very low dropout voltage can be achieved without sacrificing on silicon area for large power transistors and drivers [30, 37].

The input voltage of the LDO does not significantly affect the control circuit of a digital architecture as digital gates can operate at high and very low voltages. Thus the D-LDO is capable of functioning at near threshold input and output voltages where the EA in the A-LDO requires a certain voltage headroom to function properly. The ultra low quiescent current nature of digital gates offer a significant improvement in the current efficiency of the D-LDO. Both of these results in the D-LDO to be ideal for low voltage high efficiency application which is very desirable for modern technologies and devices that operate from battery storage [30, 37].

Using a digital architecture results in the D-LDO designs to be highly scalable with our evolving technology. As the node size changes, digital circuits are significantly easier to adapt to a different processes. Digital circuits are also less sensitive to PVT variations compared to its analog counterpart making them more robust in extreme environments [38].

Using a D-LDO also results in some drawbacks that require improvements in order to obtain adequate performance. First, the D-LDO requires more external circuitry as a clock generating circuit is required increasing the current consumption and silicon area.

The D-LDO does not suffer from stability issues such as the A-LDO, intead the D-LDO suffers from limit cycle oscilation (LCO). When the optimum control word is achieved, the output will still fluctuate around the target output as it continuously oscillates around

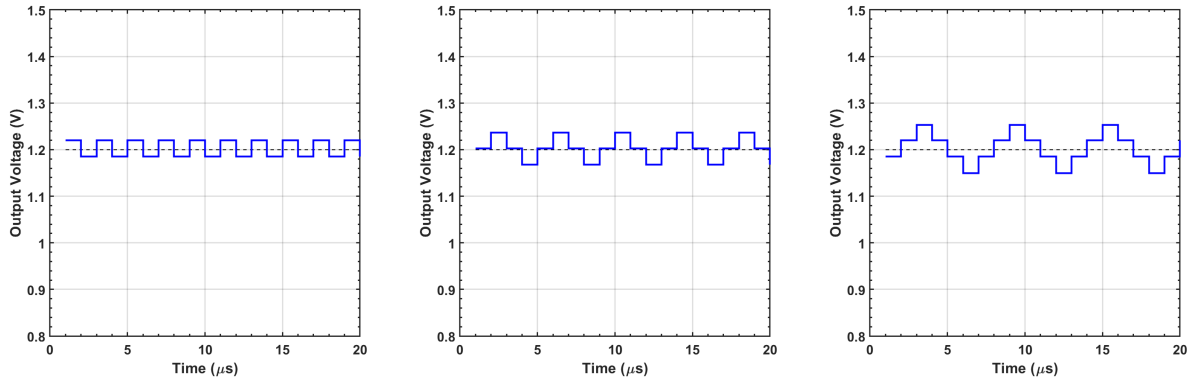


Figure 3.4: D-LDO operating in different LCO modes during static load a) LCO mode 1, b) LCO mode 2 and c) LCO mode 3.

the desired voltage. If the control word fluctuates by 1 around the target voltage this is known as mode 1 LCO as shown in Fig. 3.2. If the control word oscillates with a variation of 2 then this is known as mode 2 LCO. Higher mode of LCO is less desirable as the output will contain a larger ripple. An example of the mode of the LCO is shown in Fig. 3.4. The mode of the LCO depends on many factors such as clock frequency, load capacitance, load current and controller design.

The power transistor array and digital control introduces a quantization error significantly reducing the load regulation of the D-LDO. Due to the power transistor array being able to only generate a limited number of states, an error is introduced. This error is determined by the resolution of the power transistor array and the current requirement of the load. If the load current is low and only a few transistors are active then the error will be large as the relative step of each transistor is large compared to the load current. The quantization error also results in the D-LDO to require a minimum load current to be able to regulate the output current. The error is significantly lower when operating at large current as each transistor only changes the current slightly. Eq. (3.6) relates the output voltage to a change to the control word. Where $V_{Out,I}$ is the initial output voltage, N_I is the initial control word and N is the amount added to the control word. Based on the equation, the change in output voltage decreases with N_I which is proportional to the load current. The

quantization error results in poor load regulation and a trade off between array resolution and transient speed.

$$V_{Out} = \frac{V_{Out,I}(N_I + N)}{N_I} \tag{3.6}$$

The D-LDO samples the output based on the clock frequency resulting in poor transient performance during fast load change. In order to maintain good performance the clock period requires to be more than 5 times smaller than the fastest load transient on the output. An increased clock frequency improves the transient performance but may degrade the LCO performance and increase quiescent power consumption resulting in a performance trade off. The poor transient performance, LCO, non-continuous sampling and quantization error results in the LDO to have poor PSRR performance making the classical D-LDO unusable for low noise applications.

3.3 State of the art Review

To overcome some of the performance issues attributed to the D-LDO many techniques have been developed to improve upon the basic D-LDO architecture. The most common techniques used in the state of the art designs are reviewed next.

3.3.1 SAR Algorithm

The classical D-LDO described above uses a simple linear search algorithm (also called the hill climb algorithm) where after each clock cycles an equally sized transistor is added to the output. This requires many clock cycles to activate or shut off the entire array equal to the resolution of the power transistor array. To reduce the number of clock cycles required and increase the transient response time, the successive approximation register (SAR) algorithm is used. This algorithm has been widely used in analog to digital converters (ADC) [39, 40, 41, 42]. Using this algorithm, a binary sized array is used. During a load change on the output, the MSB of the array is initially activated or deactivated, depending

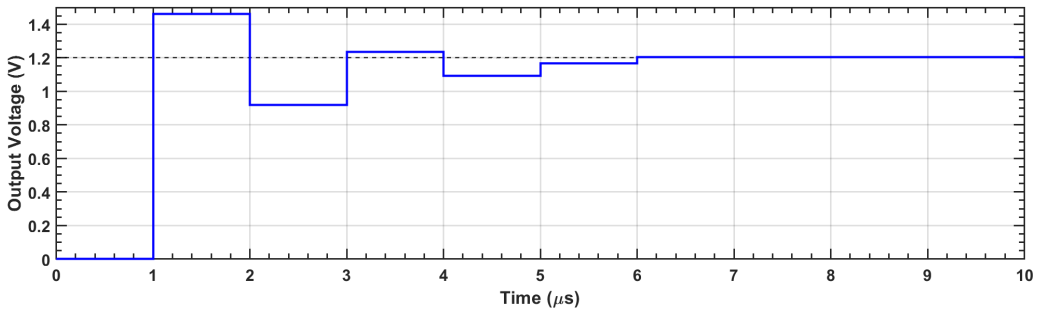


Figure 3.5: D-LDO using the SAR algorithm control method.

on if this an undershoot or overshoot situation. During the next cycle the MSB-1 is activated and the MSB bit is kept active if the output did not cross the refrence. If the output does cross the refrence then the MSB bit is deactivated. The cycle continues until the end of the array where the proper control word is found. Fig. 3.5 shows an example of a D-LDO output using the SAR algorithm. This method significantly increases the speed of convergence of the D-LDO equal to the number of bits of the array. For example, a 5 bit array converges in 5 cycles while the hill climb algorithm takes a maximum of 32 cycles with an average of 16 cycles. The main draw back of the SAR algorithm is the large overshoot and undershoot present at the output of the LDO as the algorithm converges. The SAR algorithm also suffers from accuracy issues due to the nonlinear nature of the power transistors where the best state can be missed during convergence. In [12], the large overshoot is avoided using a high clock frequency in combination with a PD controller. In [8] the SAR algorithm is used to perform the final convergence increasing the accuracy while maintaining fast transient response time and minimizing the effects of overshoot.

3.3.2 Coarse-Fine Transistor Array

The coarse fine trasistor array technique aims at improving the transient response time of the D-LDO and has been widely used [8, 11, 10]. This technique involves generating multiple linear transistor arrays of varying size. Using two arrays one of the array uses larger transistors capable of rapidly changing the voltage output during load transients. Once the coarse calibration is complete, the fine transistor array is able to fine tune the output to

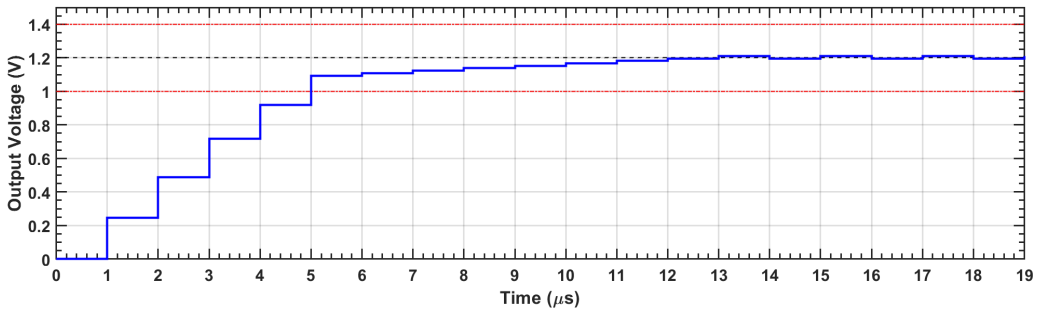


Figure 3.6: D-LDO using the coarse fine transistor array and a window detection method represented my the red lines.

increase the precision and attain improved resolution. This significantly increases the speed of convergence of the D-LDO. In order to determine the mode of operation, a window is often created. When the output voltage is outside the defined window, the coarse array is used. Once the output voltage approaches the desired target voltage, the fine array is used. This technique can be be used with more than 2 arrays but significantly increases the controller complexity as more arrays are added with diminishing returns on performance. Fig. 3.6 show an example transient using the coarse fine transistor array technique.

3.3.3 Exponential Weighted Transistor Array

As mentioned above, the resolution of the D-LDO is better as the load current increases due to the step size decreasing as more transistors are added. The size of the power transistor array can be exponentially sized such that the output voltage change for each added transistor is equal. [43] This also increases the usable current range of the D-LDO. The constant and the ratio of the transistor array can be approximated using (3.7) [43]. It can be seen that the ideal constant is dependent on the desired output voltage making this method better for a fixed output voltage regulator.

$$S(n) = q^n \tag{3.7}$$

Where $S(n)$ represent the size increase from the LSB power transistor and n represents the control word. The output voltage change after each addition of $n + 1$ can be approximated

using:

$$\Delta V(N+1) = \frac{(q-1)V_{OUT}V_{DO}}{qV_{OUT}+V_{DO}} \approx V_{DO}\frac{q-1}{q}. \tag{3.8}$$

Where the approximation assumes a large N is used. In general a q value of 1.02 is used for most designs.

3.3.4 Freeze Mode

During steady state operation the classic D-LDO architecture has an intrinsic ripple on the output above and below the desired voltage generating an LCO mode. This oscillation generates ripples on the output and consumes extra quiescent current to charge and discharge the gate of the power transistor. In order to obtain improved regulation a freeze mode is added eliminating the ripple and maintaining a constant control word [8, 43]. An extra circuit is added to detect the presence of LCO and stop the evaluation of the output. When a load transient occurs the LCO detector must re-enable the calibration. The control of the freeze mode requires extra attention as it must be able to properly detect LCO as well as rapidly enable the calibration only during transient load change. If too large of an error is present to determine transient load changes, then a large error will be seen at the output reducing the load regulation performance of the D-LDO.

3.3.5 Variable Sampling Frequency

Increasing the clock frequency on a D-LDO design will allow faster transient response while resulting in higher quiescent current consumption and possibly degraded LCO performance. In order to increase the transient speed while not significantly increasing the current consumption a variable clock technique can be employed [9, 11, 10, 44]. During steady state operation the LDO can operate at a low frequency as adjustments on the output are not required. When a load transient is detected, the clock frequency is increased to improve the transient response and quickly return the output voltage to the desired value. Once steady state is achieved the clock frequency is subsequently reduced again. When operating at low frequency, the clock period must be smaller than the expected transient slew rate of the load

change. This is to ensure that the high frequency sampling can be enabled before the droop becomes too significant. Another option is to use a window method as in the coarse fine technique. This technique contains the draw back of low transient response when subject to a small load step.

3.4 Summary

During this chapter a comprehensive overview of the digital LDO is presented. The general architecture and z-domain transfer function was analyzed. The advantages and limitation of the D-LDO were explored along with the state of the art designs with their implementations to improve the performance of the D-LDO.

Chapter 4

Hybrid LDO

This chapter pertains to design of hybrid LDO regulators. This type of LDO regulator implements both an analog and digital circuit in order to improve the performance of the LDO regulator. The architecture and design of the hybrid LDO is introduced followed by state of the art designs and their implementation methods.

4.1 Architecture

In the previous two chapters the analog and digital approach to the LDO regulator have been explored along with their advantages and disadvantages. In an effort to further improve the performance, a hybrid configuration has been explored where both methods are used in the same design. The main goal is to obtain the advantages of both architectures without their respective deficits. Hybrid LDO can be further classified as analog assisted digital (AAD) and digital assisted analog (DAA) [45]. The AAD-LDO will implement a D-LDO with an analog portion to "assist" the digital portion to increase the performance usually the loop bandwidth and slew rate limitation of the A-LDO [45]. Similarly, the DAA-LDO implements an A-LDO with a digital circuit to improve the performance. In order to determine the type of H-LDO being implemented, one can look at the control method at the gate of the power transistor or the control method driving the main current to the load. One of the basic configuration of an H-LDO is the implementation of a D-LDO and A-LDO in parallel as shown in Fig. 4.1. In this architecture, both the digital and analog portion supply

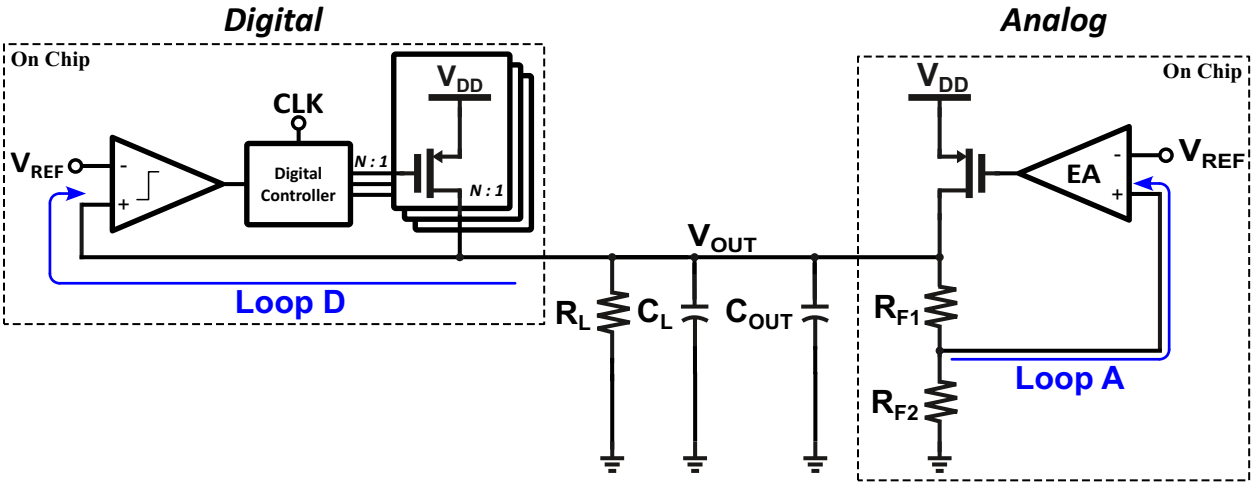


Figure 4.1: H-LDO architecture [13].

a constant current to the load. Depending on the ratio of load current, this architecture can either be AAD or DAA design, where most often case the use of a AAD-LDO is used in order to save on quiescent current consumption.

4.2 Advantages and Disadvantages

The main advantages of the H-LDO is the capability of improving the performance compared to a design that is not analog or digitally assisted. Depending on the design implemented, the hybrid LDO architecture is capable of achieving improved performance without some of the drawbacks of the standalone D-LDO and A-LDO. In most cases, the addition of an AAD-LDO results in improved PSRR, load regulation, line regulation and output ripple that stem from the discontinuous operation of the standalone D-LDO [45]. The addition of an analog circuit results in continuous operation of the loop improving response. The analog loop can be implemented using passive components or active components. Using the passive components often result in lower quiescent current. Similarly, DAA-LDOs result in the A-LDO to obtain larger loop gain and improved slew rate using the digital circuit [45].

Both implementation method of the hybrid LDO result in increased complexity and design. For example, when designing the analog portion of the AAD-LDO, extra care must be taken to ensure that the low quiescent current and low input voltage operation is maintained. If these performance metrics are not maintained, part of the advantage of the D-LDO is lost. When implementing an H-LDO such as the one implemented in Fig. 4.1, extra control circuitry must be added in order to ensure that both loops can function together. For example, if one loop responds faster than the other, there can be a case where all the current is supplied by one power transistor if controller intervention is not implemented. Thus stability and loading become an important factor when multiple loops are operated in parallel.

4.3 State of the Art Review

In the following section, some state of the art implementations of different H-LDOs are explored.

In [14], a low voltage, capacitor less AAD-LDO regulator is implemented. This design implements a 3 level coarse-fine control method for the D-LDO to achieve fast transient response. Two analog loops are added to improve the performance of the regulator. First, the use of an NMOS power transistor is used instead of the conventional PMOS design. The complementary power transistor results in the source being connected to the output voltage. During an undershoot condition, the lower voltage at the source of the NMOS result in a larger V_{gs} voltage increasing the gm of the transistor. The increased gm results in more current flowing to the load increasing the output voltage and significantly reducing the droop. An improvement of 19% in the I-V characteristics of the NMOS is reported in [14] significantly reducing the droop voltage. The intrinsic analog loop of the NMOS also results in extremely large bandwidth. In order to drive the NMOS, a higher than V_{DD} voltage is generated using a charge pump. The second analog loop implements a NAND gate based high pass analog path. During a sharp load transient, the high pass filter formed from by C_c and R_1 will reflect the output voltage change at the input of the NAND gate. If the

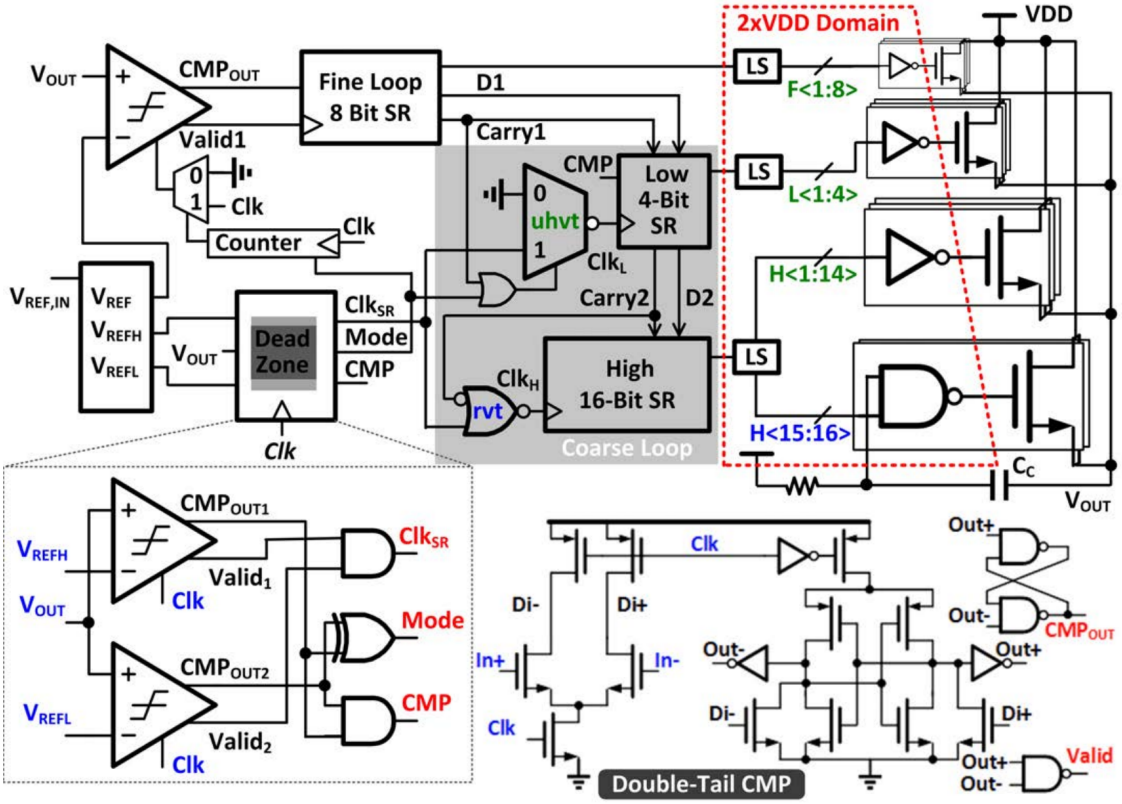


Figure 4.2: Architecture of the NAND base LDO with NMOS power transistors [14].

voltage drops below the threshold of the NAND gate the output transistor is then activated increasing the output voltage. This results in a closed loop system biasing the gate of the power transistor close the the threshold voltage of the NAND gate. The digital control then activates and increases the output voltage to the desired voltage. The NAND based loop is only used for undershoot as during overshoot the state of the NAND gate remains the same. Using both of these loops together, the droop is reduced to 244 mV compared to the 426 mV using the traditional PMOS array. Fig. 4.2 shows the design implementation of the H-LDO.

A low voltage capacitor less AAD-LDO regulator is implemented in [46] using simple digital LDO with a 7 bit barrel shift register connected to equivalently sized power transistors. In order to quickly drive the gate of the power transistors, inverters are used. The analog loop is introduced similarly to [30] connecting the pull down network of the inverter to the

output of the EA. This then creates the analog feedback where the active transistors from the digital section have a gate voltage equivalent to the output of the EA. A loop controller is used to control the analog and digital operation. During steady state, the analog control is allowed to function increasing the accuracy and PSRR of the LDO. When a large load transient occurs, the analog loop is kept at a constant and the digital loop is enabled. The gate of all the digital transistors is tied to a biased voltage during digital calibration to reduce the chance of glitches. When the digital calibration is complete, the analog loop is enabled. When steady state is achieved, a freeze mode is enabled to reduce the current consumption.

In [13], a capacitor less AAD-LDO for high current applications implementing a digital LDO in parallel with an analog LDO is realized. The digital control uses the window method to enable the barrel shift register to regulate the output. After a load change, the analog portion would saturate, either close to VDD or GND depending on the load direction. In order to have the correct offset for the analog LDO, a window method is also added to the gate of the analog power transistor. Once the output voltage is within the defined window, the gate voltage is monitored and the digital control word is changed in order to be within the desired window. This results in the gate voltage of the analog to always be biased to the desired level such that the analog portion can regulate small noise and load change. To improve the current efficiency, a clock gating approach is used where the clock frequency is reduced by half during steady state operation.

In [47], a clock-less AAD-LDO regulator using a residue current lock control scheme is implemented. This control method uses the gate voltage of the EA to determine when to increase the control word of the digital section to ensure that the residue current can be controlled by the analog LDO. A window method of detection is used to determine the residue current level. When the gate voltage is outside the desired window, a signal via two comparator is sent to the asynchronous digital control. The analog LDO uses a flipped voltage follower architecture to boost the driving capability of the EA. The digital control uses a 128 bit unary transistor array with an asynchronous point shift register. In order to reduce LCO, a digitally controlled delay line is implemented limiting the activation speeds of the point shift register. The delay is dependent on the control word of the power transistor

array where larger currents results in larger delay. The delay is tunable from 290 ps to 1.65 ns resulting in an effective clock frequency of 600 MHz.

An AAD-LDO regulator targeting fast transient time and low clock frequency is implemented in [30]. This design uses a 3 level coarse-fine control implementation for the digital LDO. This design also implements a freeze mode to increase the current efficiency of the design. The analog loop is implemented to increase the current supply capability of active transistors to reduces the droop voltage. This is implemented using a high pass filter connected to the LDO output. The output of the high pass filter is connected to the pull down network of the inverters driving the PMOS power transistors. During normal operation, the deactivated PMOS transistors are connected to VDD using the pull up network of the inverter. The activated transistors are connected to the output of the high pass filter which is connected to ground during steady state operation. When an undershoot occurs, the droop voltage is reflected at the output of the high pass filter pulling the gate of the PMOS below the ground voltage increasing V_{gs}. This results in a larger current, reducing the droop voltage. This analog loop only affects the active transistors using the pull down network meaning that it has little performance gain at low currents. In order to reduce the start up time of the high pass filter, a transistor is added to provide an extra path quickly charging the capacitor. In order to minimize area, the size of the capacitor and resistor are specially chosen based on the expected load edge times.

In [48], an AAD-LDO regulator utilizing a gate drive control technique in order to increase the current range and transient speed. This design implements a 256 bits unary sized NMOS transistor array taking advantage of the intrinsic analog loop of the NMOS transistor. The gate driving strength modulator (GDSM) increases or reduces the gate voltage of the power transistors when a load change is detected. The GDSM control is implemented in two method; a time driven control and an event driven control. The time driven control changes the gate voltage until the output control word is within 50 and 70 % of full load. Thus in a steady state operation at least half the transistors are active enabling better regulation via the NMOS intrinsic loop as well as the event driven control reducing the overshoot. The event driven loop uses a window method to control the GDSM, when the output voltage

is outside the window, the driving strength is instantly changed in order to maintain the voltage close to the target voltage.

In [49], an DAA-LDO regulator that uses a digital computation algorithm to determine the desired control word is implemented. When a load increase occurs, the power transistor is initially completely turn on increasing the voltage to a certain threshold where the power transistor is then completely turned off. The output voltage then returns to the initial threshold. The time for the output voltage to rise and fall can be used to calculate the desired control word for the power transistor as follow:

$$I_{load} = I_{max} \frac{T_1}{T_1 + T_2}. \tag{4.1}$$

Where T_1 is the time when the power transistor is completely active and T_2 is the time where the transistor is completely off. Due to some non-linearity the solution of the control word can be incorrect thus multiple cycle are sometimes needed to converge to the desired output voltage. To reduce the possibility of oscillations, an α value is added to the solution to calibrate the feedback system and improve the settling times.

4.4 Summary

This chapter covered the general architecture of H-LDOs and some their implementation. H-LDOs were sub categorized in analog assisted digital and digital assisted analog LDOs. The common state of the art H-LDO implementations were reviewed at the end of the chapter.

Chapter 5

The Dual Loop Current Feedback LDO

This chapter discusses the design and methodology of our research on an A-LDO using a dual loop architecture using a current and voltage feedback loop. The A-LDO is simulated and layout using the Cadence software. The proposed A-LDO is fabricated in a TSMC 180-nm standard CMOS technology and the performance was measured on a custom PCB board.

5.1 Objective

Our research on the A-LDO focused on the implementation of high transient speed, high current cap-less LDO regulators. The targeted application of this design include memory, central processing units (CPU), automotive, industrial and SoC applications. The designed LDO is to operate at a 1.8 V supply and 1.2 V output capable of handling 500 mA and have a fast transient response while maintaining stability.

5.2 Proposed Design

The proposed transistor level diagram of the dual loop capacitor less LDO is shown in Fig. 5.1. The voltage feedback loop is composed of a voltage divider, R_{F1} and R_{F2}, an EA amplifying the error and applying a current signal to the low impedance input of the CFOA. This current signal is then further amplified and translated to the gate of the power

transistor. The current feedback is formed from the resistor R_s at the output of the regulator to the input of the CFOA at node x. A feedback resistor R_F is added between the input and output of the CFOA to improve the transient response time and provide feedback for the CFOA and the line filter. To improve the PSRR performance of the A-LDO, a feed-forward line filter is implemented injecting a canceling signal at the gate of the power transistor.

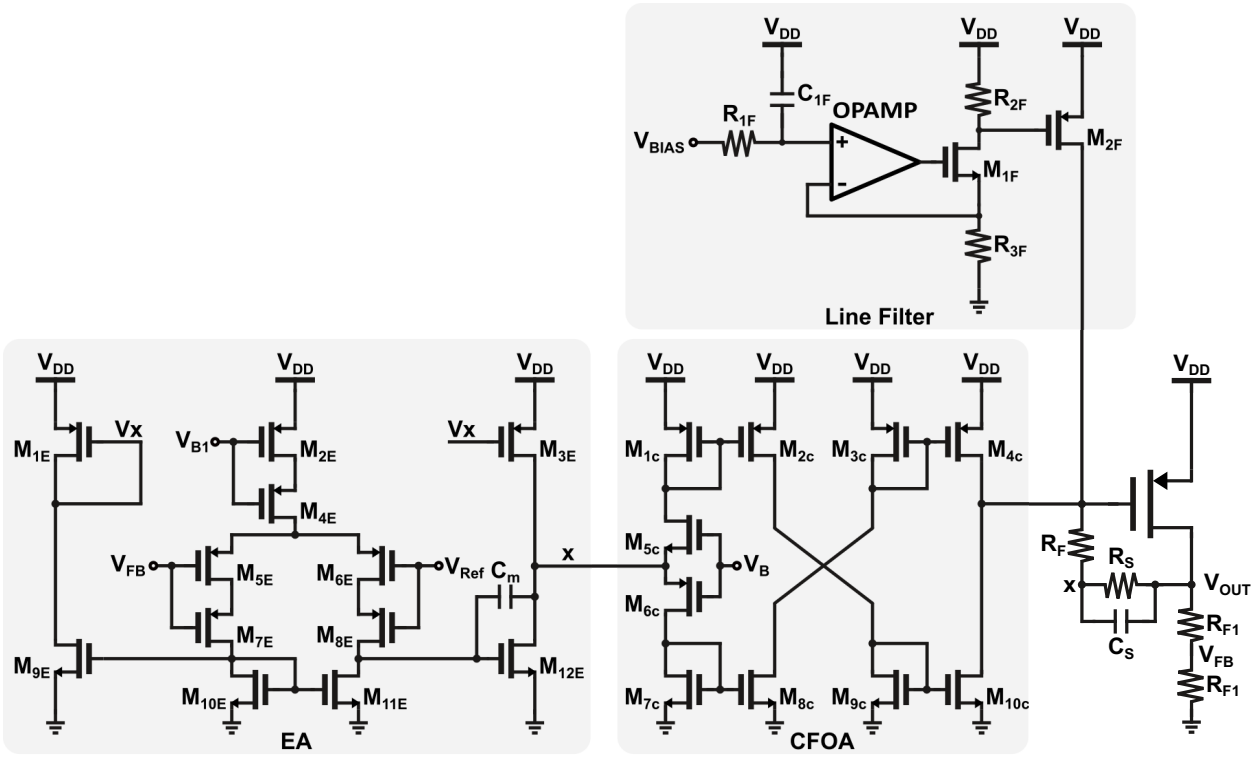


Figure 5.1: Dual loop cap-less LDO transistor level circuit diagram.

As discussed in the previous section the gate driving capabilities of the control system generates a design challenge for the A-LDO in application that require a large power transistor. The conventional method uses a voltage feedback loop to regulate the output, for our design the current feedback loop is introduced. Current feedback allows for a much faster response as it does not have the same slewrate issues as the voltage feedback. Thus in general, current feedback provide a faster response time compared to the voltage feedback. To leverage the advantages of the current feedback loop, the current feedback operational

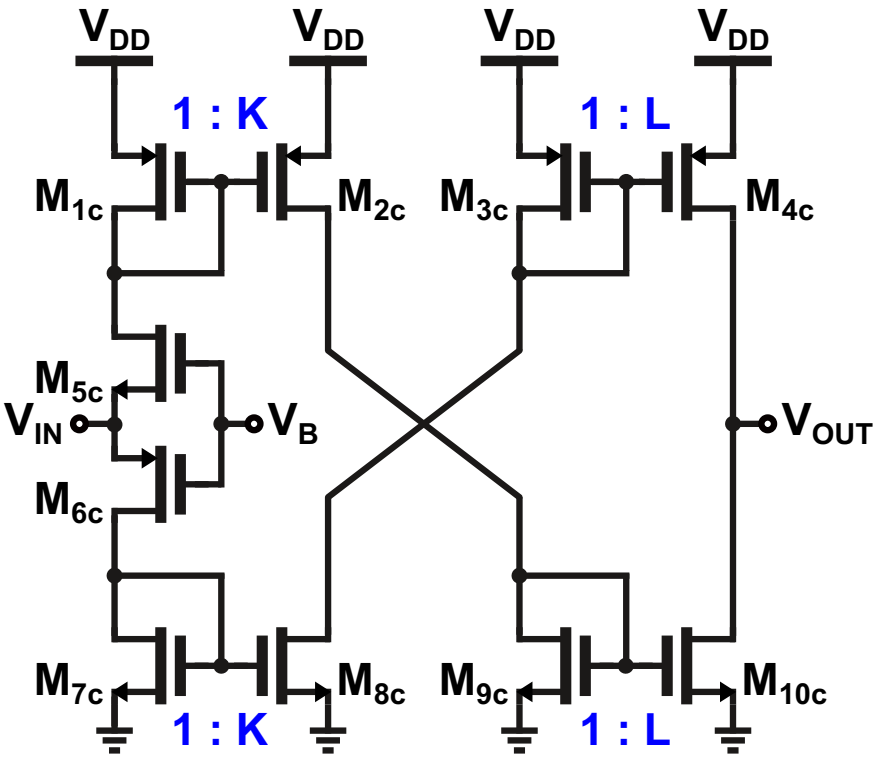


Figure 5.2: CFOA transistor level circuit diagram.

amplifier (CFOA) is used in order to amplify the error. Since the feedback of the CFOA is a current driving output, the slew rate and driving capability are drastically improved compared to the conventional operational transconductance amplifier (OTA) that conventionally form the EA. For our design, the CFOA is implemented using 2 stages of current mirror providing current amplification as shown in Fig. 5.2. The current amplification gain can be determined using:

$$F = K \times L. \tag{5.1}$$

Where K and L are the ratio of the current mirrors of the first and second stages respectively. The CFOA amplifies the current from the input V_{IN}. The V_B input is used to adjust the input stage of the CFOA controlling the amount of current that passes from the supply voltage to GND. This enables the CFOA to adjust the output current. It is important to note that the V_{IN} input of the CFOA is a low impedance node.

The A-LDO design would require a large current amplification in order to improve the output precision. Using only a CFOA in this design is undesirable as larger current amplification results in large quiescent current consumption. In order to reduce the current requirements of the CFOA, a low current amplification is used. This then presents a problem where fast transient response is achieved while low load and line regulation are seen in steady state. To remedy this situation a dual feedback loop architecture is used. The first loop is implemented via the current feedback loop mentioned previously, and the second loop is provided by a more conventional voltage feedback in order to provide large gain feedback and improved static performance. In order to take advantage of the driving capability of the CFOA, the voltage feedback loop feeds a small current into the V_B input changing the output voltage. The voltage feedback loop is implemented using a 2 stage amplifier. The first stage is a classic differential amplifier proceeded by an OTA converting the differential signal to a single ended output. Since the output of the EA is connected to the low impedance node of the CFOA, the ouput of the EA must have good current driving capability. This means that the gain introduced by the second stage is not very high due to the low output impedance. In order to achive large gain the first stage uses a cascode connection for the input transistor pair as well for the current source transistors. The cascode configuration increases the output resistance of the input transistors increasing the gain. This results in better gm performance and larger r_o increasing the intrinsic gain of the transistor increasing the gain of the amplifier [31]. The main draw back using the cascode configuration is the increased voltage headroom requirements. In order to maintain all the transistors in the saturation region, all the V_{ds} conditions must be satisfied. For this design, the nominal 1.8 V supply voltage used allows enough headroom to satisfy all the conditions and maintain high gain. The transistor level circuit of the implemented EA is shown in Fig. 5.3

With the CFOA and EA, they must be connected to the power transistor in a manner that enables the current loop and voltage loop to function as desired. First lets take a look at the CFOA and the current loop. The output of the CFOA is connected to the gate of the power transistor. The output of the CFOA drives a current thus a current path must be provided in order to convert the current signal to a proper voltage for the gate of the power transistor. The current path can be provided in many ways, the first intuition is to

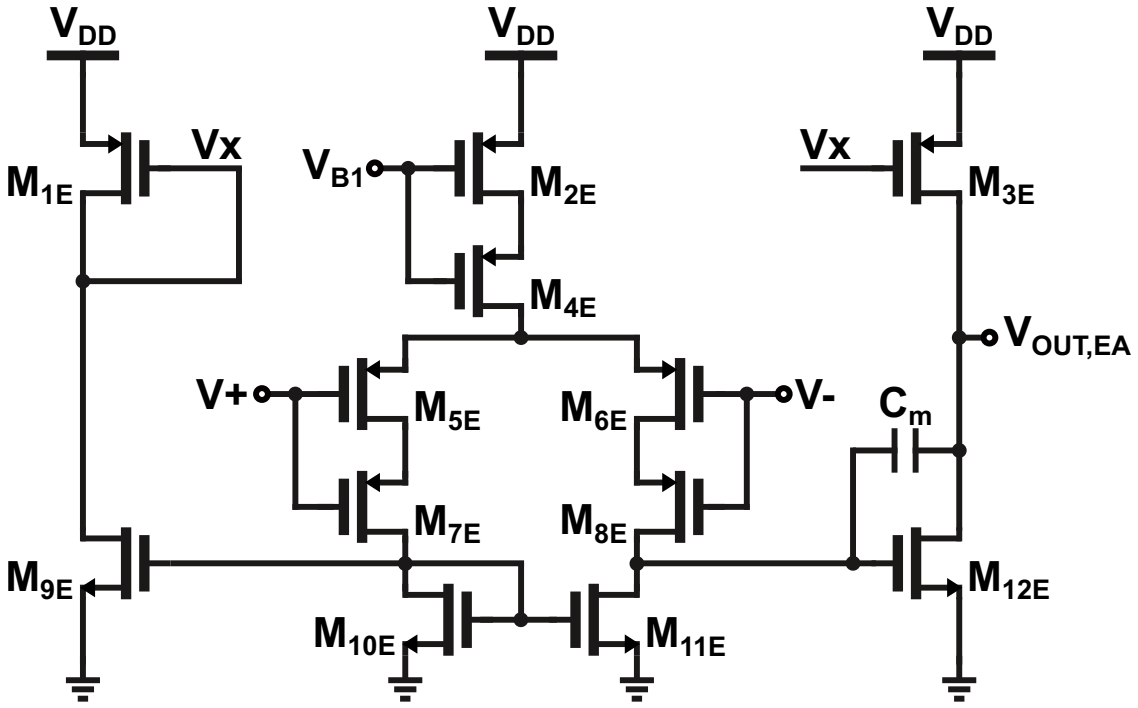


Figure 5.3: EA transistor level circuit diagram.

connect a resistor from the output to GND. This would provide the desired current path but would waste all the current that is being provided by the CFOA. A better alternative is to connect a resistor from the output to the low impedance input of the CFOA. This results in a feedback loop increasing the response of the CFOA. This effectively recycles the current from the output back to the input. In order to provide current feedback, a current path from the output of the power transistor and the input of the CFOA is created via a resistor. The simplified schematic of the current feedback loop is shown in Fig. 5.4.

To ensure a negative feedback loop is implemented, an analysis is conducted. During an increase in load, the voltage at the output drops. This causes the current flowing in R_s to drop. This drop in current results in a drop in output current as well further being reduced by the current from R_f. The reduction in current results in the gate voltage of the error amplifier to be reduced. A reduction in gate votlage on the PMOS power transistor increases the transconductance increasing the current being supplied at the drain. The increased current supplied to the load results in an increase in output voltage. Since the stimulus and response are in opposite directions, this is a negative feedback system. It can

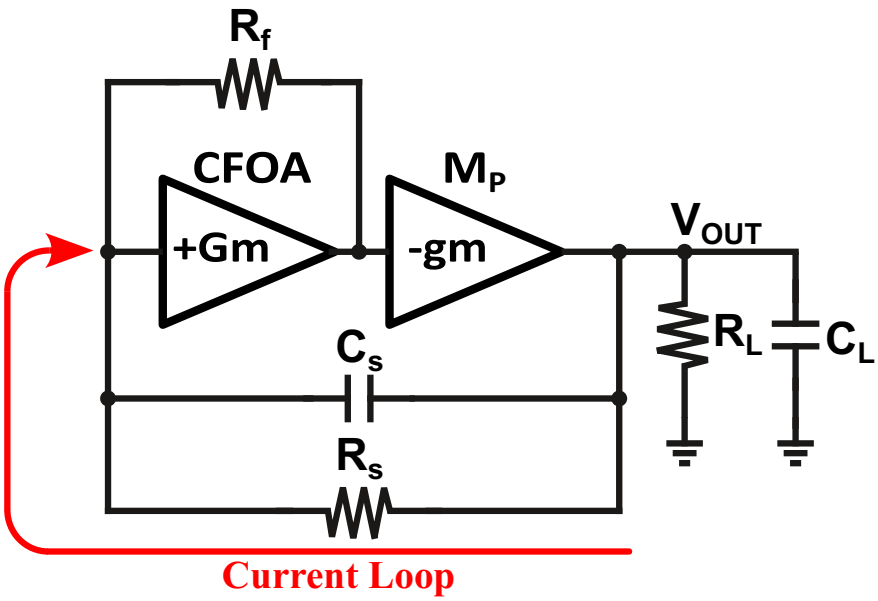


Figure 5.4: Simplified model of the current feedback loop.

be noticed that the local feedback provided by R_f results in a positive feedback loop. This does not lead to instability as it is a weak feedback compared to the negative feedback loop provided from R_s. Thus, R_f helps increase the initial response step and the negative feedback dominates afterwards.

With the current loop integrated, the voltage feedback loop is implemented as well. The EA is connected to the input of the CFOA. In order to provide feedback a voltage connection must be added from the output back to the input of the EA. First let's consider a direct connection from the output to the EA input. This would provide a voltage feedback equal to the output voltage. The EA in Fig. 5.3 uses a PMOS input transistor pair that operate in the saturation region where 2 conditions must be meet; $V_{sg} > V_{th}$ and $V_{sd} > V_{gs} - V_{th}$. The latter condition can be meet by modifying the transistor size of the EA.

In order to meet the first condition we can investigate the V_{sg} equation for the input transistor shown in (5.2). The first condition states that the V_{sg} must be larger than the threshold of the transistor which is about 400 mV in the 180 nm node process provided by TSMC. More modern nodes and special transistor masks can have a V_{th} of about 200 mV. Since this is an LDO regulator we can expect the minimum voltage difference between the

supply and output to be about 200 mV. In order to meet this condition we would require to satisfy (5.3) which is not doable with positive values of $V_{ds_{M2E}} + V_{ds_{M4E}}$.

$$\begin{aligned} V_{sg} &= V_s - V_g \\ &= (V_{dd} - V_{ds_{M2E}} - V_{ds_{M4E}}) - (V_{dd} - V_{DO}) \\ &= V_{DO} - V_{ds_{M2E}} - V_{ds_{M4E}} \qquad (5.2) \\ V_{th} < V_{sg} &< V_{DO} - V_{ds_{M2E}} - V_{ds_{M4E}} \qquad (5.3) \end{aligned}$$

Thus connecting the voltage feedback directly to the output is not a viable option as the transistor cannot operate in the saturation region. In order to meet the first condition V_{sg} must be reduced. A reduction in source voltage cannot be done as the previous analysis indicated that a negative voltage would be required. In order to achieve a lower V_{sg}, the V_g must be reduced. The simplest and most effective method for reducing the output voltage is to use a restive voltage divider. Adding a voltage divider has 2 benefits; reduces the voltage at the gate of the feedback and introduces a minimum load current to the LDO that increases light load stability. The stability conditions will be further analyzed in the stability section. With the voltage divider in the feedback loop, let's analyze the voltage divider ratio in order to fulfill the requirements of the EA. The V_g voltage in (5.2) can be modified to include the voltage divider represented as follow:

$$\begin{aligned} V_{sg} &= V_s - V_g, \\ &= (V_{dd} - V_{ds_{M2E}} - V_{ds_{M4E}}) - A_{div}(V_{dd} - V_{DO}), \qquad (5.4) \\ A_{div} &= \frac{R_{F2}}{R_{F1} + R_{F2}}. \qquad (5.5) \end{aligned}$$

Where A_{div} is the voltage attenuation ratio of the voltage divider. This can be solved for A_{div} in order to determine the minimum ratio required for the design parameters as follow:

$$A_{div} = \frac{V_{dd} - V_{sg} - V_{ds_{M2E}} - V_{ds_{M4E}}}{V_{dd} - V_{DO}}. \qquad (5.6)$$

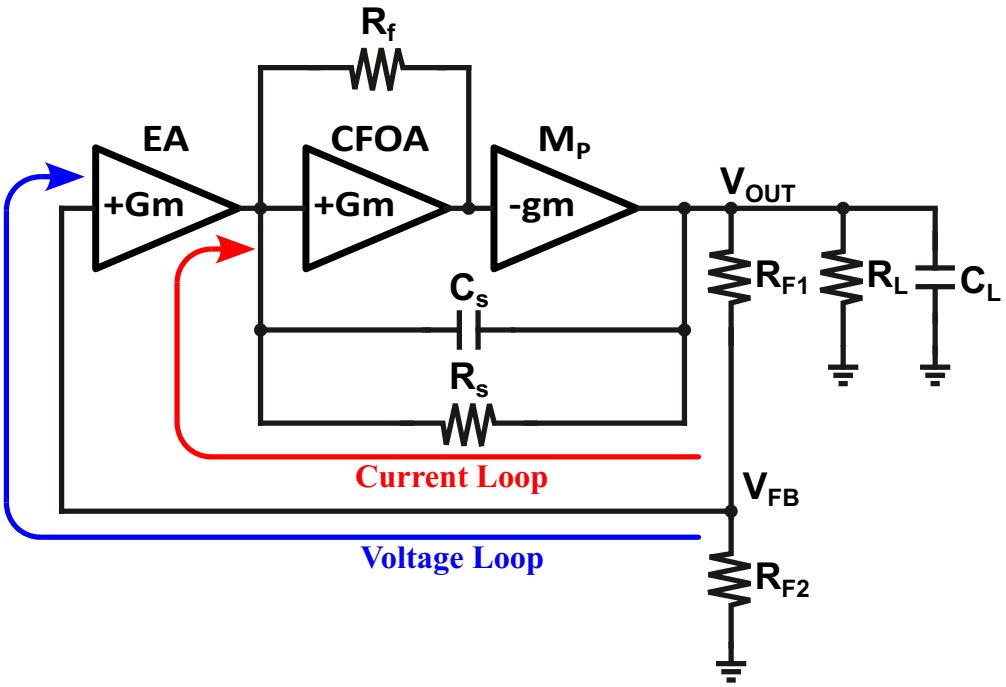


Figure 5.5: Simplified model of the voltage feedback loop.

Adding a voltage divider also has some nuisance on the performance of the design as the voltage divider adds some attenuation to the voltage feedback loop reducing the overall open loop gain of the system. It is important to pick an attenuation A_{div} to be as high as possible. For this design a ratio of 0.5 is chosen to provide good voltage headroom for the EA. With the voltage divider in place, the reference voltage must also be modified to reflect the A_{div} factor as follow:

$$V_{Ref_{EA}} = A_{div} V_{Target}. \tag{5.7}$$

The complete voltage feedback loop is represented in Fig. 5.5. This includes the current loop as it is part of the feedback voltage loop driving the power transistor. Note that the EA provides a positive Gm since the reference voltage is connected to the negative terminal and the feedback connected to the positive terminal. Lets analyze the control loop to confirm the negative feedback operation. First we assume an increases in load current resulting in a lower output voltage reducing the voltage V_{FB}. The positive Gm of the error amplifier results in a reduction in output current from the EA. The reduced current leads to less current at the input of the CFOA reducing the current being driven at the output of the CFOA.

The reduction in output current results in a lower gate voltages for the power transistor increasing the drain current. The increased current increases the voltage at the output. Since the response is in the opposite direction of the stimulus this is a negative feedback loop.

The final piece of the control loop is the power transistor. For the LDO regulator the power transistor is an important piece to design. The power transistor in part determines the minimum V_{DO} and maximum current of LDO designs. The current that a power transistor can supply can be approximated using (5.8) and (5.9) depending on the mode of operation either triode or saturation respectively [31].

$$I_d = \mu_p C_{OX} \frac{W}{L} \left[(V_{sg} - V_{th}) V_{sd} - \frac{1}{2} V_{sd}^2 \right] \tag{5.8}$$

$$I_d = \frac{1}{2} \mu_p C_{OX} \frac{W}{L} (V_{sg} - V_{th})^2 \tag{5.9}$$

Too large of a power transistor results in unnecessary gate capacitance that grows substantially with the width of the transistor. The optimal size is determined by sizing the transistor based on the minimum expected dropout and the maximum load current at the highest temperature representing the worst case scenario. If the power transistor is capable to supply the desired current under this conditions, it will be able to sustain the current under all other conditions as well.

The PSRR performance of the LDO is one of the redeeming features of the A-LDO. The PSRR performance of the A-LDO can be characterized mainly by the loop gain and the BW of the control system. A large gain results in a low PSRR value and large BW results in low PSRR over a wider frequency range. As discussed in the disadvantages of the A-LDO, BW and gain results in larger current consumption negatively impacting the current efficiency. In order to improve the PSRR only a small signal needs to be applied to the gate of the power transistor in order to compensate the supply ripple on the output. Thus adding an extra circuit to cancel only the AC magnitude reduces the current consumption of the control system and greatly improves the PSRR performance. If a control circuit amplifying the AC component of V_{OUT} is connected from the output to the gate of the power transistor

achieving high gain and BW the ripple voltage can be effectively reduced. This feedback system can effectively reduce the output ripple but never eliminate it. This is due to the fact that it can only respond to changes that already affected the output voltage and will follow the feedback system equation (2.6). A feed-forward system on the other hand monitors the ripple on the supply voltage and feeds a compensating voltage at the gate of the power transistor before the ripple occurs. The feed-forward network also does not need high gain to cancel out the output ripple. This results in improved PSRR performance and less stringent requirements on the gain of the feed-forward control system. The main disadvantage of the feed-forward system is the need to calibrate the control. For our design a feed-forward control method is implemented to improve the PSRR performance of the LDO. The feed-forward control system must be implemented within the existing LDO design. Since this design uses a current feedback loop to drive the power transistor, it is beneficial to use a current domain signal to compensate for PSRR to obtain high BW and ease of integration. If the voltage loop would be used instead, the control loop would contain more stages resulting in overall slower response. The implemented feed-forward PSRR filter is shown in Fig. 5.6.

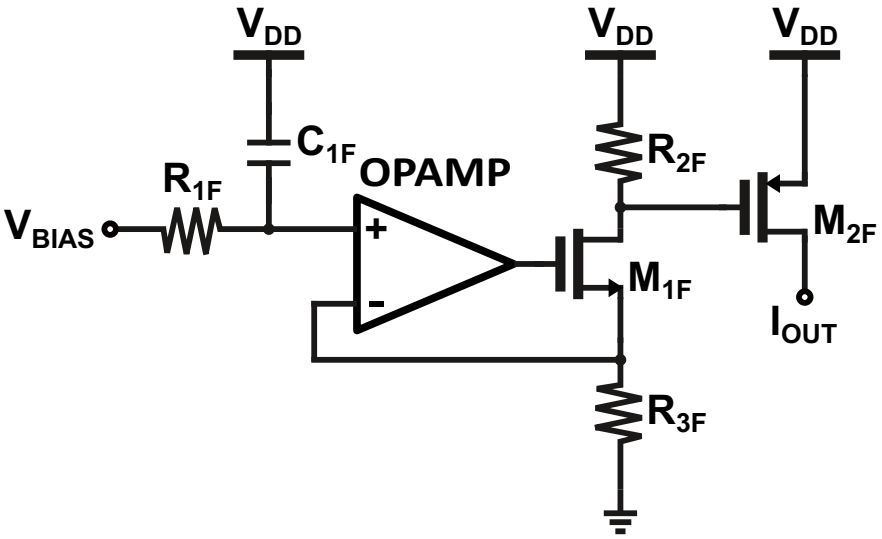


Figure 5.6: Feed-forward line filter circuit diagram.

First the AC information is extracted from the supply line. This is accomplished via the high pass filter created from R_{1F} and C_{1F} blocking the DC component of the supply. The extracted information of the supply ripple is converted to a current via a V/I converter. This is composed of an opamp, a transistor and a resistor. The opamp keeps the voltage drop across R_{3F} constant to the voltage on the non-inverting input by changing the equivalent resistance of M_{1F}. The current is supplied via a resistor R_{2F} where its voltage drop is used to drive the gate of a PMOS transistor M_{2F}. The current provided by M_{2F} is then used to compensate for the PSRR in the current feedback loop. One may consider why M_{1F} could not be replaced by a PMOS and eliminate R_{2F} by connecting the gate of M_{1F} and M_{2F} together? This is to increase the BW of the feed-forward system. If M_{1F} and M_{2F} are connected together, the gate driving requirements are increased without any change in the current consumption. Using the proposed system, the driving requirements of the opamp are minimized due to the small size of M_{1F}. The driving strength of M_{2F} are also improved as it can be driven from R_{2F} which is smaller resistance compared to the output resistance of the opamp. The output current must then be added to the current loop of the A-LDO. There are two possible connection points, at the input of the CFOA or the gate of the power transistor. When connecting to the input of the CFOA the injected current will cause the CFOA to change its output to compensate for the supply ripple. This also means that the response is limited by the BW of the CFOA. The driving capabilities of the CFOA are also leveraged to drive the gate of the power transistor. When connecting to the gate of the power transistor the current immediately drives the gate of the power transistor. The injected current flowing back through R_f to the input of the CFOA is then amplified and translated to the gate of the power transistor. The connection to the gate is used as it increases the speed of the response.

With the system fully in place, let's analyze the direction of the response to ensure removal of ripple at the output of the A-LDO. First, let's assume that an increase in supply voltage occurs. This gets filtered by the high pass filter and a voltage increase is seen at the input of the non-inverting input of the opamp. The increased voltage results in an increase in current through R_{3F}. More current results in a larger voltage drop on R_{2F} reducing the gate voltage of M_{2F}. The reduced gate voltage causes more current to flow at the drain

terminal of the PMOS. The increased current at the gate increases the gate voltage and also increases the input current of the CFOA further increasing the output current and thus the gate voltage. The increased gate voltage results in lower current and thus lower voltage at the output. Since the stimulus was going to increase the output voltage and response reduced it, then the feedforward filter can reduce the ripple in the output of the A-LDO regulator. In order to cancel out the ripple, the correct gain of the feed-forward filter must be realized. The small signal transconductance of the system is represented as follow:

$$Gm = \frac{g_{m1F} g_{m2F} K R_{3F} - g_{m2F}}{g_{m1F} K R_3 F + 1}. \tag{5.10}$$

Based on the equation the gain can be modified by changing the size of M_{2F}. The size of gm_{1F} and R_{3F} are not used to tune the system as we want to minimize their size in order to have low current consumption and high BW. The DC biasing point of the line filter can be modified by the bias voltage of the high pass filter. The DC current flowing in R_{3F} can then be represented as follow:

$$I_{R3} = \frac{V_{Bias}}{R_3}. \tag{5.11}$$

The cutoff frequency of the high pass filter is optimized in order to reduce the silicon area requirements. The A-LDO regulator capable of compensating for low frequency ripples. Thus the cutoff frequency of the high pass filter is chosen to be slightly smaller than the flat band PSRR of the regulator operating without the feed-forward line filter reducing the size of R_{1F} and C_{1F}. The cut-off frequency of a 1^{st} order high pass RC filter can be approximated as follow:

$$f_c = \frac{1}{2\pi RC}. \tag{5.12}$$

5.3 Stability Analysis

Stability of an A-LDO is an important criteria to ensure stable operation over the entire range of load current and capacitance. The stability of the LDO can be analyzed using the open loop transfer function and analyzing poles and zeros [31]. Using the poles and zeros, the bode plots representing the open loop gain and phase can be used to analyses

the performance of the system and the stability. The Barkhausen stability criterion states that the phase (ϕ) of a unity gain feedback must remain within *pi* of the DC phase for all frequencies that have gain larger than or equal to 1. The 2 conditions required for stability of a feedback system such as the one in Fig. 2.3 are shown in (5.13).

$$\begin{aligned} \|\beta A\| &< 1 \\ \phi &< \pi \end{aligned} \tag{5.13}$$

The phase margin (PM) can be determined by obtaining the phase where the open loop gain of the feedback system is at the unity gain frequency. The unity gain frequency can be used to determine the stability of the system. A larger PM results in better stability. PVT variations may change the stability of the design thus the PM must be designed to account for these effects. A minimum PM of 75 ° is considered adequate for this project.

The proposed design contains 2 feedback loops that require analysis. For the LDO to remain stable both loops must exhibit stable operation. Using the dual loop architecture classifies the A-LDO as a multi loop system complicating the stability analysis of each loops as one loop also interferes with the other. In order to simplify the analysis of both loops the the quasi-stable criteria is employed. This criterion states that if two feedback loops are inter connected and one loop responds much faster than the other, then both loops can be separated as the slower loop will always respond only when the other loop is stabilized. A a general rule of thumb, the BW of the faster loop should be around 10 times faster than that of the slower loop. [50] If this is applied to the dual loop A-LDO we can expect that the voltage loop will exhibit slower response compared to the current loop. In order to confirm that this criteria can be used, both loops are derived separately and the BW of each loop can be compared in order to confirm the conditions of the criterion.

First, the current loop is analyzed to derive the transfer function. In order to perform our analysis we can assume that the voltage loop is invariant. The small signal model is shown in Fig. 5.7 is derived from the simplified circuit in Fig. 5.4. Where R_z is the output impedance of the CFOA and R_L includes the load resistance and the feedback resistors in

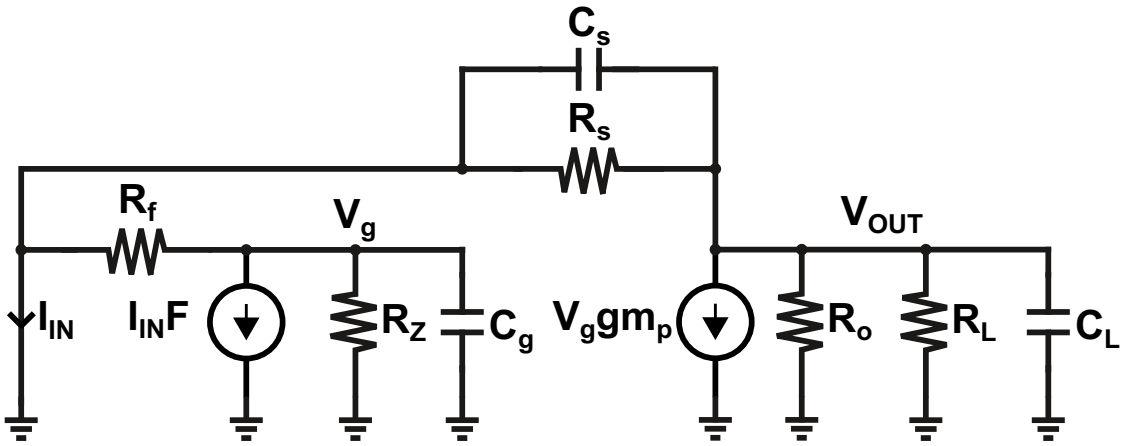


Figure 5.7: Small signal model of the current feedback loop.

parallel defined with using:

$$R_L = \frac{R'_L(R_{F1} + R_{F2})}{R'_L + R_{F1} + R_{F2}}, \tag{5.14}$$

where R'_L is the load resistance, F represents the current gain of the CFOA and R_L is the combined load resistance. It can be noted that at high loads $R_L \approx R'_L$. The input resistance of the CFOA is neglected in this analysis since $R_{IN} << R_S << R_F$. To increase the stability and performance of the current loop, the C_s capacitor is added in parallel to R_s. The current through the capacitor can be defined as:

$$I_{Cs} = C_s \frac{dV_{OUT}}{dt}. \tag{5.15}$$

With the current feedback loop C_s the extra capacitor adds a derivative function to the feedback where the slope of the output gets amplified. During a sharp load change, the current feedback is further amplified by the slope of the output voltage. A derivative loop will add an extra zero in the transfer function. The loop is separated at the gate of the power transistor in order to obtain the open loop transfer function. Using KCL and KVL, the transfer function of the current loop is defined by:

$$TF_{CL} = \frac{FR_z(C_s gm_p R_L R_f R_s s - C_s R_L R_s s - C_L R_L R_s s - R_s + gm_p R_L R_f - R_L)}{-Rf(C_s R_L R_s s + C_L R_L R_s s + R_s + R_L)(C_g R_z s + 1)}. \tag{5.16}$$

For simplicity the transfer function has already been factorized. The obtained transfer function contains 2 poles and 1 zero represented as follow:

$$P_{1,CL} = -\frac{1}{C_g R_z}, \tag{5.17}$$

$$P_{2,CL} = -\frac{R_s + R_L}{(C_s + C_L) R_L R_s}, \tag{5.18}$$

$$Z_{1,CL} = \frac{R_s - gm_p R_L R_f + R_L}{(C_s gm_p R_f - C_s - C_L) R_L R_s}. \tag{5.19}$$

The dominant pole of the system is located on the gate of the power transistor and is represent by (5.17). The non-dominant pole is located on the output of the A-LDO and is represented by (5.18). The non-dominant pole is modified by the load resistance and load capacitance where larger R_L pushes the pole to a higher frequency and C_L pushes the pole to a lower frequency. This means that there can be a situation where the dominant pole and non-dominant pole cross at light loads and high capacitance levels. For this design the minimum load set by $R_{F1} + R_{F2}$ ensures that this does not occur and the LDO remains stable when no external load is applied. Since this is a cap-less design, the minimum C_L is set by the parasitic capacitance of the layout and the maximum C_L that the design can handle is defined by the stability based on the location of this pole. The current loop contains one zero located on the gate of the power transistor. The zero moves with R_L and C_L where larger R_L and C_L increases the frequency of the zero. For this loop to be stable, the zero must be located on the LHP. The zero can be unstable based on the positive feedback from R_f that requires further analysis. For the numerator to be negative requires that $gm_p R_L R_f > R_L + R_s$. For the denominator to be negative we obtain the condition of $gm_p C_s R_f < C_s + C_L$. The conditions in order to obtain a LHP zero is represented as:

$$\frac{C_s + C_L}{gm_p C_s} < R_f < \frac{R_L + R_s}{gm_p R_L}. \tag{5.20}$$

For the case where low load capacitance is present the stability condition can be simplified to:

$$\frac{1}{gm_p} < R_f < \frac{R_L + R_s}{gm_p R_L}. \tag{5.21}$$

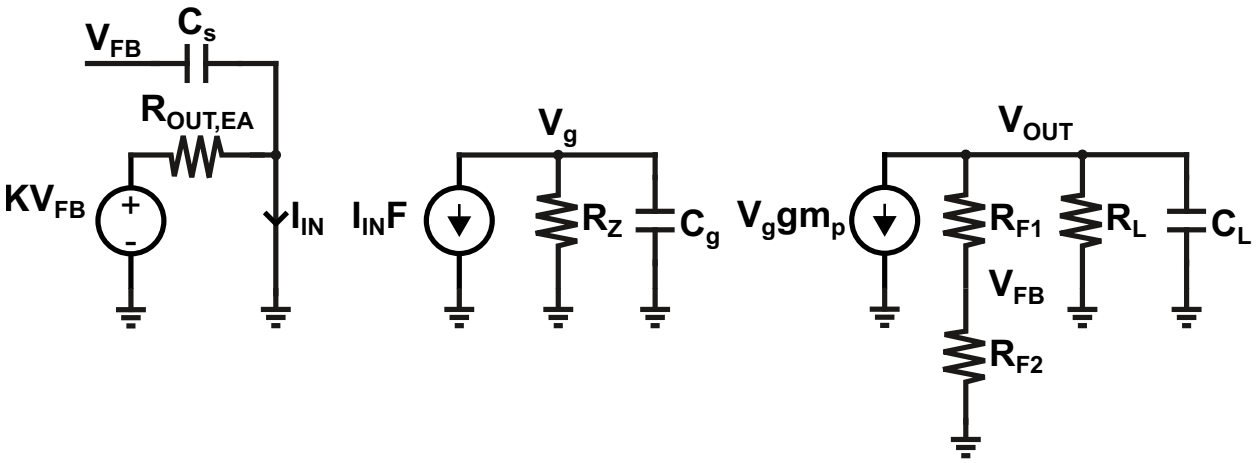


Figure 5.8: Small signal model of the voltage feedback loop.

Using the stability conditions the minimum and maximum size of R_f can be determined in order to remain stable. Furthermore, the location of the zero should be between the dominant and non-dominant poles in order to increase the phase margin.

The analysis of the voltage feedback loop is performed in a similar manner. Again, using the quasi-stable criteria the current loop is considered invariant and the small signal model shown in Fig. 5.8 is derived based on Fig. 5.5. The CFOA is still present as current amplification will still occur. F is then equivalent to the overall current amplification that the current loop provides including R_f and R_s. The EA uses a miller capacitor in order to inject a zero in the feedback of the EA improving the PM of the voltage feedback loop. The derived transfer function of the voltage feedback loop is represented as follow:

$$TF_{VL} = \frac{-Fgm_pR_{F2}R_LR_z(C_mR_{OUT,EA}s + K)}{-R_{OUT,EA}((R_{F1} + R_{F2})C_LR_Ls + R_L + R_{F1} + R_{F2})(C_gR_zs + 1)}. \tag{5.22}$$

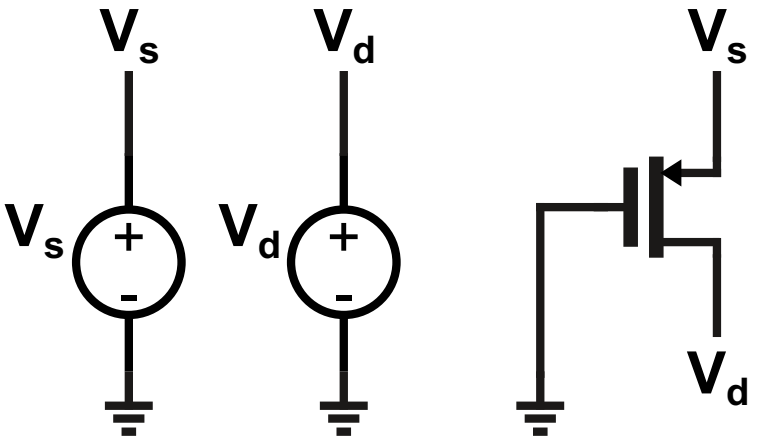


Figure 5.9: Power transistor simulator test bench.

The transfer function contains two poles and one zero. The poles and zeros can be represented using:

$$P_{1,VL} = -\frac{1}{C_g R_z}, \tag{5.23}$$

$$P_{2,VL} = -\frac{R_L + R_{F1} + R_{F2}}{(R_{F1} + R_{F2}) C_L R_L}, \tag{5.24}$$

$$Z_{1,VL} = -\frac{K}{C_m R_{OUT,EA}}. \tag{5.25}$$

As expected from the derivation from the general A-LDO, the two poles of this system are located at similar locations. The main pole is located on the gate of the power transistor. The non-dominant pole is located at the output of the LDO. The zero is located at the output of the EA generated by the miller compensation capacitor.

With the stability of the current feedback and the voltage feedback loops derived, the simulation results and optimization can be performed. The simulation are performed using the Cadence Virtuoso software and the ADS Spectre simulator. The A-LDO is designed using the TSMC 180 nm standard CMOS PDK. The simulation is used to design and optimize the values of the A-LDO. The first component to be designed is the power transistor. To reduce the size and gate capacitance the minimum process length of 180 nm is used. A test bench setup is used shown in Fig. 5.9 in order to determine the optimum size of the power transistor. In order to test the power transistor current capability, the source voltage is set

to 1.4 and the drain voltage to 1.2 resulting in a V_{DO} of 200 mV. The simulation temperature is set to $80C^{\circ}$. In order to test for maximum current, the gate voltage is connected to GND. The simulation results are shown in Fig. 5.10. For the desired 500 mA current, the minimum

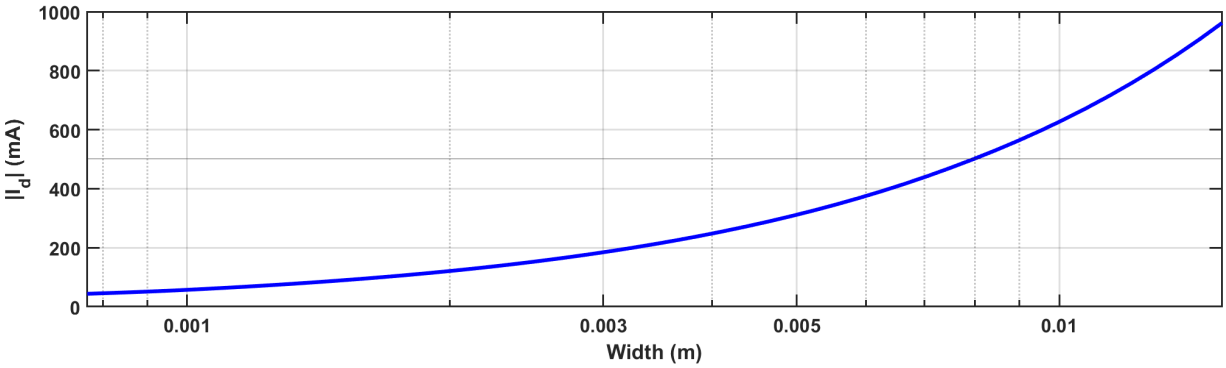
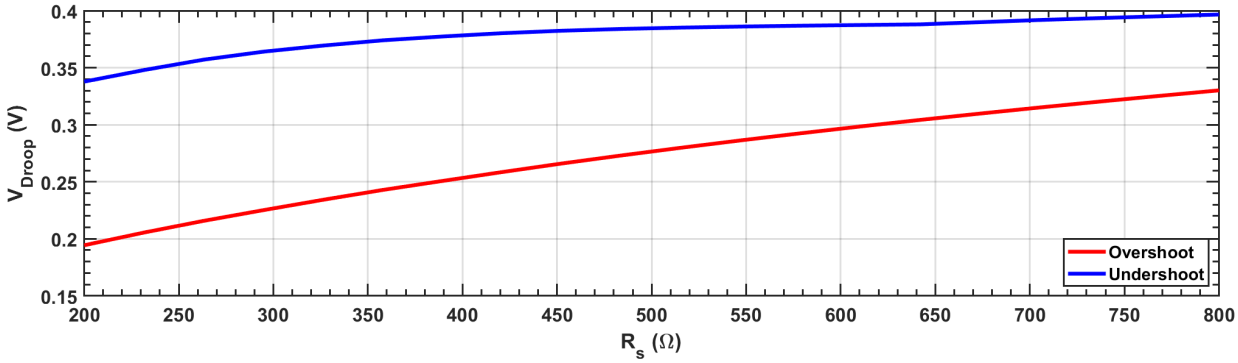


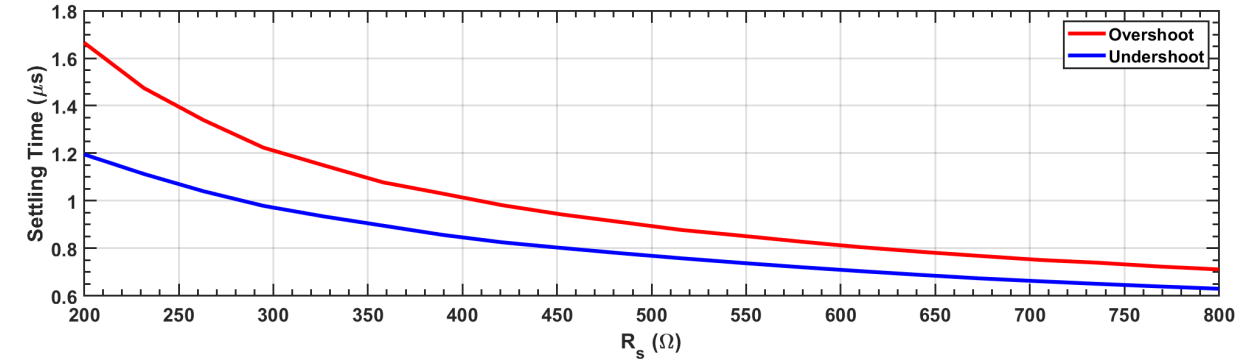
Figure 5.10: Power transistor simulated width vs current at V_dd = 1.4 V TT, $80C^{\circ}$ and V_{DO} = 200 mV.

size of the power transistor is 8 mm. When accounting for PVT variation and extra trace resistance included from the layout, the final size of the power transistor chosen is 9.6 mm. The resulting gate capacitance is 16.57 pF.

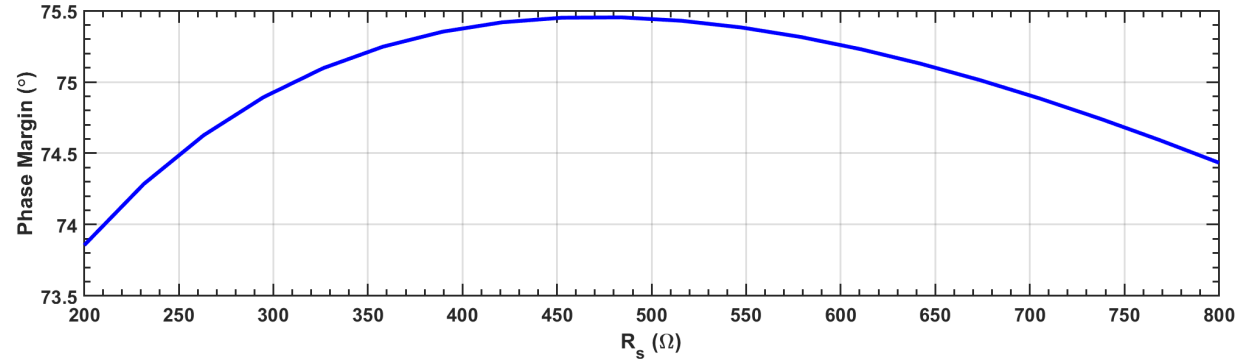
The CFOA components are designed next, we first look at the current gain F. Larger current gain will result in higher accuracy with the drawback of larger current consumption. Since the accuracy will be used by the voltage loop, a low F value can be used saving on current consumption. For our design, L and K in (5.1) is set to 2 resulting in a current gain of 4. With the CFOA mostly designed, the current loop can be completed. For the current feedback loop a small value of R_s is chosen and a larger value of R_f is used in order to enable larger output capacitance. Using (5.17) - (5.19) the stability of the current loop is simulated analyzing the PM, settling time and droop to determine the optimum values of R_s. Fig. 5.11 shows the simulation results with changes in R_s. Based on the simulations, the droop voltage increases with the size of R_s while the settling time is increased. The phase margin of the current loop is optimized when $R_s = 475\ \Omega$ Though this results in the best PM, V_{Droop} suffers. In order to meet the 75° PM requirement R_s can be chosen between 315 and 675



(a)



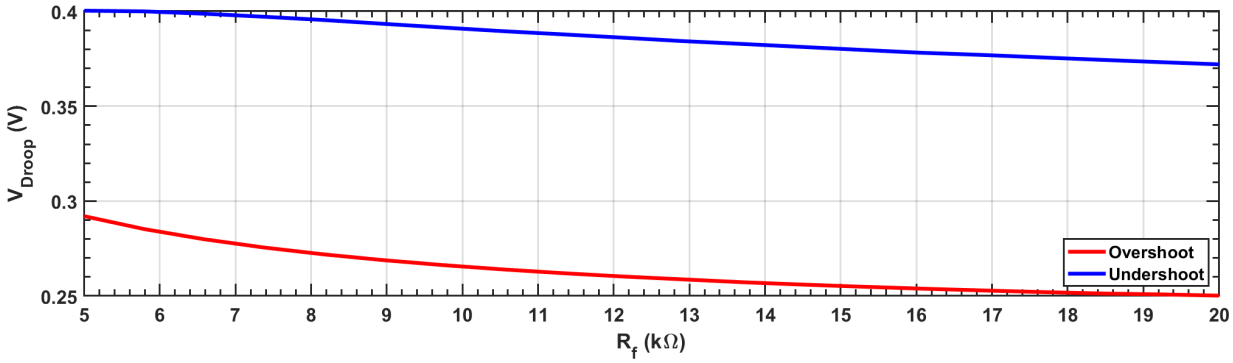
(b)



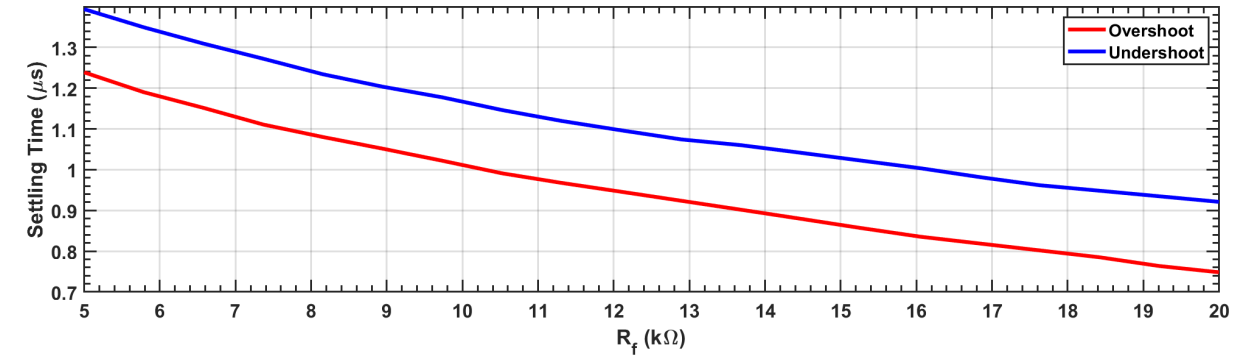
(c)

Figure 5.11: Current loop simulation results with varying R_s, a) Maximum and Minimum V_{Droop}, b) Settling time within 10 mV of final value, c) Phase margin of current loop, at V_{dd} = 1.8 V, V_{DO} = 600 mV, TT, 27 C°.

Ω. As a good compromise between droop voltage and settling time, an R_s value of 400 Ω is used for the design resulting in near peak PM, good settling time and reduced droop voltage. Using the same R_s the R_f is varied in order to determine the optimum value. The same tests are performed for the R_f values. The simulation results are shown in Fig. 5.12. The



(a)



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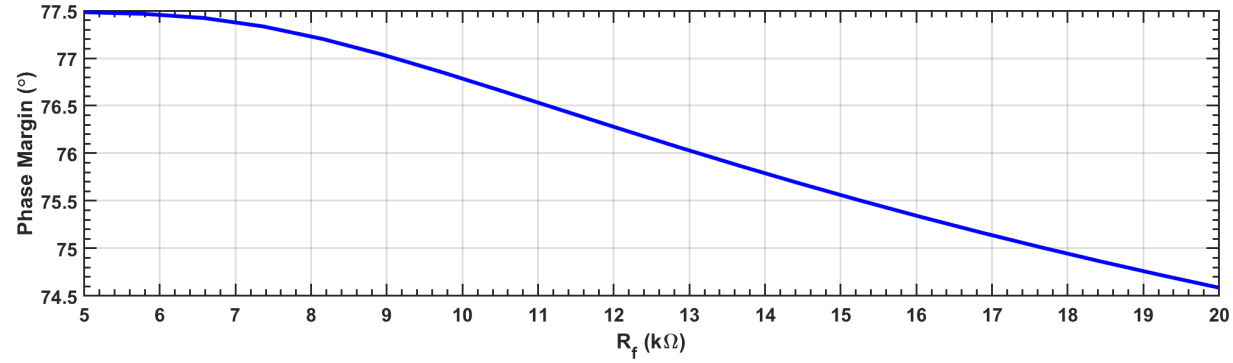
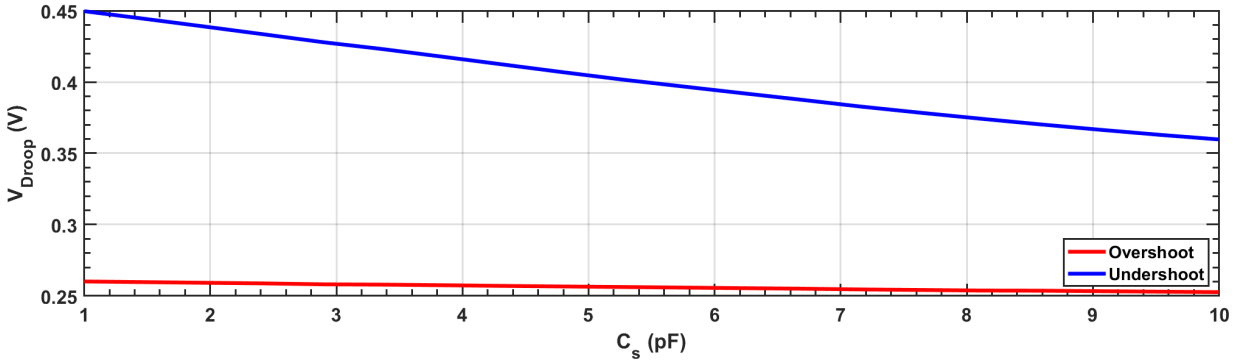


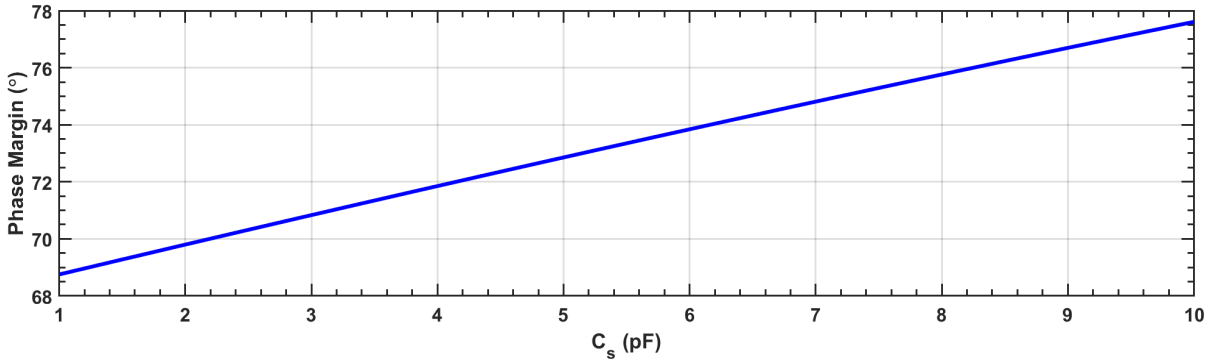
(c)

Figure 5.12: Current loop simulation results with varying R_f, a) Maximum and Minimum V_{Droop}, b) Settling time within 10 mV of final value, c) Phase margin of current loop, at V_{dd} = 1.8 V, V_{DO} = 600 mV, TT, 27 C°.

R_f resistor is used as a feedback in order to increase the gain of the CFOA thus we expect that larger resistance level to increase the speed of the current loop. The simulation shown in Fig. 5.12 shows that increase in R_f reduces the settling time as well as the droop voltage at the cost of lower PM leading to a trade off between speed and stability. We want to



(a)



(b)

Figure 5.13: Current loop simulation results with varying C_s, a) Maximum and Minimum V_{Droop}, b) Phase margin of current loop, at $V_{dd} = 1.8$ V, $V_{DO} = 600$ mV, TT, 27 C°.

maximize the performance of the LDO while maintaining good stability, an R_f value of 15.8 kΩ is used in order to meet these requirements. It can be noted that increasing the value of R_f results in larger loop gain of the current loop resulting in the increased performance observed. The same simulations are completed by changing C_s, the results are shown Fig. 5.13. Changing C_s does not have significant effects on the settling time while reduces the maximum droop and increase the PM. The value of C_s is chosen as 7.6 pF achieving good stability, size and performance. This completes the entire current loop component values. Note that this shows the general considerations for obtaining the component values and the optimization procedure used. In order to obtain the best results, the first value of R_s must be reworked as the other devices may change the performance characteristics. Thus these steps are performed many times to obtain an optimum solution. The results shown are the last iterations of the design process.

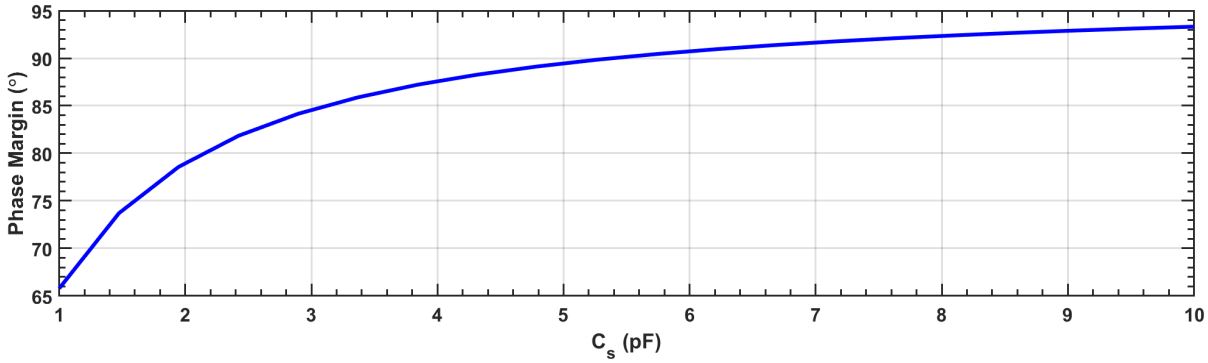


Figure 5.14: Voltage loop simulation results with varying C_m, Phase margin, at $V_{dd} = 1.8$ V, $V_{DO} = 600$ mV, TT, 27 C°.

A similar design approach is performed on the voltage loop. First, the feedback resistor values are designed. An attenuation ratio of 0.5 was chosen, the sum of the resistance determine the minimum load current. The minimum load current set by the resistor ladder drastically effects the quiescent current. In order to maximize the current efficiency, a value of $R_{F1} = R_{F2} = 5k\Omega$ is chosen. This results in a minimum load current of 120 μA. C_m is designed and is used to increase the PM of the voltage loop. The simulation of the PM of the voltage loop is shown in Fig. 5.14. A value of 7.6 pF is used for C_m enabling a high PM increasing the stability of the loop with high load currents and capacitance.

With all the components determined, the bode plots of the voltage and current loops can be plotted. The bode plot of the current loop is shown in Fig. 5.15. As expected from the derived transfer function, the PM is lowest when the load is low and the capacitance is high. This is due to the non-dominant pole moving to a lower frequency and the zero moving to a higher frequency. This results in a lower phase value at a lower frequency reducing the PM. The minimum PM simulated is 73.73 ° @ 10.74 MHz. The main pole of the system remains relatively constant over the entire range of simulated load as was predicted from (5.17). At light loads, the open loop gain is lowest at 9.54 dB. As the load is increased more current flows in the input of CFOA resulting in larger gain. The bode plot of the voltage loop is shown in Fig. 5.16.

As predicted from the transfer function, only the non-dominant pole of the voltage loop changes with the load. The results in a very stable loop. The minimum PM achieved

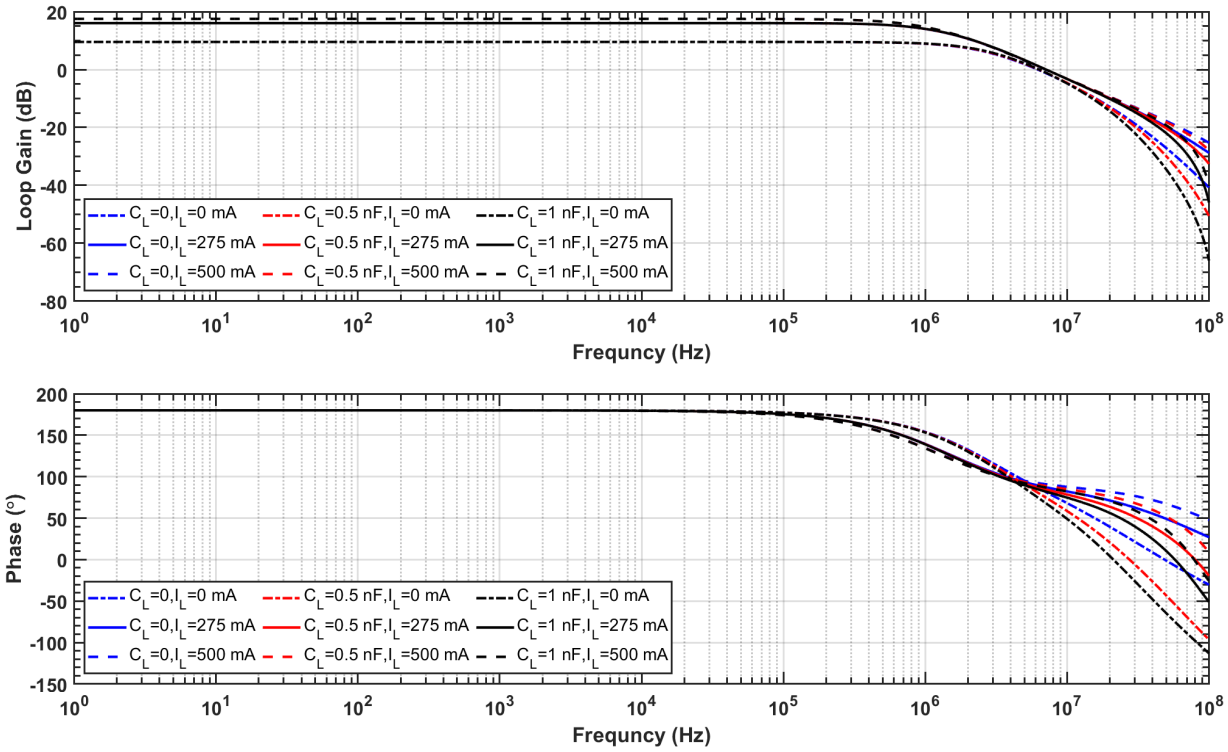


Figure 5.15: Current loop Bode Plot at $V_{dd} = 1.8$ V, $V_{DO} = 600$ mV, TT, $27C°$.

is 91 ° at a frequency of 337.54 kHz. The open loop gain of the voltage loop has a flat band gain of 48.4 dB giving the A-LDO a good line and load regulation as using (2.6). The zero being injected from the miller compensation can be clearly seen maintaining the the phase of the feedback over a wide range increasing the PM significantly.

With the A-LDO fully configured, the feed-forward line filter is optimized for the components values used in the current loop. First the PSRR performance of the LDO is simulated without the line filter in order to analyze the performance shown in Fig. 5.17. The simulation results show good low frequency performance of -56.49 dB up to 500 Hz where the attenuation starts to increase until 1 MHz. There is no improvement of PSRR due to the controller above 1 MHz, any attenuation is a result of parasitic capacitance in the power transistor and load. The high pass filter for the feed-forward line filter can be designed in order to obtain the ripple voltage from the supply. A value of $C_1 = 6\ pF$ and $R_1 = 10M\ \Omega$ are used. Using (5.12) the cut-off frequency of the high pass filter can be calculated as 2.6 kHz allowing for PSRR improvements above the flat band of the A-LDO.

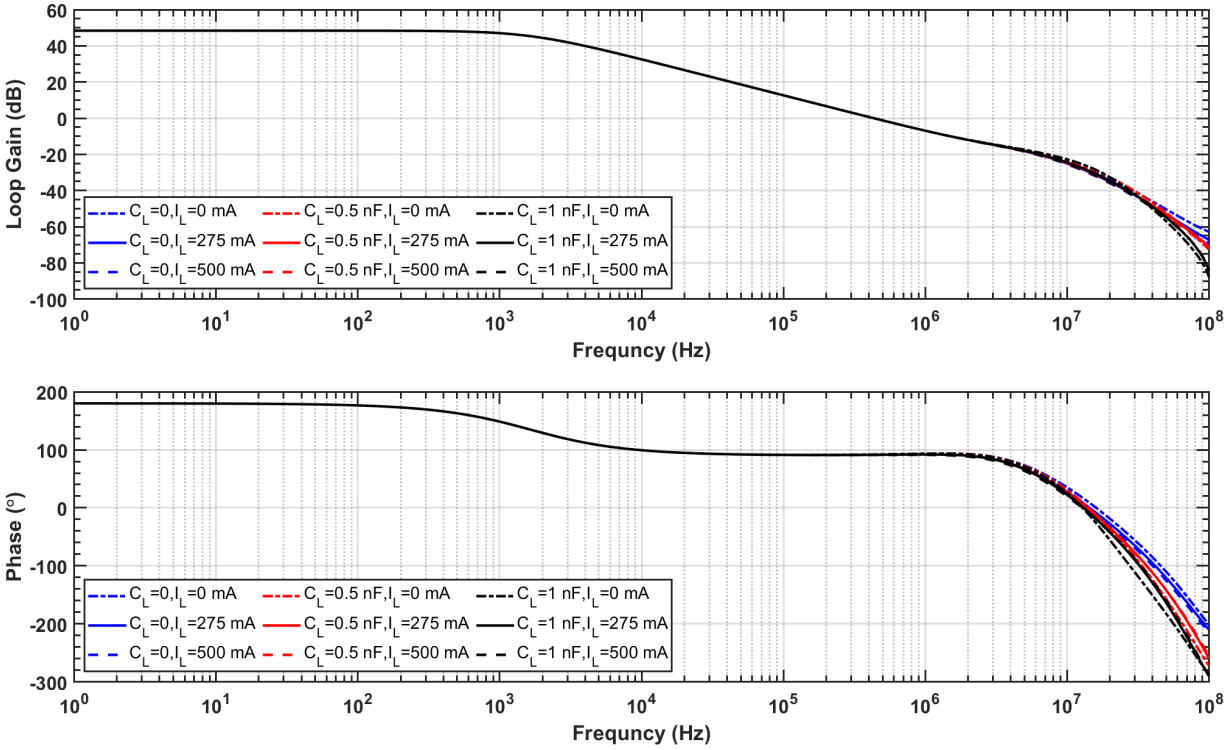


Figure 5.16: Voltage loop Bode Plot at $V_{dd} = 1.8$ V, $V_{DO} = 600$ mV, TT, $27C°$.

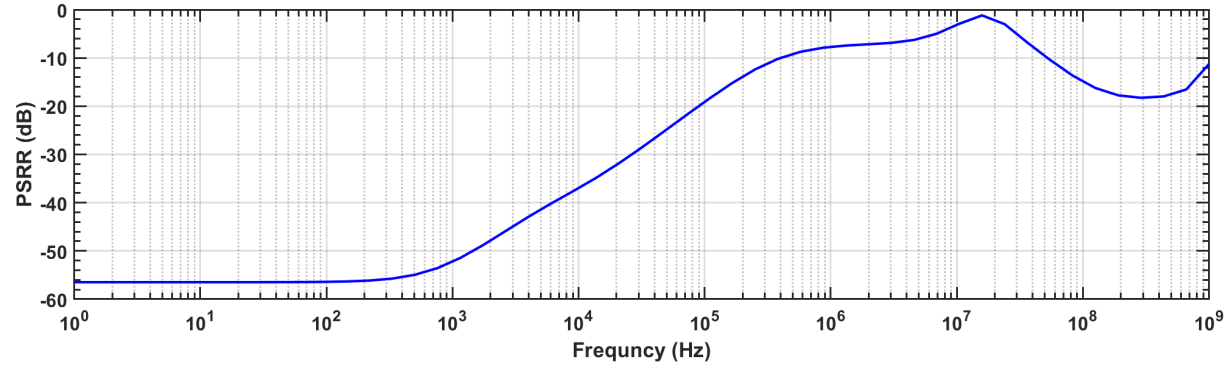


Figure 5.17: Simulated PSRR performance without feed-froward line filter at $V_{dd} = 1.8$ V, $V_{DO} = 600$ mV, TT, $27C°$.

As mentioned previously, the gain of the feed-forward line filter must be optimized in order to reduce the PSRR. Based on (5.10) the current gain can be adjusted by varying the size of transistor M_{2F}. In order to optimize the PSRR an AC simulation is conducted varying the size of M_{2F} in order to determine the optimum width. With the feed forward line

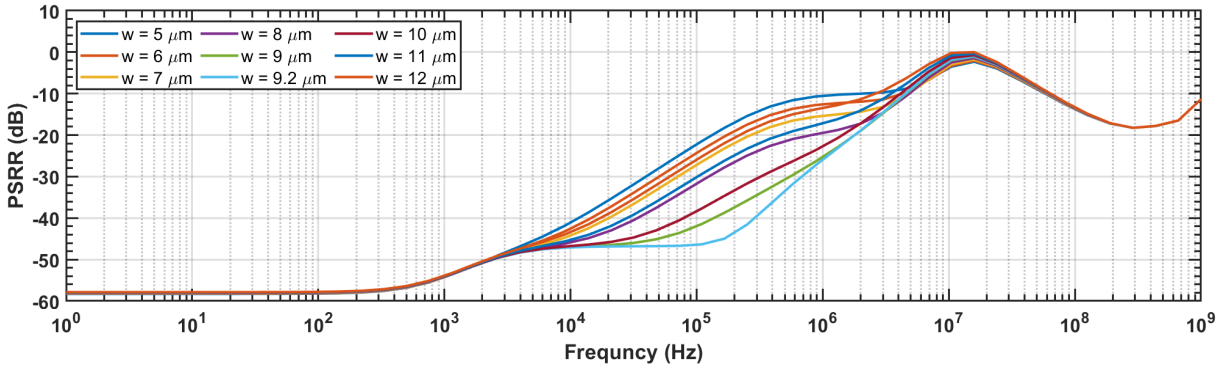


Figure 5.18: Simulated PSRR performance with feed-froward line filter with varying M_{2F} width at V_{dd} = 1.8 V, V_{DO} = 600 mV, TT, 27$C°$.

filter activated, the PSRR is greatly improved in the range from 2.6 kHz up to 7 MHz. At frequencies larger than 7 MHz the PSRR is similar to that of the original design without the line filter. The reduction in performance is due to the BW limitations of opamp in the line filter implementation. The width of M_{2F} drastically affects the PSRR performance where a width of 9.2 μm results in the best performance. The addition of the feed forward line filter is capable of maintaining a -46.3 dB PSRR up to 100 kHz where is then rises at 20 dB per decade. Since the high pass filter rejects low frequencies, the PSRR below 2.6 kHz remains the same. Fig. 5.19 show the transient simulation of the LDO at varying load current and capacitance.

Transient simulation in Fig. 5.19 are performed for typical corners using a load edge time (t_r) of 100 ns. The transient simulations are performed at light loads Fig. 5.19 (a)(b) as well as at high load Fig. 5.19 (c)(d) to determine the change in performance with different load conditions. From the results we can determine that the overshoot and undershoot increase with the size of the load capacitor. This is due to extra time required to charge the load capacitance after a droop has occurred. The maximum overshoot and undershoot are 500.8 mV and 299.6 mV respectively and occur when the LDO is subject to a high load current and capacitance.

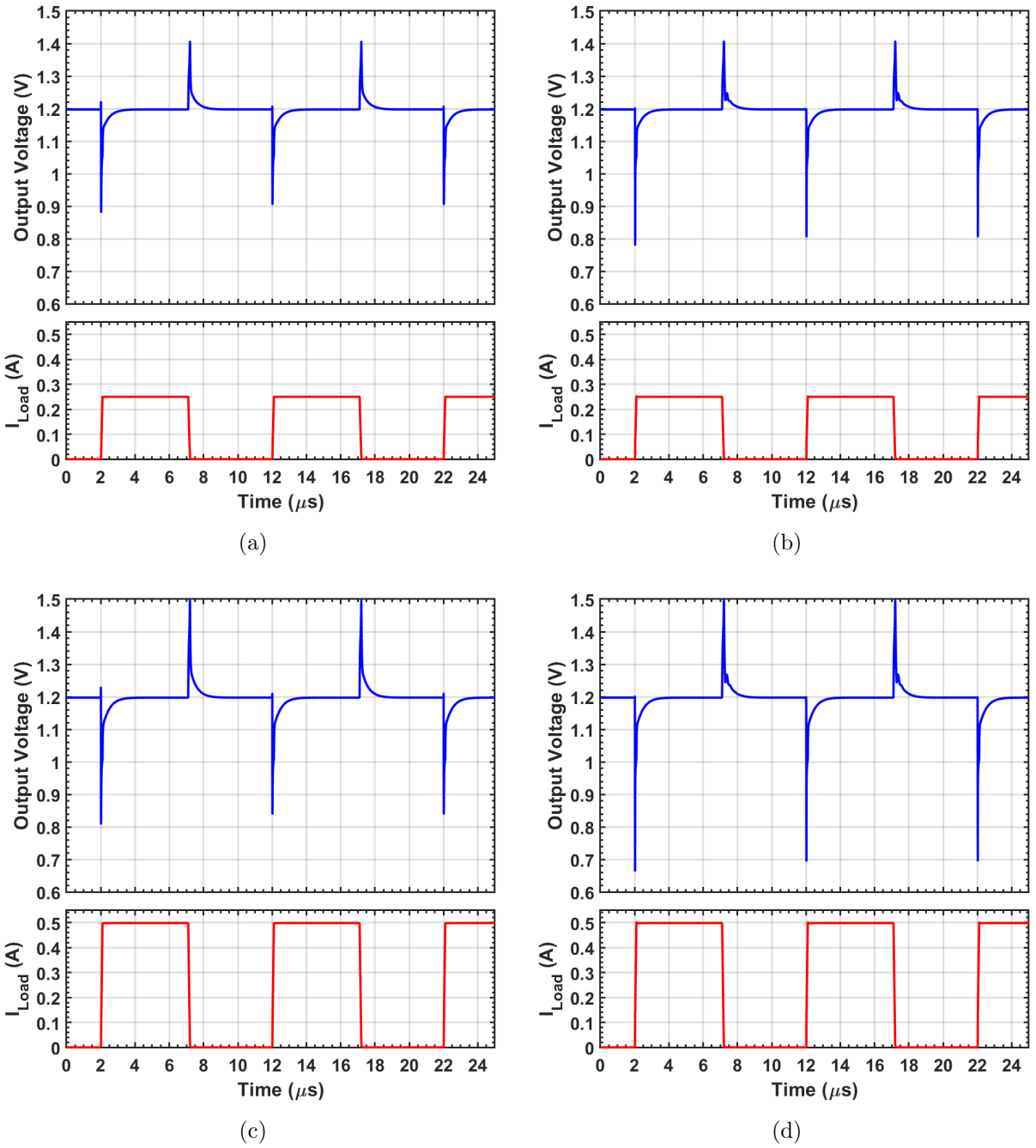


Figure 5.19: Transient simulation at a) I_L = 0 - 250 mA, C_L = 0 pF b) I_L = 0 - 250 mA, C_L = 500 pF c) I_L = 0 - 500 mA, C_L = 0 pF d) I_L = 0 - 500 mA, C_L = 500 pF. Test conditions of V_dd = 1.8 V, V_{DO} = 600 mV, t_r = 100 ns, TT, 27 C°

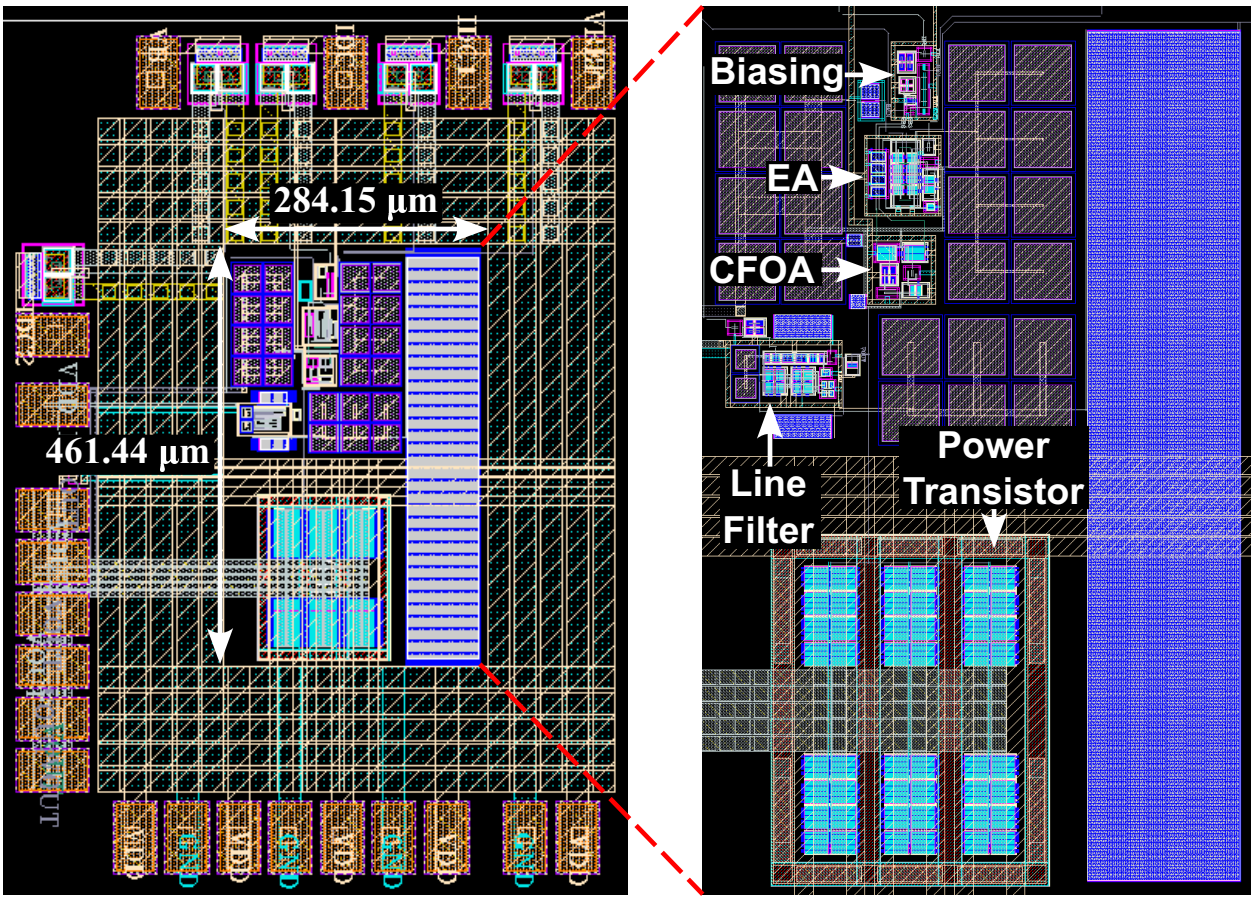


Figure 5.20: A-LDO layout.

5.4 Layout

The dual loop A-LDO design is to be manufactured using the TSMC 180 nm standard technology. This is a 1 poly 6 metal 1.8 V with MiM caps process. Fig. 5.20 shows the complete layout of the design including locations of the different components. The layout of the A-LDO consumes 0.0131 mm^2 of active area excluding the pads and power distribution.

The layout of the LDO regulator is crucial in order to obtain a functional LDO with the desired performance level investigated in the previous section. Many layout techniques must be applied to minimize the effects of parasitic. First lets look at the matching of transistors. Many components of the A-LDO contains current mirrors and differential transistor pairs that require the transistors to exhibit the same performance characteristics. Any mismatch between the transistors and resistors results in a loss in functionality or performance.

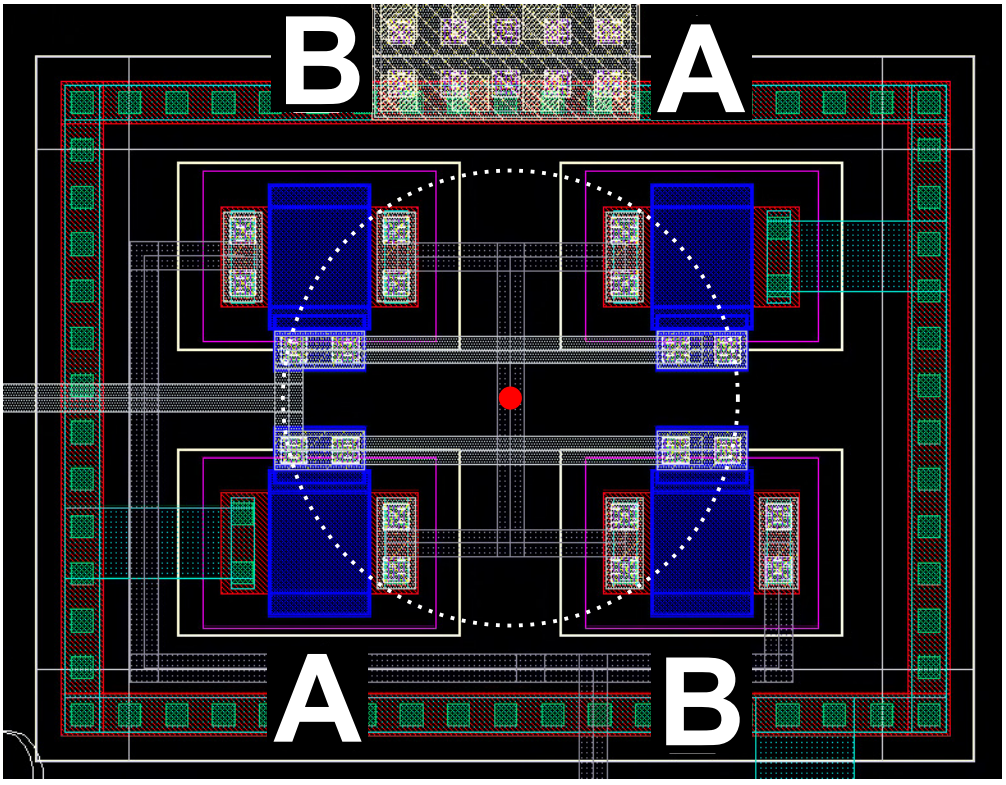


Figure 5.21: Example of the common centroid layout of 2 transistors.

When transistors are manufactured the dopant concentration may not be even uniformed over the entire area of the silicon. This results in differing gm performance of transistors next to each other. To minimize the effects, transistor are divided and connected in parallel such that the total length equals that of the design. Layout topologies such as the common centroid and interdigitation are used to reduce the effects of silicon variance. The common centroid method is the most used in this design where transistors are layout in a grid shape and the transistors are arranged such that they all share the same mid point. This means that the transistors share more common area of the silicon reducing the mismatch. Interdigitation alternates between each devices in order to increase the shared area. Fig. 5.21 shows an exaple of the common centroid method used in the A-LDO layout where the red dot represents the middle point shared by both transistor A and B. The common centroid and interdigitation techniques can be applied to match more than 2 transistors.

The A-LDO design is high current design, the current density of the traces and vias must be carefully examined for the power transistor. The current density capability of each metal layer is represented in Table 5.1. The maximum current density of the metal

Table 5.1: Maximum current density of metals in TSMC 180 nm at 110 °C

	J_{max} (mA/μm)		J_{max} (mA/via)
M1	1	Contact	0.53
M2	1	Via12	0.28
M3	1	Via23	0.28
M4	1	Via34	0.28
M5	1	Via45	0.28
M6	1.6	Via56	0.706

is dependent on the temperature where Table 5.2 shows the conversion factor at different temperatures. The rating factor can be used to calculate the maximum current density at a

Table 5.2: Current density conversion factor at different temperatures

Temperature (°C)	70	85	100	110	125	150	175
Rating factor (R_f)	3.44	2.1	1.33	1	0.671	0.367	0.215

given temperature using:

$$J_{max,New} = J_{max} R_f. \tag{5.26}$$

Where J_{max} comes from Table 5.1 and R_f comes from Table 5.2. For the design of the power transistor, we expect that the cooling will be sufficient to maintain the power transistor below 70 °C thus a rating factor of 3.44 is used. To save silicon area, the power transistor is divided into 6 banks. This facilitates the various connections across the power transistor. Each banks are sub divided in 8 sections containing 16 transistors of 12.5 μm width. In total the power transistor layout contains 768 individual transistors, when all connected in parallel result in a total width of 9.6 mm. Fig. 5.22 shows the layout of each section of the power trasistor. All the current from each of the banks are directed to the center of the power

transistor where it is collected in 5 parallel traces each 8 μm width. The traces are separated in order to reduce the EM effects during fabrication and helps for thermal expansion. In order to meet the current requirements, each trace is composed of 4 metal layers stacked on top of one another. The maximum current carrying capability can be calculated as follow:

$$\begin{aligned} I_{max} &= N_{traces} \sum j_{max} W R_f \\ I_{max} &= 5 \sum_{M_2}^{M_5} 1 \times 8 \times 3.44 \\ I_{max} &= 550.4mA \end{aligned} \tag{5.27}$$

Where N_{traces} is the number of traces connected in parallel, W is the width of each metal segment. The current capability is higher than the desired 500 mA. Each of the traces are connected together using via farms of 15 x 15 resulting in a maximum current capability of 216.72 mA per trace. Each transistor bank consume 62.5 mA. The source of each bank is connected to the supply voltage using two M6 trace with a width of 10 μm resulting in a current capability of 110.08 mA for each banks. The output, V_{OUT} is connected using two parallel traces composed of 2 metal layers of 8 μm each resulting in a current capability of 110.08 mA. Thus both traces can handle the current requirements of each banks. Each individual transistors within the sections carry a current of 0.488 mA each. The current is distributed across the width of each transistors using 3 metal layers with a width of 0.38 μm each resulting in a current capability of 3.92 mA. Each side of the transistor is connected using 15 vias capable of handling 4.2 mA. This completes all the traces used to connect the power transistor, all achieve a maximum current capability larger than the maximum load current.

Another key factor is the line resistance of the metal traces. The power traces introduce parasitic resistance that have not been simulated in the schematic simulation. The resistance is introduced in the traces from the supply pads to the source of the transistor and from the drain of the transistor to the output pads. This line resistance is also the reason that a larger power transistor is chosen in order to achieve the desired current at low V_{DO}. When current flows in the traces an extra voltage drop occurs, negatively effecting the

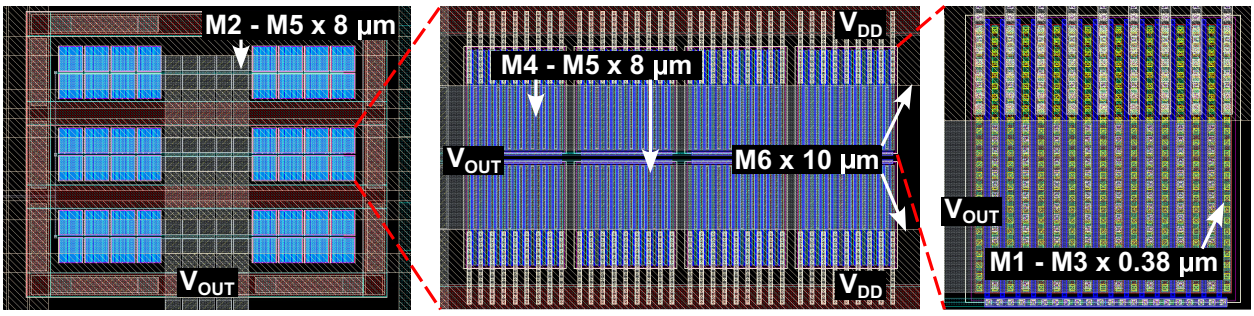


Figure 5.22: Power transistor layout.

load regulation. Two layout methods can be used to minimize the effects of line resistance. First, the resistance can be reduced by increasing the width or number of traces carrying the current. This comes at the cost of extra silicon area utilization. The second method is to include as much trace resistance within the feedback loop as possible. The feedback is connected at the drain of the power transistor, thus the supply line resistance are always within the feedback loop. The output traces can be connected anywhere from the drain of the power transistor to the output pads. Let's consider the scenario where we connect the feedback path to the drain of the power transistor. When the LDO operates at no load the output voltage at the drain is set to V_{Ref} by the feedback loop and since no current is flowing at the load, there is no voltage drop on the trace resistance. When full load is applied to the A-LDO, the feedback loop maintains the voltage at the drain of the power transistors to V_{Ref}. The current flowing in the traces introduce an extra voltage drop to the output resulting in a reduced output voltage. Depending on the line resistance and the load current, the voltage drop can be significant. The output voltage can be expressed as:

$$V_{OUT} = V_{Ref} - I_{Load}R_{Trace}. \tag{5.28}$$

If the feedback voltage is connected to the output pads, the no load condition remains the same where the pads are kept at 1.2 V and no voltage drop occurs. When full load is applied, the feedback loop maintains the pad voltage at V_{Ref}. Trace resistance is proportional to the length of the trace, thus the trace resistance to the output pads is reduced and a lower voltage drop is achieved. This means that the feedback loop takes into account the trace

resistance and thus maintains the drain of the power transistor at a higher voltage in order to compensate for the voltage drop. This greatly improved the load regulation performance while not costing any extra silicon area. Fig. 5.23 shows the connection methods for the feedback loop including the trace resistance.

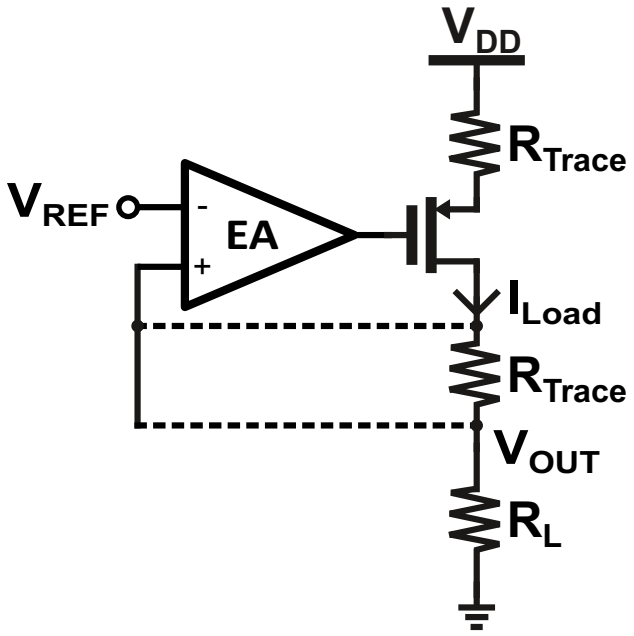


Figure 5.23: Feedback loop including trace resistance.

Manufactured IC are extremely sensitive to electrostatic discharge (ESD) resulting in prevention methods being implemented to reduce the likelihood of accidental ESD damaging the designed circuit. This is achieved using the simplest method where inputs signals are clamped between to V_{DD} and GND using silicon diodes. This endures a low impedance path is available if ESD were to occur on an input pin.

With te layout complete, a post layout simulation can be conducted to ensure the parasitic resistances and capacitance from layout does not affect the performance. The layout parasitic is extracted using the Calibre software. The extracted components includes line resistance, line capacitance and coupling capacitance. The inductance is not considered in this analysis as the inductive values are very small and the frequency of operation is small

resulting in negligible effects on the results. This helps reduce the simulation time. Fig. 5.24 shows the typical transient performance of the A-LDO. The post layout simulation is very

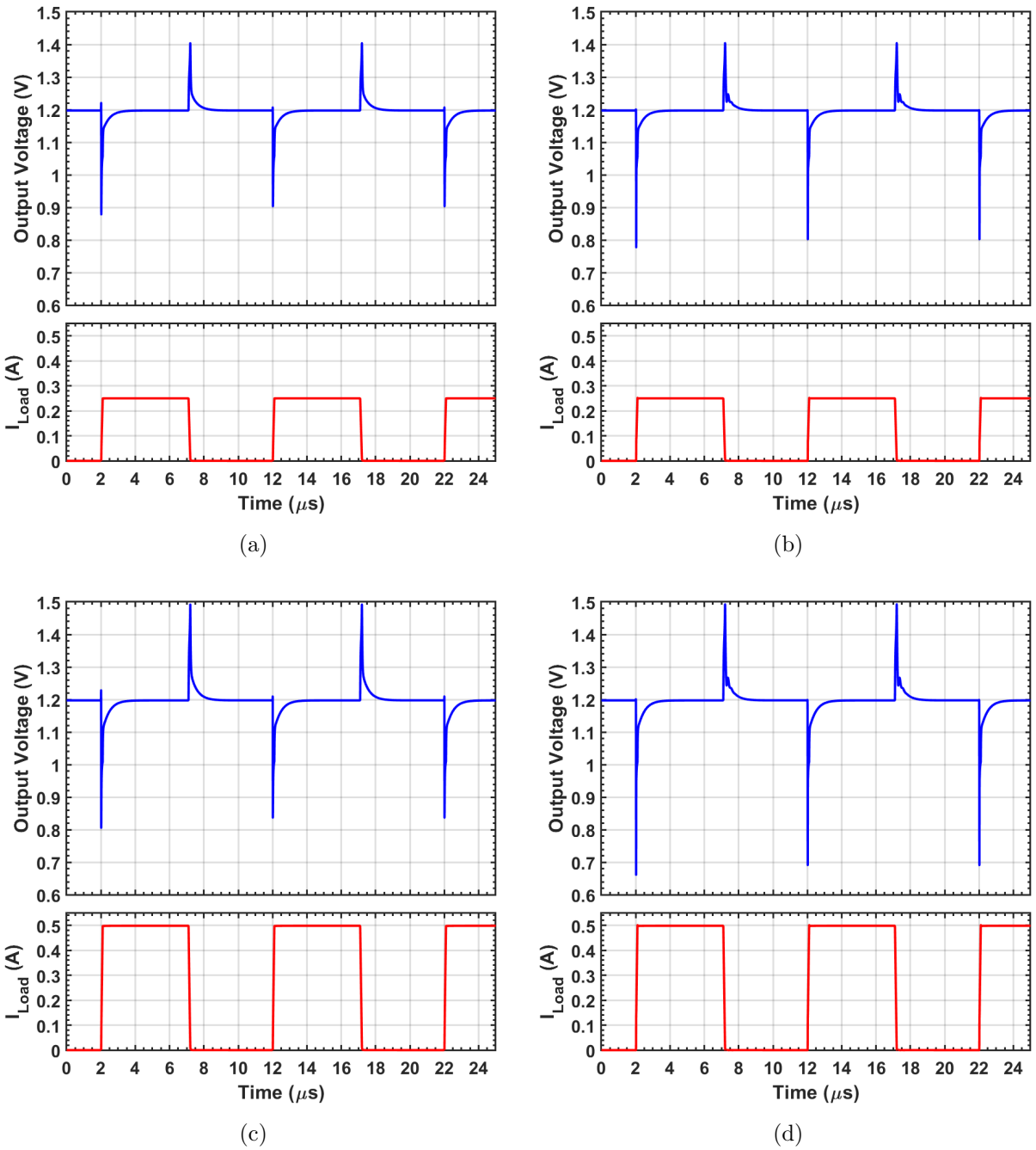


Figure 5.24: Transient simulation of post layout circuit at a) I_L = 0 - 250 mA, C_L = 0 pF b) I_L = 0 - 250 mA, C_L = 500 pF c) I_L = 0 - 500 mA, C_L = 0 pF d) I_L = 0 - 500 mA, C_L = 500 pF. Test conditions of V_dd = 1.8 V TT, 27$C°$ and V_{DO} = 600 mV, t_r = 100 ns.

similar to the schematic simulation meaning that the introduced resistance and capacitance from layout have minimal effects on the results. PVT variation can have a large effect on the circuit performance. Simulation of some of the corner conditions will be investigated. During the manufacturing process, the gm performance can vary by as much as ±15% according to the process documentation. Thus, the corner simulation must be performed when such variation occur. Model are provided by the foundry for simulating the SS and FF corner of the transistors. The designed working temperature of the A-LDO is from -40 °C to 70 °C. At low temperatures, the speed of a transistor increases and at high temperatures the speed of a transistor decreases. The worst case scenario for each conditions is where the A-LDO is subject to high temperatures and SS performance and when the A-LDO is subject to a low temperature and exhibits FF corner performance. Figs. 5.25 and 5.26 show the transient results for both cases respectively.

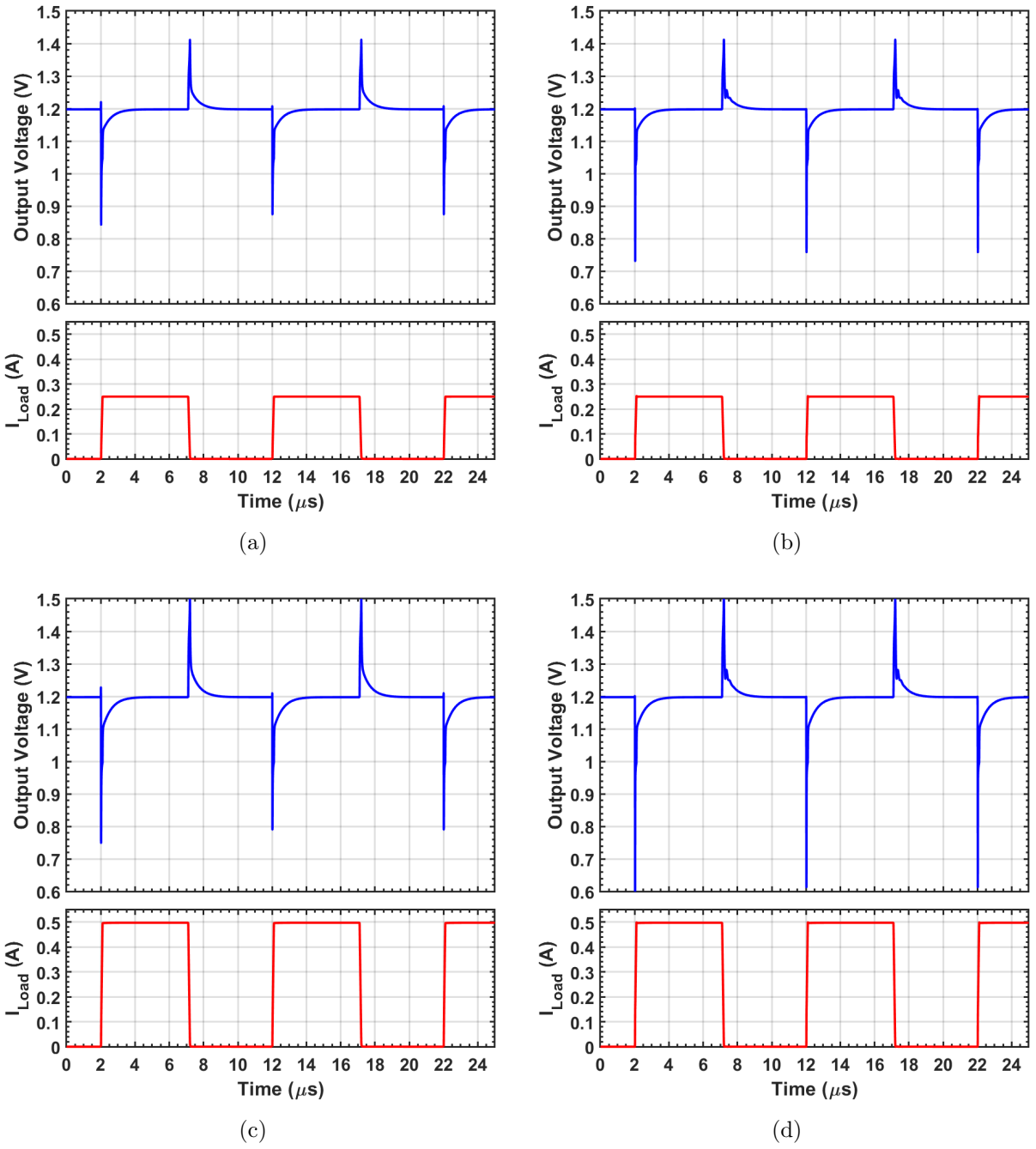


Figure 5.25: Transient simulation of post layout circuit at a) I_L = 0 - 250 mA, C_L = 0 pF b) I_L = 0 - 250 mA, C_L = 500 pF c) I_L = 0 - 500 mA, C_L = 0 pF d) I_L = 0 - 500 mA, C_L = 500 pF. Test conditions of V_dd = 1.8 V SS, 70 $C°$ and V_{DO} = 600 mV, t_r = 100 ns.

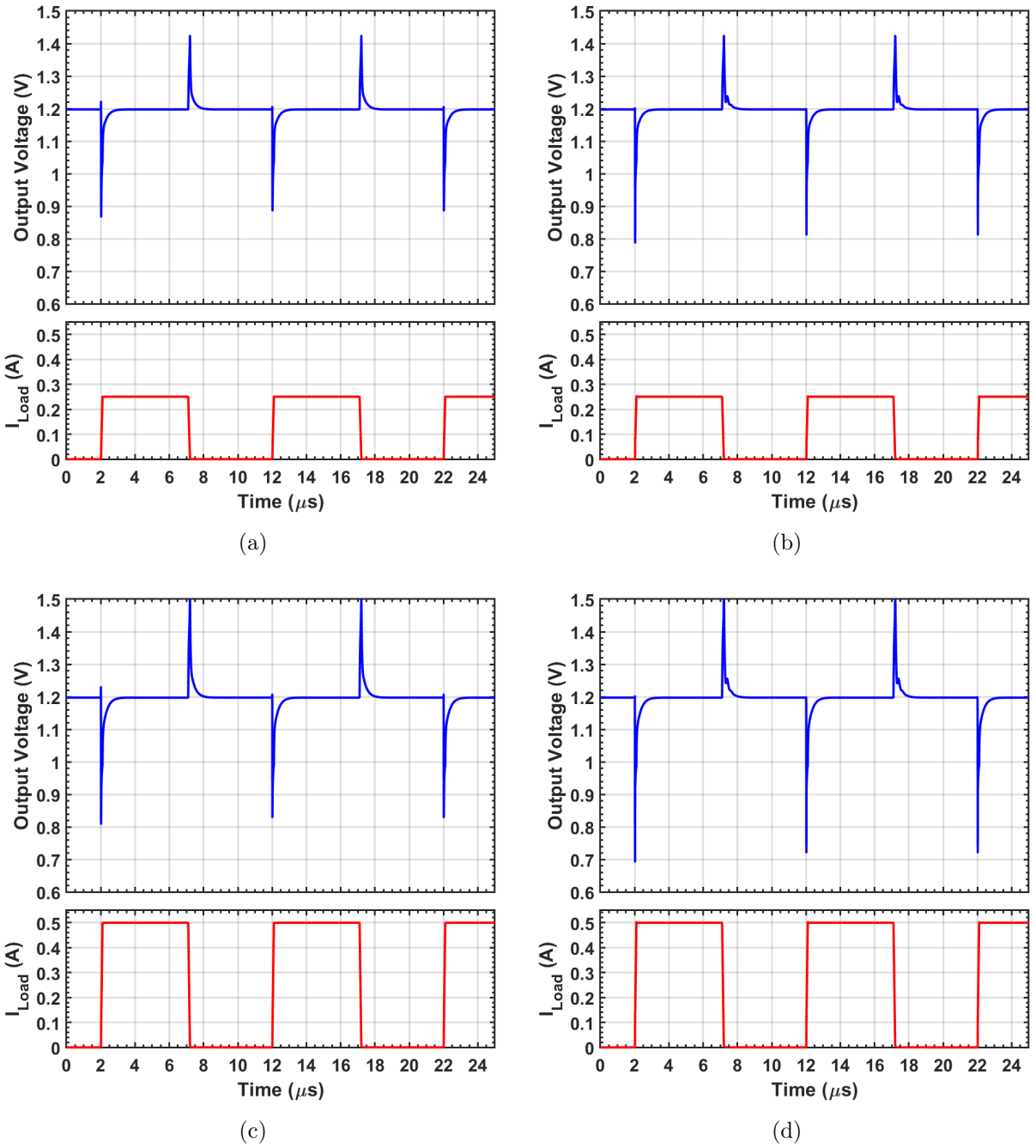


Figure 5.26: Transient simulation of post layout circuit at a) I_L = 0 - 250 mA, C_L = 0 pF b) I_L = 0 - 250 mA, C_L = 500 pF c) I_L = 0 - 500 mA, C_L = 0 pF d) I_L = 0 - 500 mA, C_L = 500 pF. Test conditions of V_dd = 1.8 V FF, -40 $C°$ and V_{DO} = 600 mV, t_r = 100 ns.

5.5 Measurements

The completed design is sent to the foundry to get manufactured using the TSMC 180 nm technology. The die micro graph of the A-LDO is shown in Fig. 5.27. In order to test the

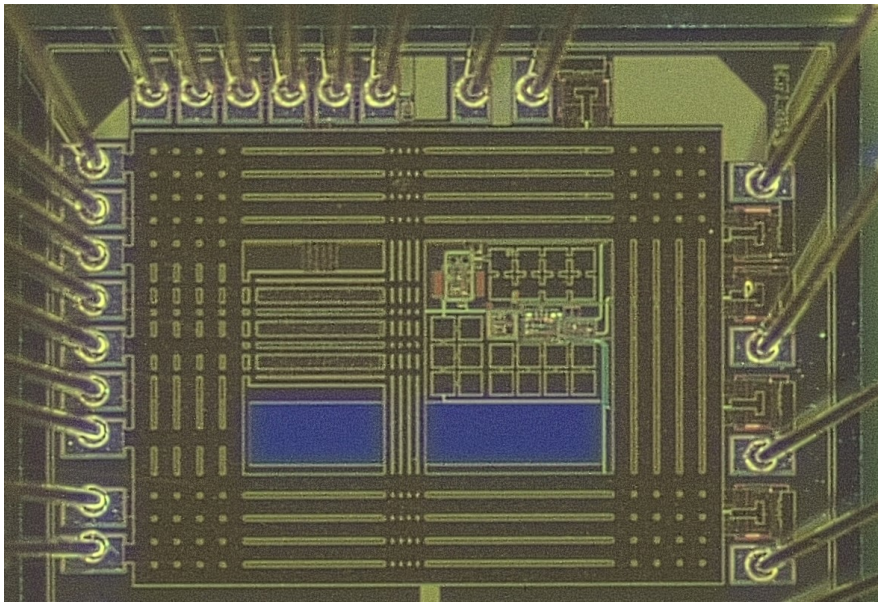


Figure 5.27: Manufactured die micro graph of the dual loop LDO regulator.

performance of the A-LDO, the die is packaged in a CPGA68 package allowing for simpler connections to external test circuitry. A custom PCB is manufactured to generate all the desired bias currents, reference voltage and load conditions. The bias current is generated using the LM334M adjustable current source. In order to measure the quiescent current consumption, the input and output current are monitored using a shunt resistor and the signal is amplified using the INA214 high precision current sense amplifier. A configurable input shunt resistor is used for increased precision when low load current is applied. The load current is set using two resistors. One resistor is always connected to the output setting the base load. If no load current is desired, then this resistor is left unpopulated. The second resistor is used to increase the load and is switched using an NMOS transistor. The rise time t_r can be modified by changing the slope of the gate signal of the NMOS. The load current can then be represented using Eq. 5.29.

$$I_{max} = I_{R,base} + I_{R,sw} \tag{5.29}$$

Where $I_{R,base}$ is the current flowing in the always connected resistor and $I_{R,sw}$ is the current flowing in the switched resistor. The load capacitance is varied using jumpers and preset

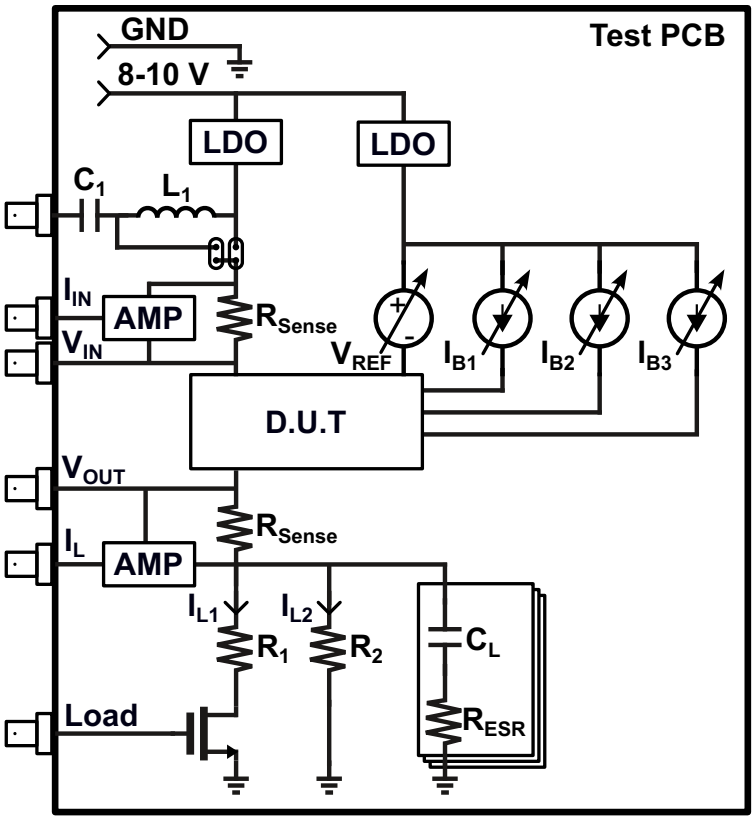


Figure 5.28: A-LDO test PCB diagram.

capacitors of 500 pF each. For PSRR measurements, a bias tee using a capacitor and inductor is implemented on the PCB. This enables the superposition of and AC and DC signal to supply current to the A-LDO while injecting the desired ripple on the supply line. In order to facilitate the measurement of all signals, test points and BNC connectors are added such that the signals can be directly connected to the measurement equipment. Fig. 5.29 shows the manufactured PCB with all the components populated. Using the equipment available in the lab at Lakehead University, the dual loop LDO is tested. First, the DC tests are performed. The quiesent current of the LDO regulator is measured at 1.278 mA at no load. When a load is applied to the output the maximum quiesent current measured is 17 mA. The increase in current is due to the increased current flowing in the current loop. The resulting current efficiency is 97.85 %. The load regulation is measured at different supply voltages and the load current is varied from no load to full load. Fig. 5.30 shows the resulting load regulation performance. A load regulation performance of 0.0146 mV/mA @ 1.8 V

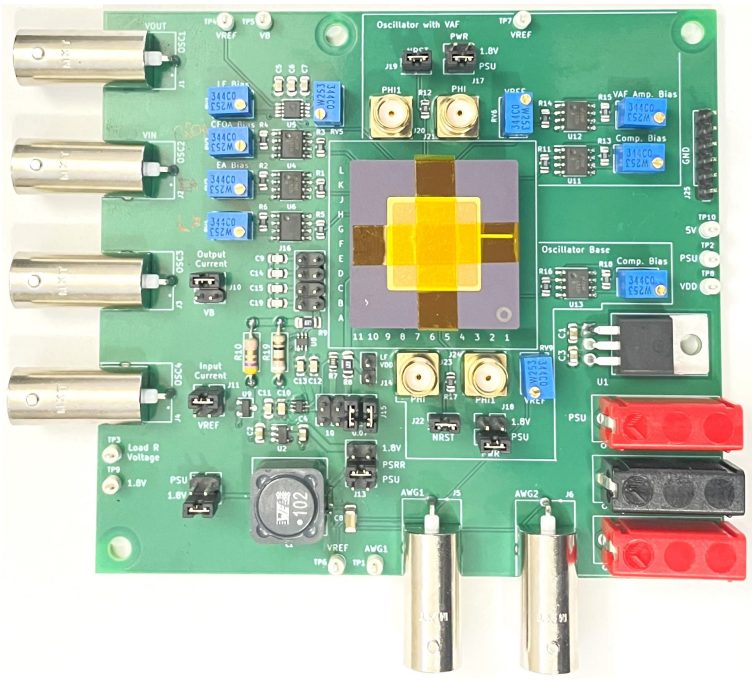


Figure 5.29: A-LDO test PCB.

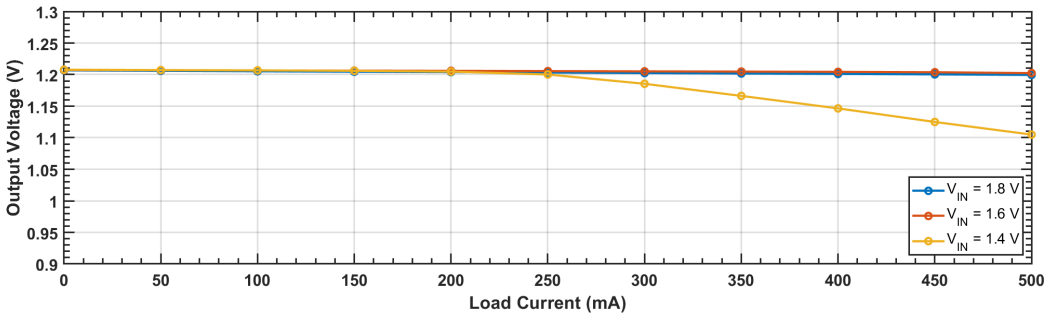


Figure 5.30: Load regulation measurements of the dual loop LDO.

and 0.0206 mV/mA @ 1.4 V is measured. The line regulation of the A-LDO is measured at different load currents. Fig. 5.31 shows the resulting line regulation performance. The measured line regulation of the dual loop LDO is 36.36 mV/V @ no load and 0.27 V/V @ full load. Based on Fig. 5.31 the minimum V_{DO} of the regulator while maintaining adequate output voltage is 300 mV. If the desired V_{DO} is lower then 300 mV, a reduction in maximum load is required. The transient simulation of the A-LDO can be performed next. The same transient conditions are used as the simulations. Fig. 5.32 demonstrate the obtained results.

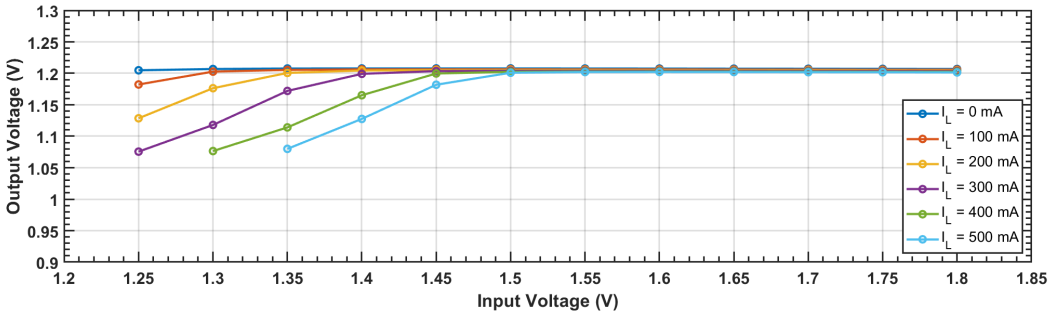


Figure 5.31: Line regulation measurements of the dual loop LDO.

The transient results show drastically reduced overshoot and undershoot values where the maximum droop measured is 27 mV. This is significantly better than the simulation results where the reduced droop is attributed to the extra parasitic of the PCB test board. The extra capacitance and line resistance introduced filters out the sharp loading spikes seen on the simulation results. The settling time of the LDO is measured when the output voltage reaches 3 % of the final value. The measured settling time is more than the simulated values at 3.2 μs on average. This is also attributed to the extra line resistance and capacitance that is introduced by the test PCB. The PSRR is measured from 1 kHz to 10 MHz. An oscilloscope is used to measure the PSRR where multiple measurements are performed and then plotted. Fig. 5.33 shows the PSRR performance with and without the feed forward line filter. The minimum PSRR measure is -50 dB @ 1 kHz. The addition of the line filter has a significant effect on the PSRR performance where in the range of 20 kHz to 5 MHz an average of 5.4 dB improvement is observed. With all the measurements taken, Table 5.3 shows a summary of the design performance as well as comparison to other state of the art designs.

5.6 Summary

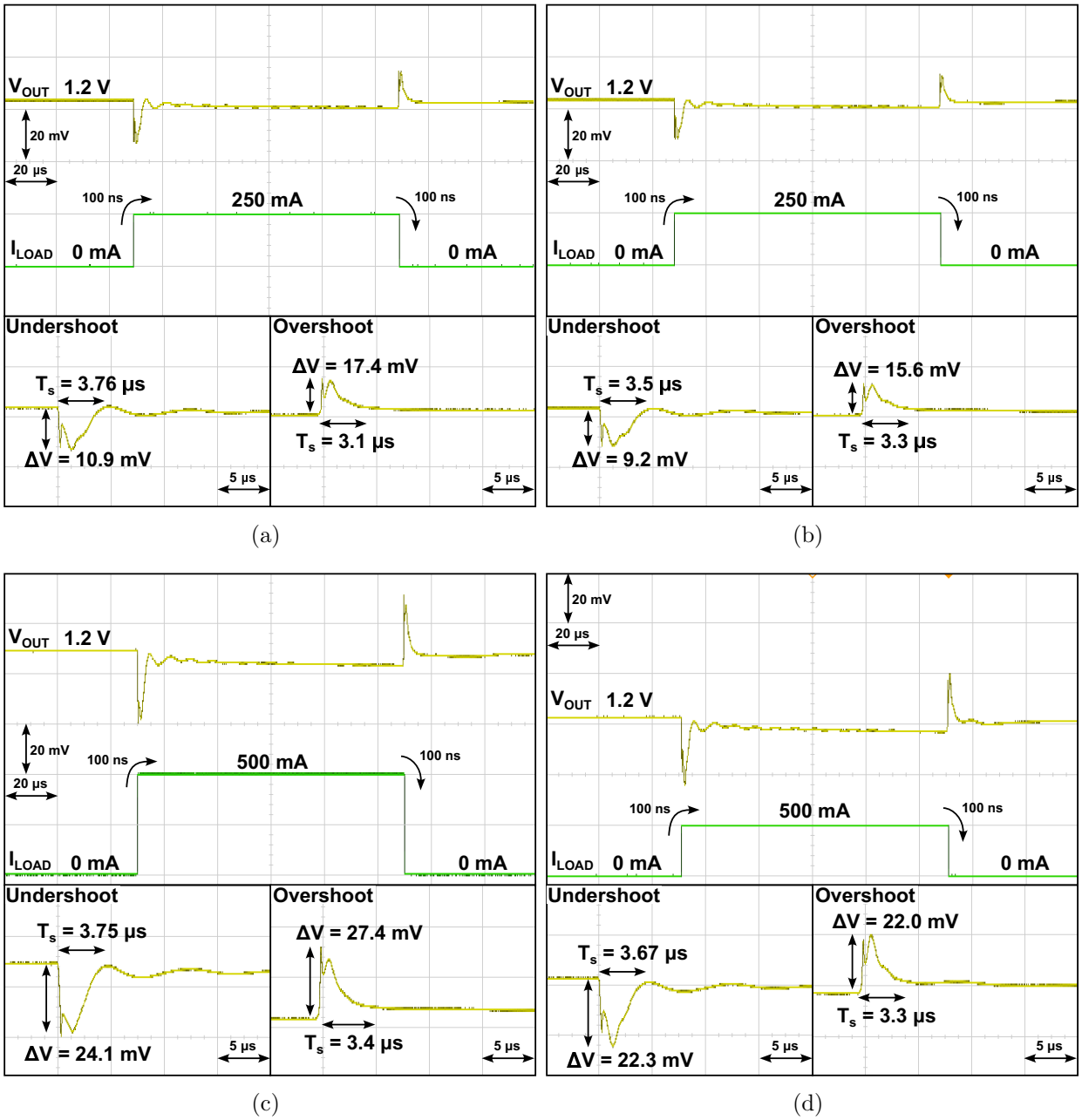


Figure 5.32: Measured transient results at a) I_L = 0 - 250 mA, C_L = 0 pF b) I_L = 0 - 250 mA, C_L = 500 pF c) I_L = 0 - 500 mA, C_L = 0 pF d) I_L = 0 - 500 mA, C_L = 500 pF. Test conditions of V_dd = 1.8 V, 27 C° and V_{DO} = 600 mV, t_r = 100 ns.

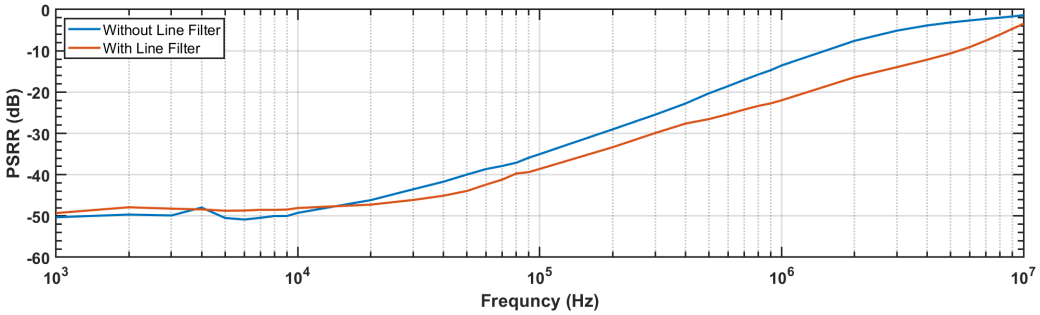


Figure 5.33: Measured PSRR performance with and without the line filter.

Table 5.3: Performance summary and comparison with state of the art designs.

	This Work	TCASI	TCASI	TCASII	TPEL	TCASII
Year	2024	2023	2012	2013	2017	2016
Technology (nm)	180	350	65	110	180	180
Architecture	Cap-Less	Cap-Less	Cap-Less	Cap-Less	LDO	Cap-Less
V_{IN} (V)	1.5 - 1.8	3.3	2	2.2	1.4	1.8
V_{OUT} (V)	1.2	2.5	1.2	2	1.2	1.6
V_{DO} (mV)	300	200	200	200	200	200
C_{LOAD} (pF)	500	100	100	40	1000000	100
C_{TOTAL} (pF)	16	14	4.5	40	1000000	12.7
I_q (µA)	1300	66	82.4	415	1.6	101
V_{Droop} (mV)	27.4	255	65.1	385	24	210
I_{Load} (mA)	500	100	100	200	50	100
Load Reg. (mV/mA)	0.0146	0.8	0.3	8.9	0.1	N/A
Line Reg. (mV/V)	36.36	0.06	4.7	0.108	5.5	131
Current Eff. (%)	97.85	99.83	99.91	99.79	99.6	99.93
T_{Edge} (ns)	100	400	300	500	10	100
T_{Settle} (µs)	3.76	0.7	6	1.6	1.2	0.2
K	10	40	30	50	1	10
PSRR (dB)	-38.6	-41	-58	N/A	-30	-76
Area (mm_2)	0.0131	0.077	0.017	0.21	0.0285	0.033
FoM_1 (ps)	0.00228	0.02356	0.00241	0.15978	15.36	0.03
FoM_2 (ps)	0.00857	0.01649	0.01448	0.25564	18.43	0.01
FoM_3 (mV)	0.712	6.732	1.609	39.944	0.001	2.121
FoM_4 ()	219.877	549.551	3808.928	33011.364	0.237	654.630

Chapter 6

An H-LDO with Fast Transient Approximation Algorithm

This chapter discusses the design and methodology of our research on an H-LDO using a novel approximation algorithm to enhance the transient speed of low clock frequency LDOs. The H-LDO is simulated and layout using the Cadence software. The proposed H-LDO is fabricated in a TSMC 180-nm CMOS technology and the performance was measured on a custom PCB board.

6.1 Objectives

Many applications require LDO regulators where low power and low clock frequencies are required. Such applications include microcontrollers, IoT and sensing devices [14, 48, 47]. Our research on the H-LDO focuses on improving the performance of the LDO regulator where low clock frequencies are used. This research focuses on improving the transient response of LDO's operating at low clock frequencies. The designed LDO is to be designed to handle up to 500 mA current and operate at low frequencies.

6.2 Proposed Design

The proposed architecture of the H-LDO using the novel approximation algorithm and droop detector is shown in Fig. 6.1. The H-LDO is composed of an A-LDO and D-LDO

working in parallel. The D-LDO uses a 6 bit power transistor array and is controlled using an approximation algorithm significantly improving the transient response at low clock frequency. The approximation algorithm is implemented using a charge distribution technique, digital logic and an adder/subtractor circuit. To reduce the droop voltage during load transients, a high pass RC circuit and a droop detector is added to the digital portion. The A-LDO is implemented using a simple low voltage EA and voltage only feedback. The A-LDO in this design supports 1/8 of the total load current thus this H-LDO implementation can be classified as an AAD-LDO.

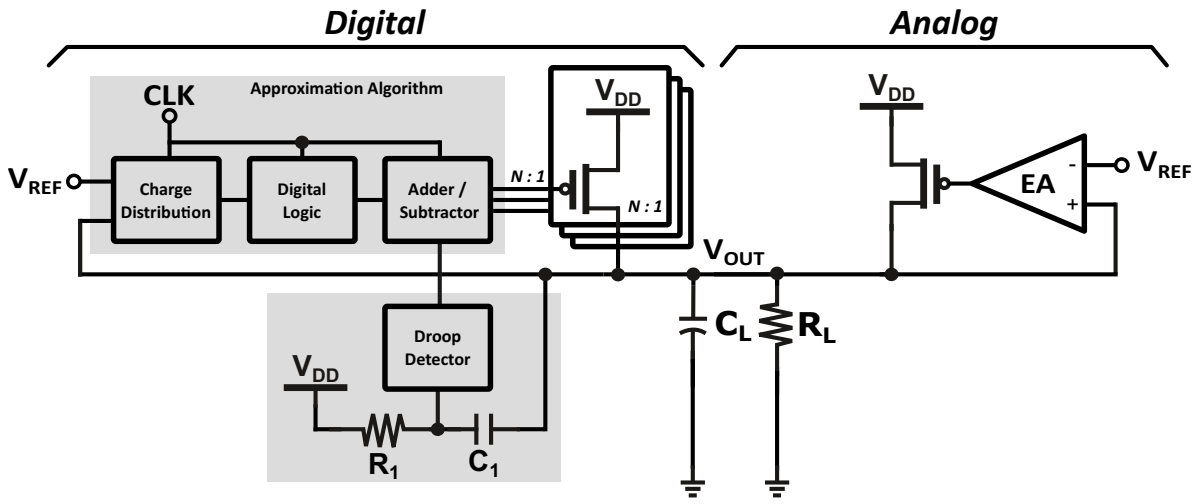


Figure 6.1: Proposed approximation algorithm H-LDO Architecture.

Chapter 3 demonstrated the tradoff between clock frequency and transient response where low clock frequencies result in poor transient response. The transient response time can be greatly improved using different algorithms such as the SAR algorithm which greatly improves the transient response time compared to the hill climb algorithm [12]. The SAR algorithm's main drawback are the large overshoots involved during the convergence process. Both of these algorithms converge to the output by changing the control word and looking at the results. In the case of the hill climb algorithm, the same step size is used after every iteration until convergence is achieved. Similarly, the SAR algorithm tests different size transistor sequentially until convergence is reached. Both methods "blindly" changes the

control word without looking at their effects on the output. This results in low transient speed for the hill climb algorithm and large overshoot for the SAR algorithm. The ideal algorithm response would be able to calculate the exact control word required after each clock cycles. When the control word is applied to the output, the correct output voltage would be attained. To achieve such a controller the desired control word N must be derived based on the available information. The load resistance can be modeled using:

$$R_L = \frac{V_{OUT_I}}{I_{LSB} N_I} \tag{6.1}$$

Where N_I is the current control word, I_{LSB} is the current supplied by the LSB transistor and V_{OUT_I} is the initial output voltage. This assumes that that the V_{sd} does not significantly change the current per transistor value. This is true when the output voltage is small. To achieve the desired output voltage, V_{OUT_F}, where N is added to the control word. The output voltage is defined by:

$$V_{OUT_F} = I_{LSB}(N_I + N)R_L. \tag{6.2}$$

Where V_{OUT_F} is the final output voltage after adding N to the control word. Using (6.1) and (6.2) the load resistance can be removed and solved for N as follow:

$$N = \frac{N_I(V_{OUT_f} - V_{OUT_I})}{V_{OUT_I}}. \tag{6.3}$$

As the voltage increases the power transistors enter the deep triode region where they act closer to variable resistors rather then current sources. Thus the equivalent resistance of the power transistors can be represented by:

$$R_p = \frac{V_{dd} - V_{OUT}}{N_I}. \tag{6.4}$$

Eq. 6.5 is used to calculate the the required control word change when the output voltage is high.

$$\begin{aligned} \frac{V_{dd} - V_{OUT_I}}{N_I} &= \frac{V_{dd} - V_{OUT_F}}{N_I + N} \\ N &= \frac{N_I(V_{OUT_F} - V_{OUT_I})}{V_{OUT_I} - V_{dd}} \end{aligned} \tag{6.5}$$

Using (6.3) and (6.5) a good approximation of the required N is obtained. This method assumes that the changes in V_{sd} have little effect on the transistor current. Fig. 6.2 shows a simulation of the approximation error over the voltage range of the regulator. Where the

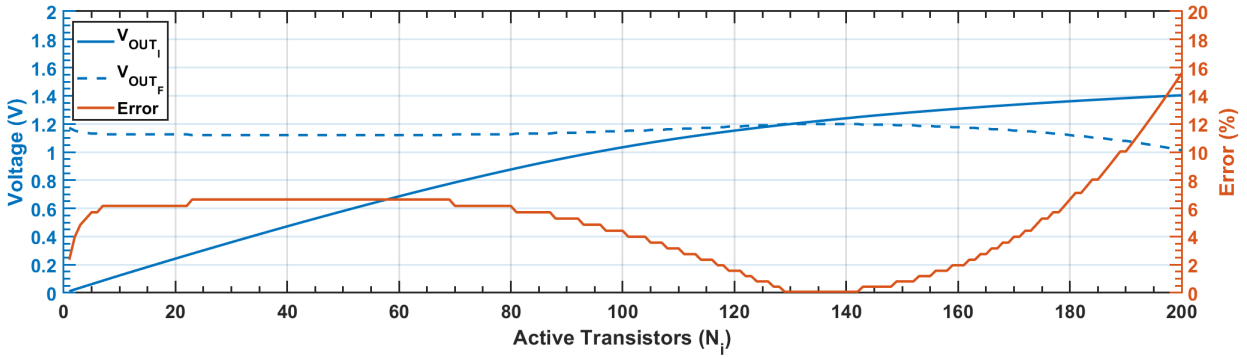


Figure 6.2: Approximation algorithm over a single cycle with varied N_I with a fixed 500 mA load current and V_{Ref} at 1.2 V.

LSB size is set to 1 μm. The results in Fig. 6.2 show that in a single cycle, the algorithm can return the output voltage to within 16 % error margin which is significantly better than the hill climb algorithm where where the error doesn't change significantly for each step. The mean error over the entire range of the LDO is 5 %. Using this algorithm also results in no overshoot as the estimation ensures that the output remains close to the desired voltage as seen form the final voltage represented by V_{OUT_F}. When using this algorithm continually, an accurate output can be achieved within a small number of cycles. Fig. 6.3 shows the number of cycles required in order to reduce the error below 0.5 %. The algorithm is able to achieve a high level of accuracy with fast convergence resulting in a fast transient response. Compared to the the hill-climb algorithm, that requires on average 128 cycles and the SAR

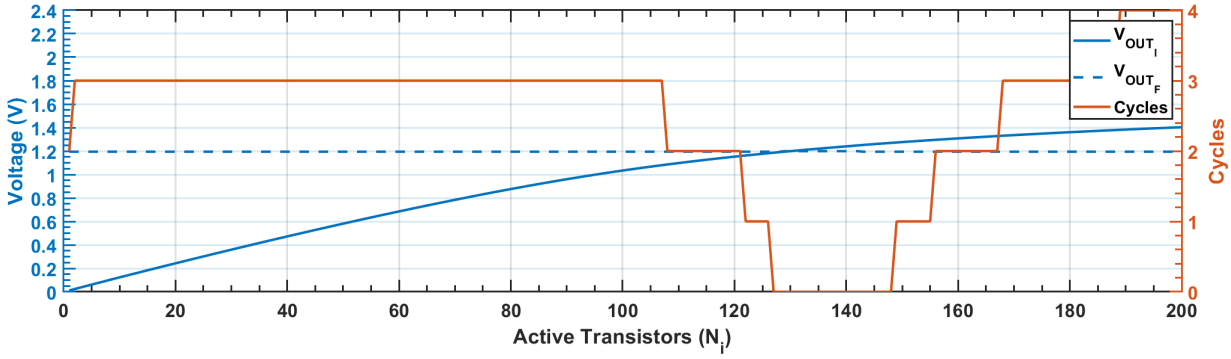


Figure 6.3: Approximation algorithm cycle requirements to reach an error < 0.5 % with varied N_I with a fixed 500 mA load current and V_{Ref} at 1.2 V.

algorithm that requires 8 cycles with an 8 bit array, the approximation algorithm proves to have significant speed benefits with a mean cycle of 2.16 to reach a 0.5 % error margin.

During the analysis of the approximation algorithm, it was assumed that the load and power transistors exhibit linear relationships. When implementing the regulator the power transistors and the load will be non-linear in nature. When the approximation is applied to such loads, increased output errors and oscillations may occur due to the introduced error. To reduce the effects of non-linear loads, three methods are implemented. First the resulting N obtained from the approximation is rounded. When the approximation is completed, a reduction in N reduces the approach to the desired output voltage in multiple steps. This significantly reduces the error as the output voltage gets closer to the desired voltage improving the convergence of the algorithm. When implementing the transistor array, a binary array is used. Thus for the approximation algorithm, the results are rounded to the nearest binary digit. In order to ensure that the algorithm maintains its transient performance, a simulation is conducted with the rounding to the nearest binary digit shown in Fig. 6.4. It is not surprising that the algorithm maintains a speed advantage compared to the hill-climb and SAR algorithm with an average number of cycles of 4.8. One can consider this as a SAR algorithm that is capable of activating only the desired bits without testing all the bits one by one. The second method to improve non-linear load capability is the inclusion of oscillation detection circuitry. This circuit monitors the control word of the power transistor array. If 2 approximations of the same magnitude in opposite direction

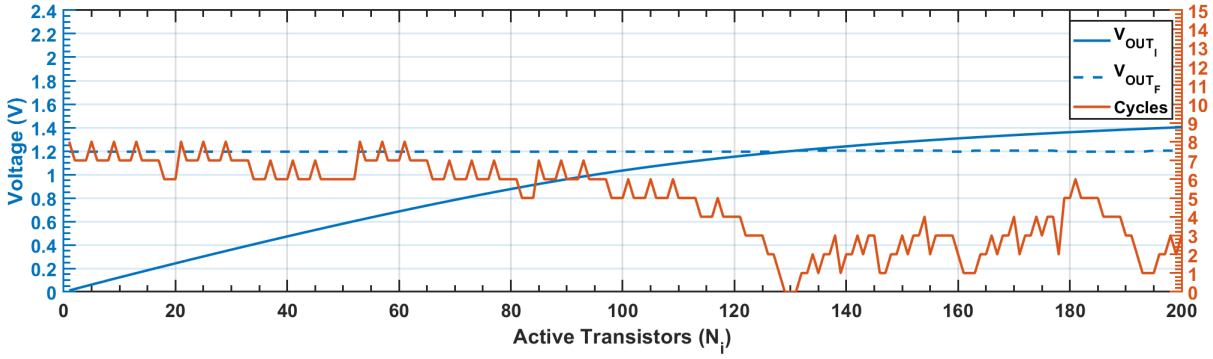


Figure 6.4: Approximation algorithm with rounding to the nearest bit cycle requirements to reach an error < 0.5 % with varied N_I with a fixed 500 mA load current and V_{Ref} at 1.2 V.

occur sequentially, then oscillation will be present on the output. The ideal control word can be found within the 2 approximations. Using the bisection method, the approximation is divided by half leading the output voltage to be closer to the desired output. Finaly the non-linearaties may cause larger output error resulting in poor load and line regulation of the H-LDO. This cannot be removed using the approximation algorithm as near the desired voltage the approximation may indicate that the ideal control word is reached even if the the non-linearity would require a small change of control word for optimum precision. To improve the regulation performance, the hill-climb algorithm can be used next increasing the control word in small increments until the output voltage crosses V_{Ref}. At this point, the output voltage is closest to the desired value as possible. All of these techniques combined result in a robust, high speed, high precision algorithm suitable for low frequency applications.

For the approximation algorithm to function properly, a method for calculating (6.3) and (6.5) in circuit must be found. This could be done using an ADC sampling the output, and all the formulas being implemented digitally. While this would result in functioning design, a high resolution ADC would be required in order to obtain the desired accuracy increasing the current consumption and silicon area of the design. Solving (6.3) and (6.5) for V_{OUT_I} results in:

$$V_{OUT_I} = \frac{N_I V_{OUT_F}}{N_I + N}, \tag{6.6}$$

$$V_{OUT_I} = \frac{N_I V_{OUT_F}}{N_I + N} + \frac{N V_{dd}}{N_I + N}. \tag{6.7}$$

Comparing (6.6) and (6.7) to the charge distribution formula for parallel capacitors, it can be seen that they express the same formula:

$$V_{OUT} = \frac{C_1 V_1}{C_1 + C_2} + \frac{C_2 V_2}{C_1 + C_2}. \tag{6.8}$$

Based on this, the approximation algorithm can be implemented using the charge distribution principle. Two capacitor arrays are used, one representing the relative power transistor size and the second representing the values of N. For our case, a binary sized power transistor array is used thus the C_A capacitor array is size as 2^n where n represents the resolution of the power transistor array. The C_B capacitor array is sized such that its sum represent the binary digits to be estimated, in our case equal to 2^{n-1}. Fig. 6.5 shows the basic diagram of the charge distribution. The C_A capacitor bank represent the active power

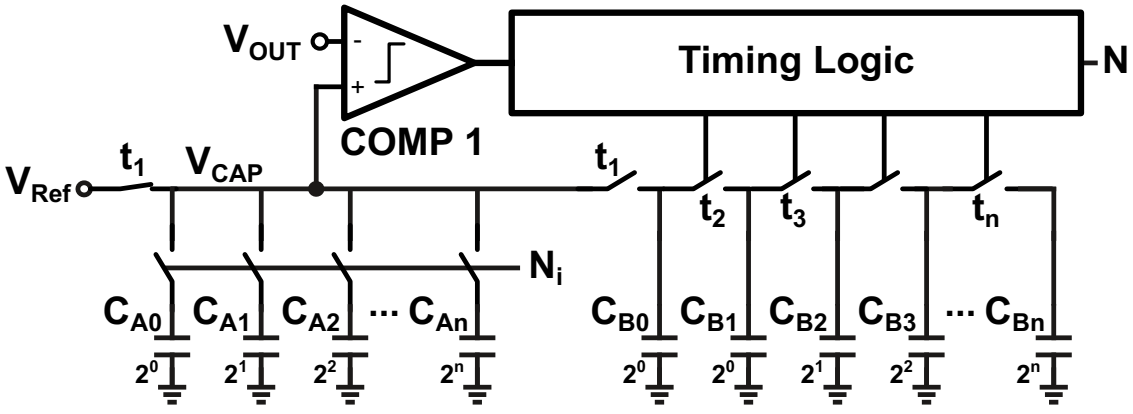


Figure 6.5: Charge distribution schematic.

transistors set by N_i. If the corresponding transistor is providing current to the output, the

switch is closed representing that the transistor is active. During the charge phase, when the CLK is low, the C_A capacitor array is initially charged to V_{Ref} which is the desired output voltage. If the output voltage is lower than V_{Ref}, the C_B capacitor bank is discharged to GND. When the output voltage is higher than V_{Ref} the C_B capacitor bank is charged to V_{DD}. At the rising edge of the clock the smallest capacitor from C_B, with a relative size of 1, is connected to the first capacitor bank at t_1. Charge distribution reduces the voltage on the C_A capacitors array. The voltage V_{CAP} is then compared to the output voltage using COMP1. If the voltage on the capcitor bank crosses V_{OUT}, then no extra transistors need to be added as the approximation estimates that adding one to the control word will cause the output to cross V_{REF}. If not, the next transistor from the second capacitor bank is added to the output at t_2. The voltage V_{CAP} is compared with the output voltage again. The process continues until a) V_{CAP} crosses the output voltage or b) the end of C_B capacitor array is reached. If the the first condition is met, the desired number of transistor to add to the output, N, is equal to the equivalent number of capacitors added to the C_A array that did not cross the output voltage. If the end of the C_B array is reached, then N is set to the largest value of C_B. This method enables high accuracy due to the analog comparison of the capacitor bank voltages to the output. The method also leverages the the commonly used charge distribution in the SAR implementation for ADC thus has already been proven as a viable technique for implementation. [39, 40, 41, 42] The approximation algorithm requires at minimum that one transistor in the array be active. If that is not the case, then no approximation is preformed as any transistor added will instantly change the output V_{DD} or GND. Extra circuitry is needed in order to prevent this situation. The steps of the approximation algorithm using the charge distribution is shown in a state diagram in Fig. 6.6 and summarized as follows:

1. Charge C_A capacitors based on currently active transistors to V_{Ref}.
2. Charge or discharge the C_{BN} capacitors based on overshoot or undershoot.
3. Add capacitors C_{BN} until V_{CAP} crosses V_{OUT} or the end of the array is reached.
4. Set N as the number of C_{BN} added that did not cross the output.

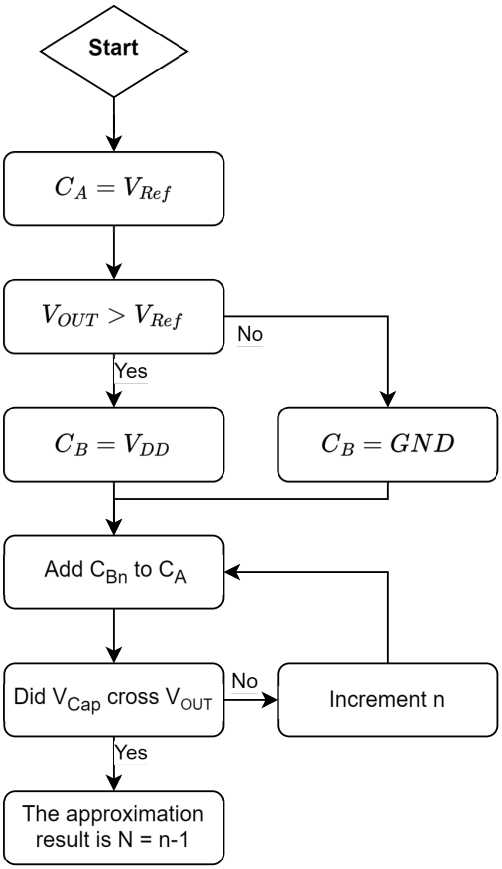


Figure 6.6: State diagram for implementation of the approximation algorithm.

For example, Fig. 6.7 show a typical example of the V_{CAP} during an estimation phase. N_I is set to 6 thus the capacitors C_{A1} and C_{A2} are connected to V_{CAP}. Since the output voltage is lower than V_{Ref} the C_B capacitors are discharged to GND. At t_1, the first C_B capacitor is connected to C_A and V_{CAP} is compared to the output with no change. The next two C_B capacitor is then connected and compared to the output at t_2 and t_3. V_{CAP} crosses V_{OUT} at t_3, the sum of added capacitors are $2^0 + 2^0 = 2$ thu $N = 2$. The approximation algorithm estimates that the control word should be set to $N_I + N = 8$.

For the charge distribution to function as intended, a small delay must be added in order to allow the capacitor charge to distribute from one array to the other. This delay is implemented using a current starved inverter cell shown in Fig. 6.8. Each of theses cells introduce a small delay using the RC constant. Transistor M_{4D} limits the current of the pull down network introducing a delay to discharge the capacitor. In order to reduce the size of

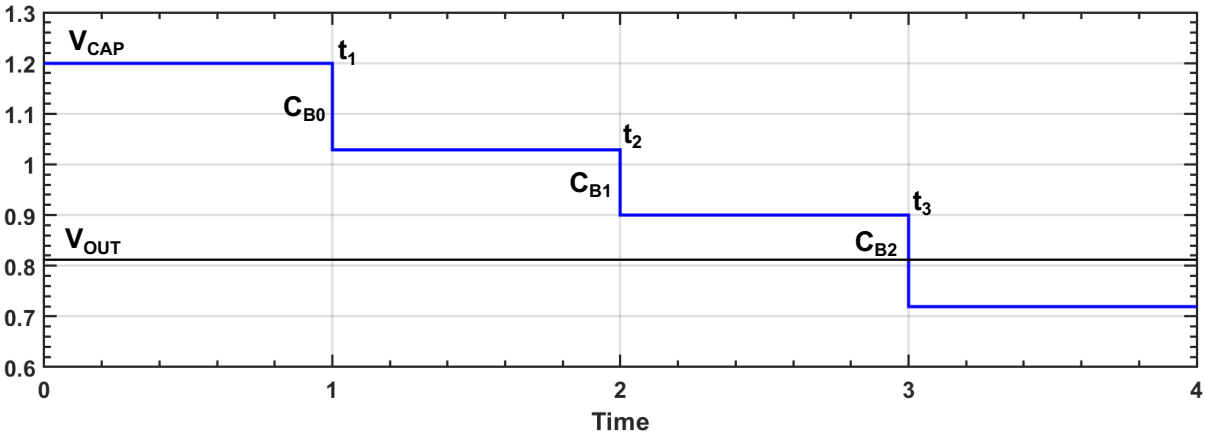


Figure 6.7: Example of charge distribution implementing the approximation algorithm using $V_{DD} = 1.8$, $V_{Ref} = 1.2$ and $N_I = 6$.

the capacitor, a very small current is used along with the smallest size of capcitor. Due to the slow rise time of the current starved inverter, large dynamic current is observed during the transition period. In order to limit this current, a long channel device is used limiting the maximum short current. The delay cells only provide a delay in the rising edge of the input signal, on the falling edge, the capacitors are charged rapidly with the pull up network. Three of these cells are used in order to implement a single delay from one capacitor to the next. This allows sufficient time for the charge distribution to occur.The clocked comparator is triggered at the 2/3 point in the cycle to analyze the output.

After each C_B capacitor addition, a clocked comparator is used to determine if the bank voltage crosses the output voltage. The comparator used is a strong arm clocked comparator shown in Fig. 6.9. This accurately compares the voltage between both of its inputs at every rising edge of the clock. It uses a pair of inverters that are inter connected. The inverter with the highest voltage will respond faster than the other thus it will remain active and deactivate the other inverter providing the results of the comparison. When the clock goes low, the the inversters are charged back to their initial state for the next clock cycle. A latching circuit is used to maintain the output during the charge mode.

Another comparator is used to determine if V_{OUT} is above or below V_{Ref}. This comparator must be continuous as the output may change state at any point in the cycle. The continuous comparator used is the strong arm comparator with cross coupled load. The

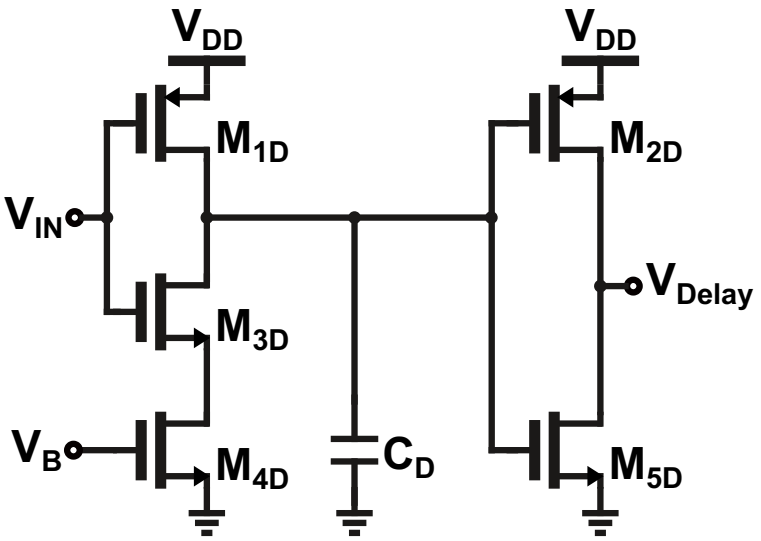


Figure 6.8: Delay cell transistor level diagram.

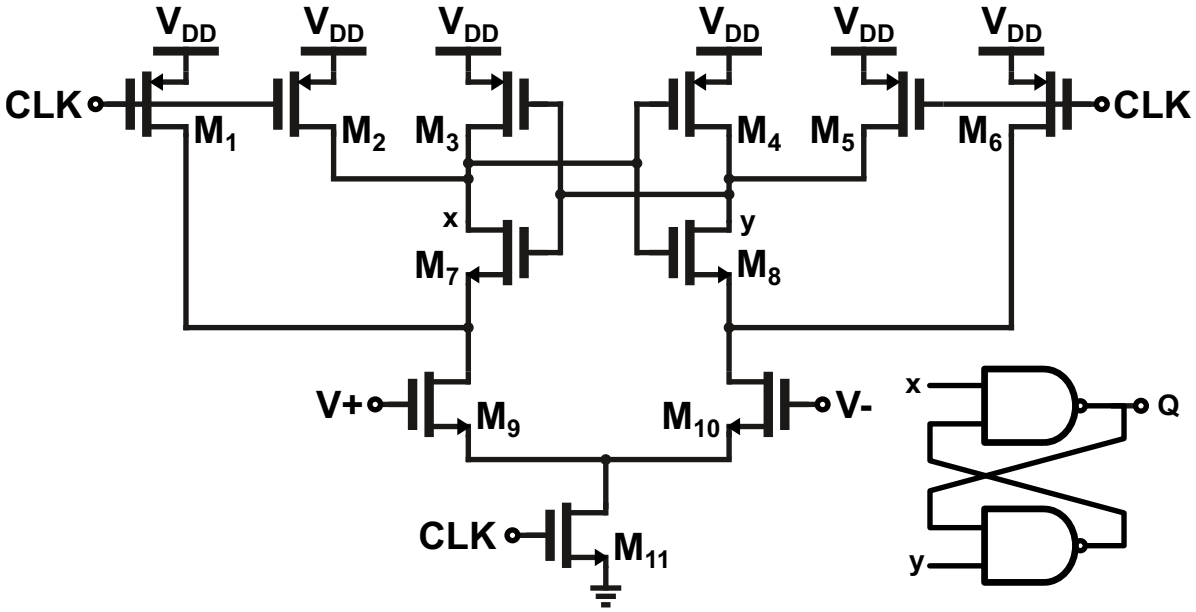


Figure 6.9: Strong arm clocked comparator transistor level diagram.

cross coupled load enables better matching an a more accurate output. Fig. 6.10 shows the schematic of the continuous comparator.

With all the charge distribution network complete, the entire circuit can be put together to form the entire operation cycle. The results from the approximation can then be

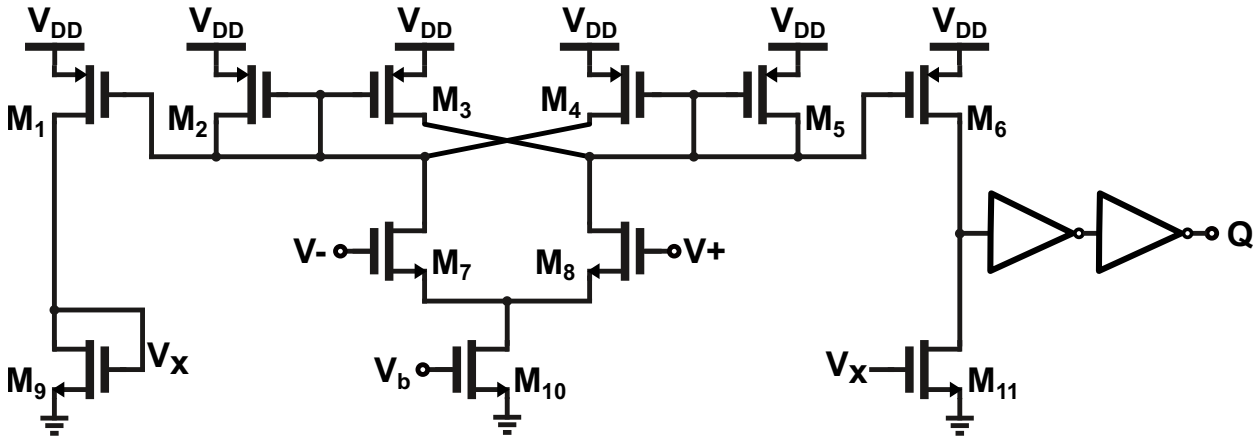


Figure 6.10: Strong arm comparator transistor level diagram.

tested for any oscillations and added or subtracted from the current number of active power transistors. The entire cycle can be represented as follows and is represented using the state diagram in 6.11

1. Perform the approximation using the charge distribution
2. If the approximation return a $N = 0$ then enter the linear mode until we cross V_{Ref}
3. If the approximation return a $N \neq 0$ check if it will cause oscillations.
4. If not add / subtract the approximation to the current number of output transistors.
5. Repeat from set 1 at every clock cycle.

The addition and subtraction is completed using a digital adder and subtractor. Extra logic is added to the add/subtract circuit to ensure the output does not overflow. The circuit is clocked using DFF such that the output is retained after each cycle. The output of the adder represents the control word for the D-LDO used to drive the power transistors. The digital logic gates are not capable of rapidly charging and discharging the large gate capacitance of the power transistors. To increase the driving capability, an inverter chain is added at the output of the adder for each bit. The power transistor are binary sized resulting in a varying gate capacitance. If all the inverters driving the power transistors are the same size, then each bit would exhibit a different charge time. This is unacceptable as it could

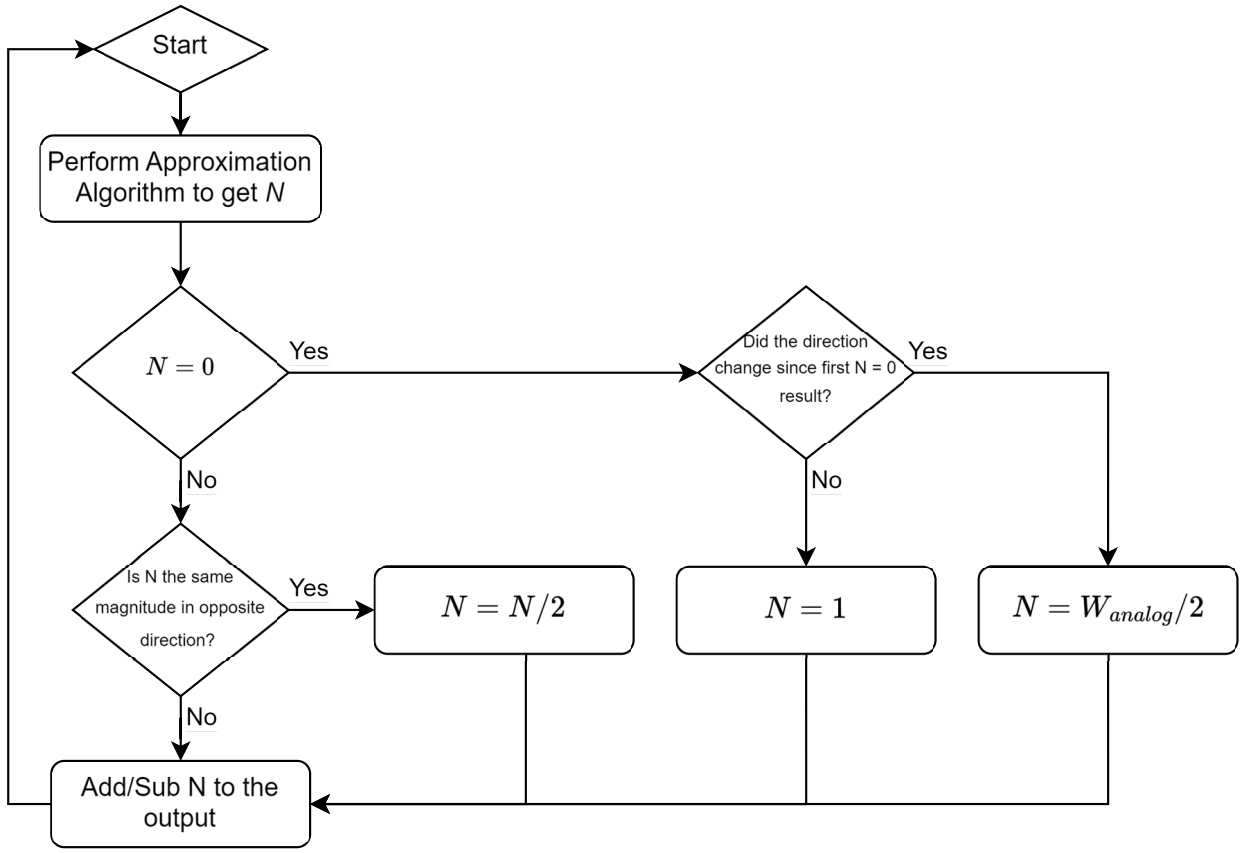


Figure 6.11: State diagram for full cycle implementation of the D-LDO algorithm.

cause glitches where the output spikes quickly during the transition period. Glitches are caused when a transistor is turned on and the other turned off, due to the unequal transition time, the current is reduced quickly and then compensated by the slower transistor causing a spike at the output. To reduce the glitches, we want the transition period between each transistor to the the same. This is accomplished using 3 inverter stages. All the power transistors get the same number of stages in order to maintain the same propagation delay introduced by each inverter. Larger transistors require a larger driving capability increasing the size of the inverter stage in order to maintain the inverter width ratio between each transistor the same. Glitches may still occur, where a drop in output voltages is significantly worst than an increase. A drop in voltage may cause the proceeding circuit to not function, for example in a memory system, bits could be dropped if the voltage gets too low but remain if an increase is seen. To ensure the that if glitches occur they will be in the positive

direction, the inverters are all set such that they have a slightly faster pull down network compared to the pull up network. This results in the PMOS power transistor being activated before the other transistors are turned off resulting in any glitches to cause an increase in output voltage. Fig. 6.12 show the driving setup for the driving inverters.

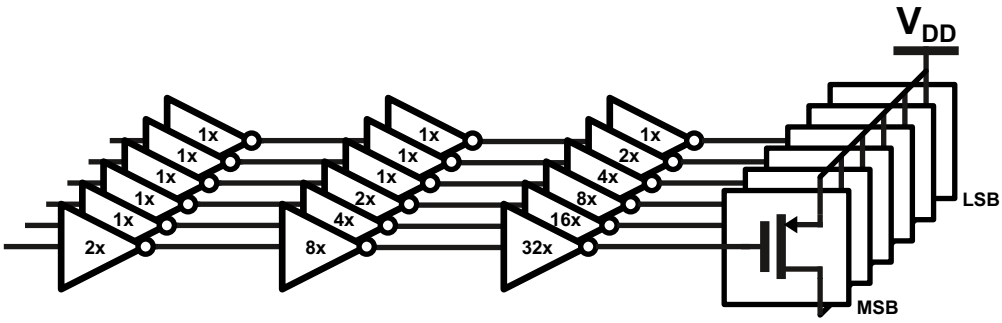


Figure 6.12: Power transistor driving inverter size schematic.

When the D-LDO operates at low frequency, the cycle period can be quite long. This means that the droop voltage is large in the case of fast transient load change. For example, a D-LDO operating at 10 MHz has a period of 100 ns between each rising edges. A load that transitions faster than 100 ns will not be compensated as it occurs faster than the clock period. Loads that are close the the sampling frequency will also exhibit large droop as all digital algorithms require many cycles to converge to the desired output voltage. Thus the droop voltage will be significant especially when a large load changes occurs. Fig. 6.13 show the droop voltage of a D-LDO with various load edge times. In order to reduce the droop voltage an asynchronous system is be implemented. The droop detector should be independent of the system clock and continuously monitor the output voltage while not consuming much quiescent current. The use of a high pass filter has been used to reduce droop volatges in previous designs. [14, 30] This method does not use any extra quiescent current and is capable of reducing the droop voltage. The implementation in [30] consumes large area and is not effective at light loads. The use of a digital in [14] solves some of these problems but maintains the output voltage based on the threshold of the transistor which is high for older technology. In order to solve these issues, we propose the use of a backwards

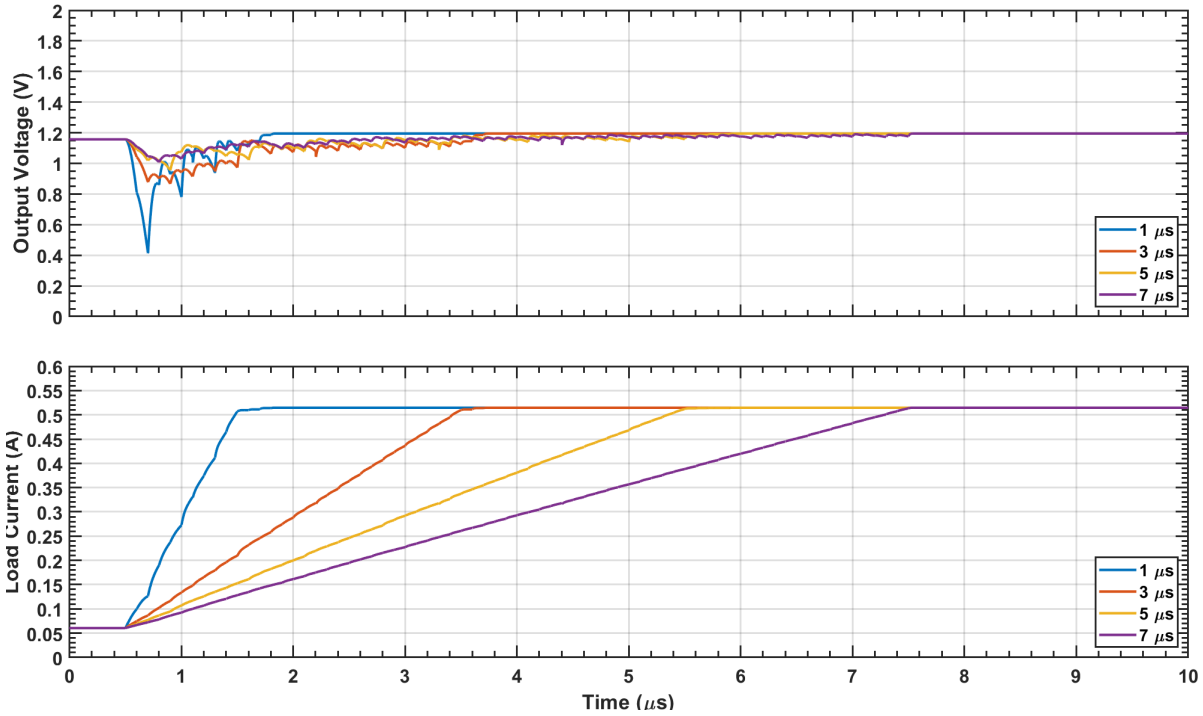


Figure 6.13: Output voltage with varying load edge time for a 450 mA load step.

binary algorithm using a footed inverter setup shown in Fig. 6.14. The footed inverter has 2 operation modes, when ϕ is high the inverter is in the pre-charge mode, where the output is kept low and the input is deactivated. When ϕ is low enables the evaluation phase where the output of the inverter remains low. During a sharp drop in output voltage, the capacitor drops by the same amount reducing the voltage on the input of the inveter. If the votlage drops low enough, the M_{2D} charges the drain capacitance of the NMOS and pulls up the ouptut high. Even if the input voltage is restored , the output is kept at a high level and can only be reset when in the charge phase. This allows a small drop in voltage to be detected as only a small amount of current is needed in order to charge the output of the inverter. The backwards binary is implemented where the LSB transistor is activated first. If the output voltage does not increase significantly, the next size up is activated and so on in order to maintain the output voltage at a high level. In order to have continuous operation, the first stage of the footed inverter is duplicated in a complementary pair such that one inverter is always in the evaluation phase. The RC time constant of the high pass filter is optimized such that it can effectively detect any sharp transients that has a higher frequency than the

clock. This algorithm has the benefit of being fast and easy to implement, while having quite low accuracy making it only good for droop detection purposes.

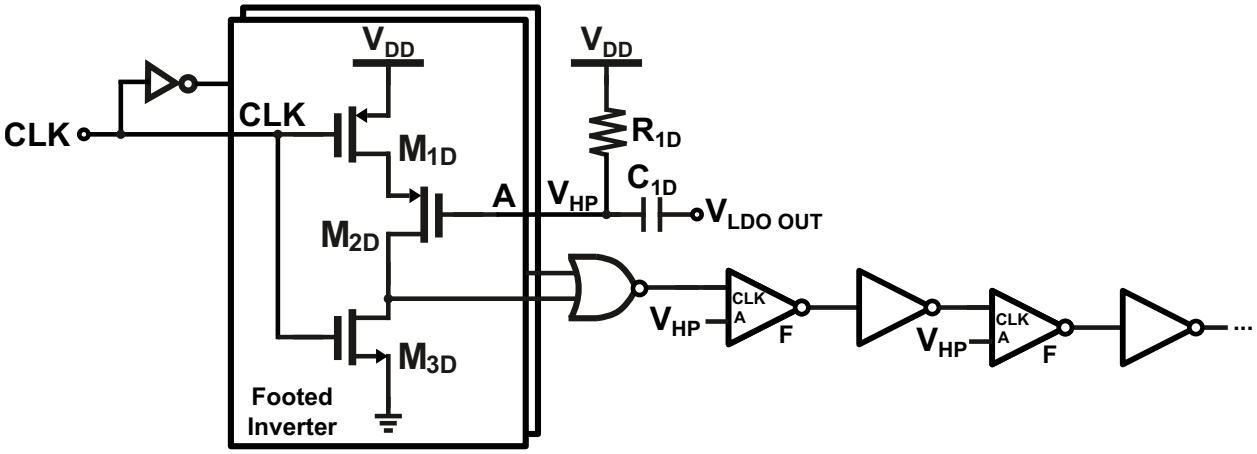


Figure 6.14: Inverter based droop detector architecture.

In order to increase the load and line regulation, PSRR and current range of the desired LDO an analog loop is added in parallel to the digital loop as depicted in Fig. 4.1. For this design, the base line current is provided by the D-LDO and the A-LDO is only used for increased output accuracy. The A-LDO is able to provide sub-LSB current to the load increasing the regulation. The small size of the power transistor used for the A-LDO enables high transient speed with a low power consumption EA simplifying the design considerably. When implementing a paralleled H-LDO one of the common issues is the distribution of load current between the power transistors of both regulators. For expample, assuming a particular design has a fast response time A-LDO and the D-LDO operates at a low clock frequency. When a load change occurs, the analog immediately changes the voltage at the gate of the power transistor saturating it. This assumes that the A-LDO power transistor is not sufficiantly large to supply the load current which is often the case. Then the D-LDO adjusts the control word in order to return the voltage to the desired value. At this point, the analog system is still saturated and cannot help to regulate the load resulting in no performance gain from the analog portion. Further more, the SAR algorithm cannot be

used at the same time as an analog EA. This is due to the addition of the analog current at the load fluctuating in order to maintain the voltage as close to V_{Ref} as possible. This then creates an error during the SAR convergence where an incorrect bit approximation may be added to the output that then yields an improper result and may also cause the A-LDO portion to saturate. To fix these issues is commonly done by deactivating one of the LDO's or by adding extra logic to ensure proper functionality [13].

Using the approximation algorithm greatly simplifies the addition of an A-LDO. First, a capacitor is added to the C_A array to represent the power transistor size of the A-LDO. This then ensures that the current contribution of the A-LDO are taken into account when performing the approximation algorithm. The addition of the C_A capacitor only adds the full current of the A-LDO to the approximation which is not representative of the actual current. This is not an issue for this design for 2 reasons. First, the A-LDO has a small power transistor thus the transient speed is faster than the D-LDO with the low clock frequency. This means that the A-LDO can often respond within the period of a single clock cycle. Second, if the A-LDO is still in transient when the approximation is performed, the full load is taken into account thus even after the approximation is complete, the A-LDO is capable of settling and provide the needed current that the approximation assumed initially. This enables the D-LDO and A-LDO to always function at the same time. This still leaves the issue where the A-LDO may be left saturated reducing its contribution to the output. One method to fix this is to monitor the gate voltage of the EA and change the output control word until it is within the desired limit [13]. This requires 2 extra reference voltage for the window and 2 comparators increasing the current consumption and the complexity of the design. The method used with approximation algorithm eliminates the use of comparators and reference voltages. Then the algorithm converges and the linear mode is activated, the A-LDO will be saturated as discussed earlier. When the output voltage crosses V_{Ref} the current supplied by the D-LDO and the A-LDO are such that they are as close to the desired voltage as possible. When this occurs, if the D-LDO reduces the control word by half the size of the analog in the previous direction then the A-LDO is capable to compensate half the total current capability. This means that the A-LDO is ideally biased at half its current capability and is able to accurately regulate the output voltage as well as improve

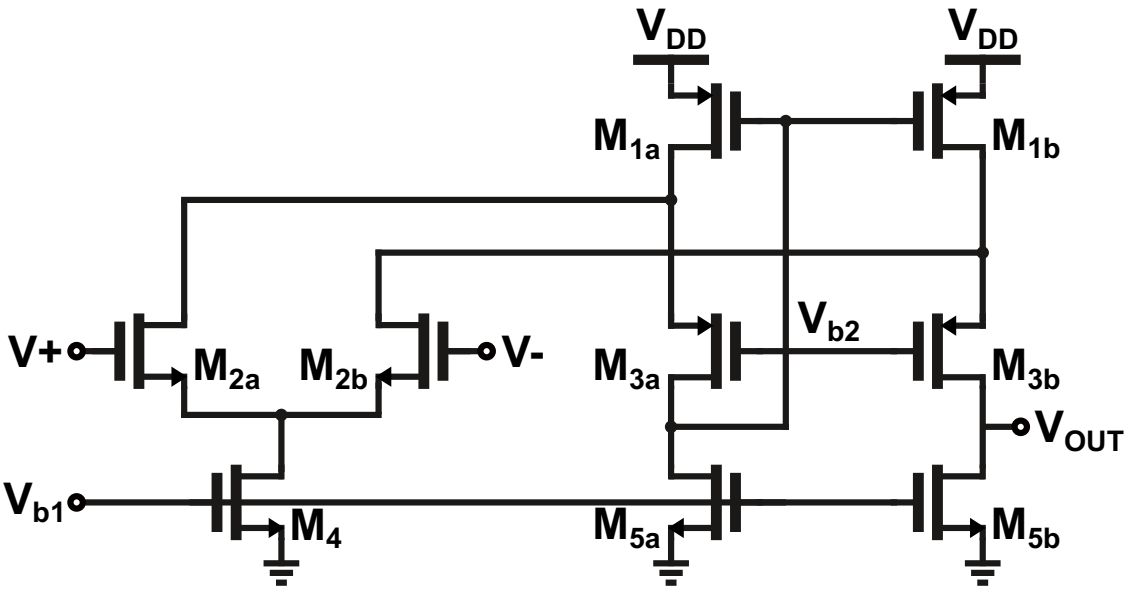


Figure 6.15: Folded cascode EA transistor level diagram.

the PSRR as it can compensate in both directions. The biasing circuit requires that the A-LDO power transistor be at minimum twice the size of the LSB power transistor of the D-LDO. With the non-linear loads, there can be situation where the A-LDO is not optimally biased. Thus, setting the A-LDO power transistor size to four times the LSB size results in better biasing accuracy and better PSRR capability. This is because the A-LDO is capable of handling more current thus can compensate for higher magnitude ripples on the input. A larger power transistor would result in increasingly larger gate capacitance reducing the performance and low power capability of the A-LDO. The implemented EA is shown in Fig. 6.15. The folded cascode design allows for low voltage operation as discussed in [13]. This design uses NMOS input transistors. This allows for slightly better performance compared to the PMOS input transistor and more importantly, allows the use of the EA without feedback resistors. When the output voltage is high, the NMOS transistor allows more current to flow between the source and drain terminal. When the output voltage is low, little current flows in M_{2a} transistor while current will always flow in the V^+ input connected to V_{Ref}. Thus the EA is capable of functioning at the desired voltage range of the design. The maximum

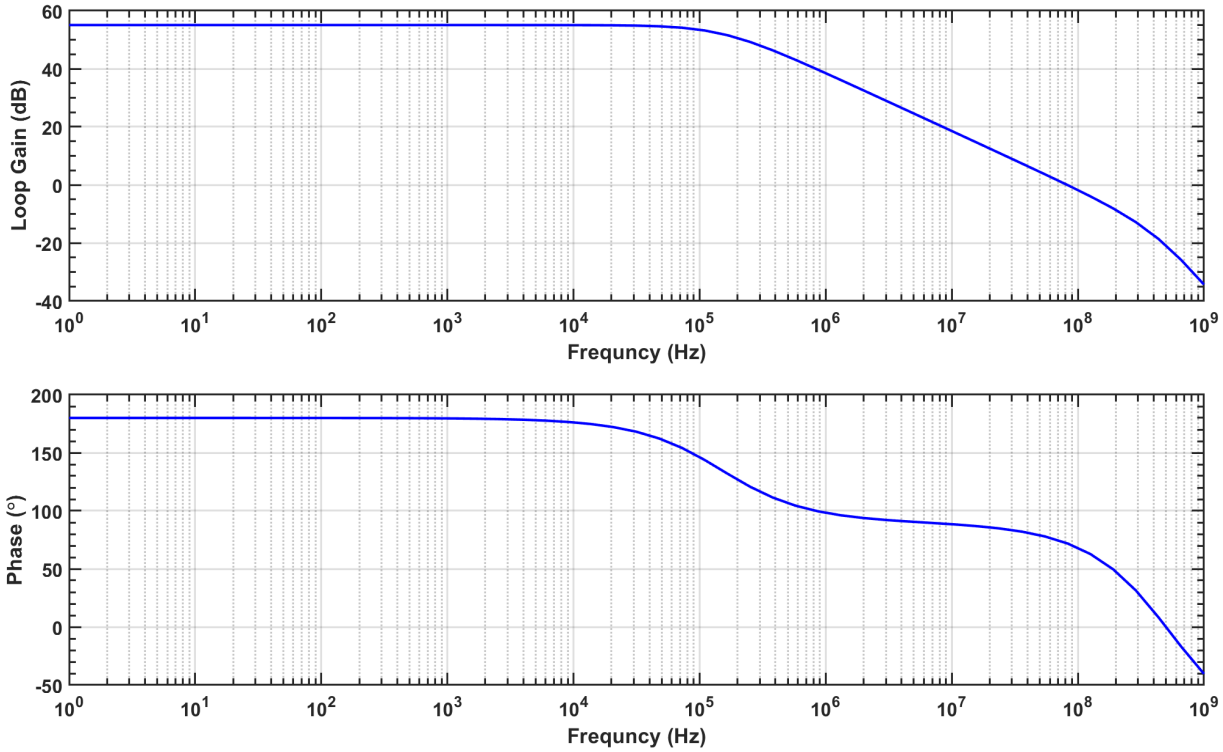


Figure 6.16: Analog loop bode plot at V_dd = 1.8 V TT, 27C° and V_{DO} = 600 mV, I_L = 12 mA.

V_{Ref} voltage allowed to maintain the input transistor in saturation is defined as:

$$Vref < V_{ds_4} + V_{ds_2} + V_{th} \tag{6.9}$$

For this design, V_{ds_4} and V_{ds_2} are large enough to push the NMOS to the saturation for the desired V_{Ref} of this design thus not requiring feedback resistors. This reduces the quiescent current consumption compared to when feedback resistors are used. The stability of the A-LDO network can be analysed next. When the H-LDO is in operation, the A-LDO is kept at about half its total current capability. Thus to represent the stability of the A-LDO, the stability simulation is performed at half the full load of the A-LDO. The poles and zeros of the A-LDO are represented using the derived equations in Chapter 2. Fig. 6.16 shows the simulation results of the A-LDO stability. The A-LDO reaches a PM of 72.01 ° @ 82.33 MHz and an open loop gain of 55.05 dB. The results of the bode plot result in 2 poles as predicted in the initial small signal equations. A high frequency PM is achieved due to the

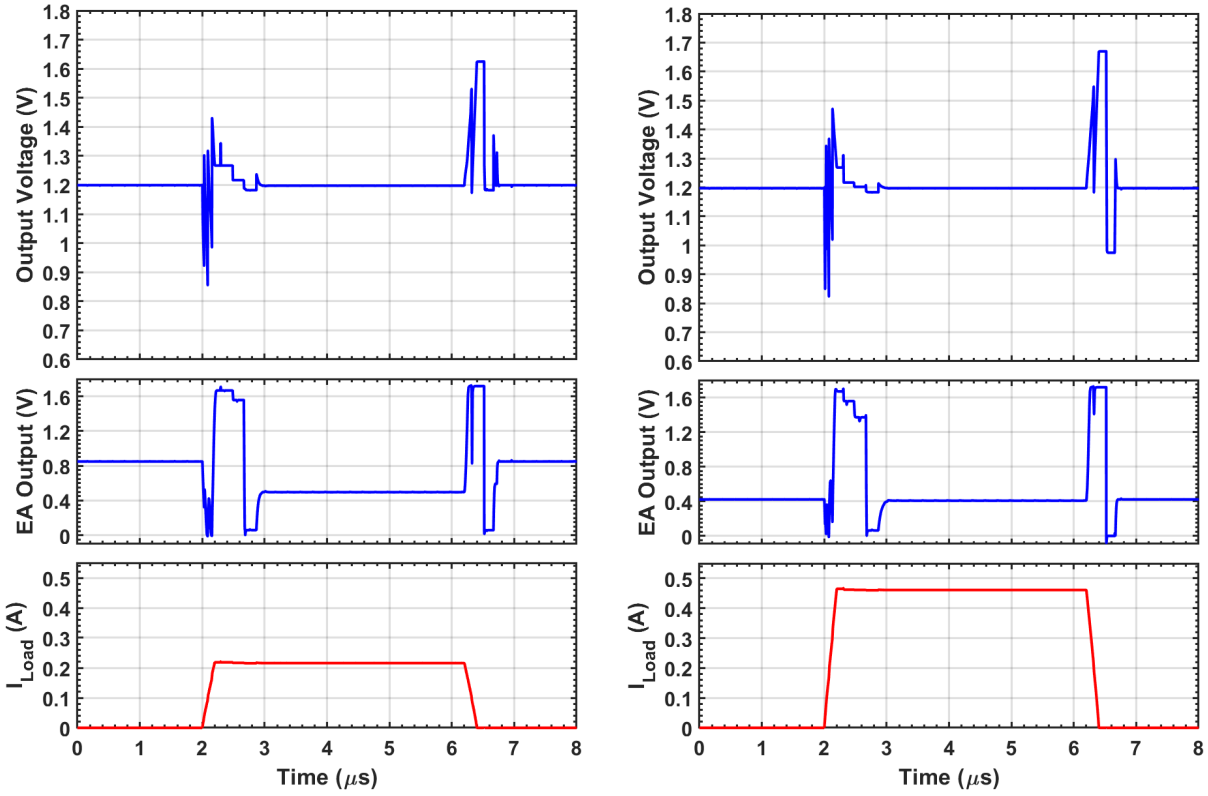


Figure 6.17: Transient simulation at a) $I_L = 25$ - 250 mA, b) $I_L = 25$ - 500 mA, test conditions of $V_dd = 1.8$ V, $V_{DO} = 600$ mV, $t_r = 200$ ns, $C_L = 1$ pF, TT, $27C°$.

small gate capacitance of the power transistor as predicted in our analysis. This results in a fast transient response while maintaining good stability and low quiescent current.

The H-LDO is designed in the TSMC 180 nm technology and is simulated using Spectre with BSIM 3.3 device models. The transient simulation is performed using the TT corner at 27 °C. Fig. 6.17 shows the transient simulation for a half load and full load step. The number of cycles to converge to the desired output is about the same in both cases at 9 cycles resulting in a settling time of about 1 μs. During the steady increase in load current, sharp voltage transitions are present. These are caused by the droop detection circuit adding a transistor to the output in an effort to maintain the desired output voltage. This is only present during the load increase. The output of the EA demonstrate the voltage from the analog circuit. It can be seen that the EA correctly compensates for the output voltage.

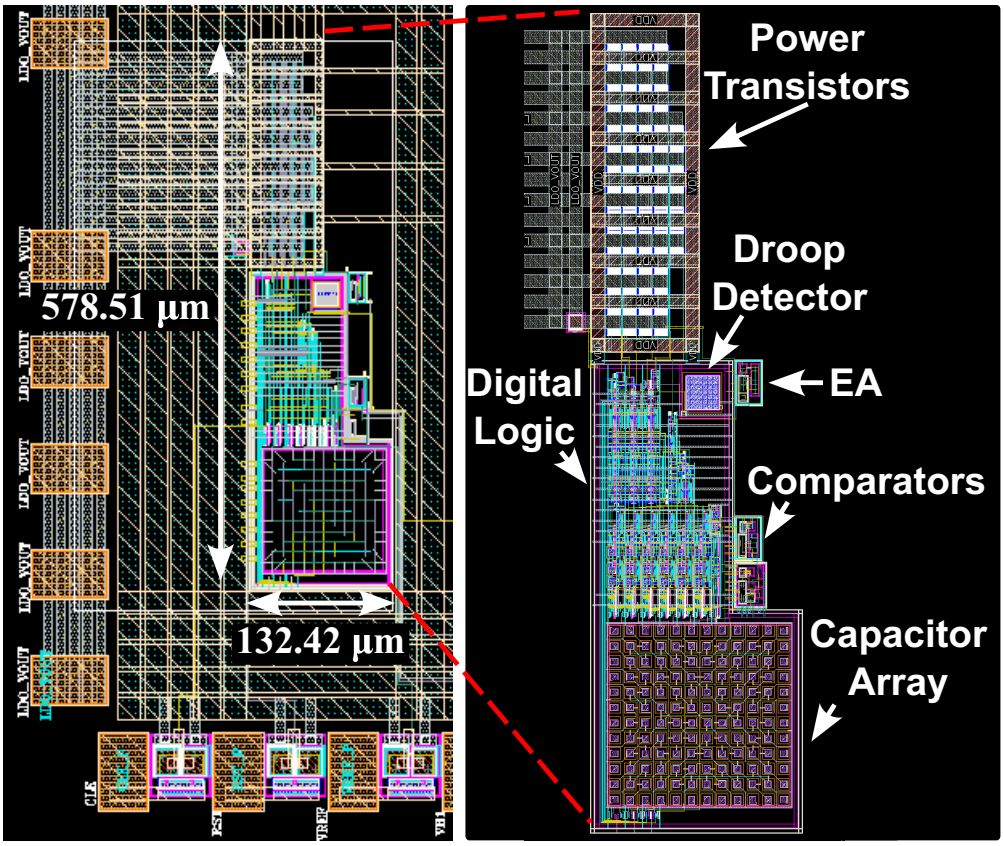


Figure 6.18: Layout of the designed H-LDO.

When the H-LDO converges to V_{Ref}, the output voltage is maintained close to half the full range ensuring that the correct biasing is achieved.

6.3 Layout

The H-LDO design is to be manufactured using the TSMC 180 nm technology using the ultra thick metal (UTM) process. This is a 1 poly 6 metal 1.8 V with MiM caps. Fig. 6.18 shows the complete layout of the design. The layout of the H-LDO consumes 0.0766 mm^2 of active area excluding the pads and power distribution. Table 6.1 show the maximum current density using the ultra thick metal where M6 has an improved current density. A similar layout to the dual loop A-LDO is used in order to obtain the proper current density where each transistor is separated in different sections in order to meet the current requirements. At

Table 6.1: Maximum current density of metals in TSMC 180 nm at 110 °C

	J_{max} (mA/μm)		J_{max} (mA/via)
M1	1	Contact	0.53
M2	1	Via12	0.28
M3	1	Via23	0.28
M4	1	Via34	0.28
M5	1	Via45	0.28
M6	9.2	Via56	0.706

full load the unit transistor must supply a maximum of 7.8 mA. Each transistor are composed of 5 fingers with a length of 9 μm each. The current from the transistors is carried to the output using 8 traces, 10 μm wide made from M2 to M5. Using (5.26) the maximum current a single trace ca handle is 84 mA @ 85 C°. The maximum number of transistors connected to a single line is 10 resulting in a maximum current of 78 mA which can be handled by the metal trace. In order to perform the charge distribution for the algorithm, a matched capacitor array must be implemented in the layout. If the capacitors don't exhibit all the same capacitance, an error is introduced to the final output level reducing the accuracy of the H-LDO. A common centroid implementation of the capacitor array is used in order to reduce the mismatch. Fig. 6.19 show a close up of the capacitor array. Dummy capacitors are used all around the array in order to assure all the capacitors within the array exhibit the same parasitic capacitance as the capacitors at the perimeter of the array. The capacitors are positioned such that all have a common point as close to the center as possible. This was not possible for single capacitors thus they are placed in the middle and array with larger capacitors interconnected around the center of the array. All the traces for inter connecting the capacitors are placed in between each capacitors and at a lower metal layer to minimize the coupling capacitance and maintaining a high level of matching.

6.4 Measurement

The completed design is sent to the foundry to get manufactured using the TSMC 180 nm technology and packaged in a DIP 40 format. The die micro graph of the A-LDO is shown

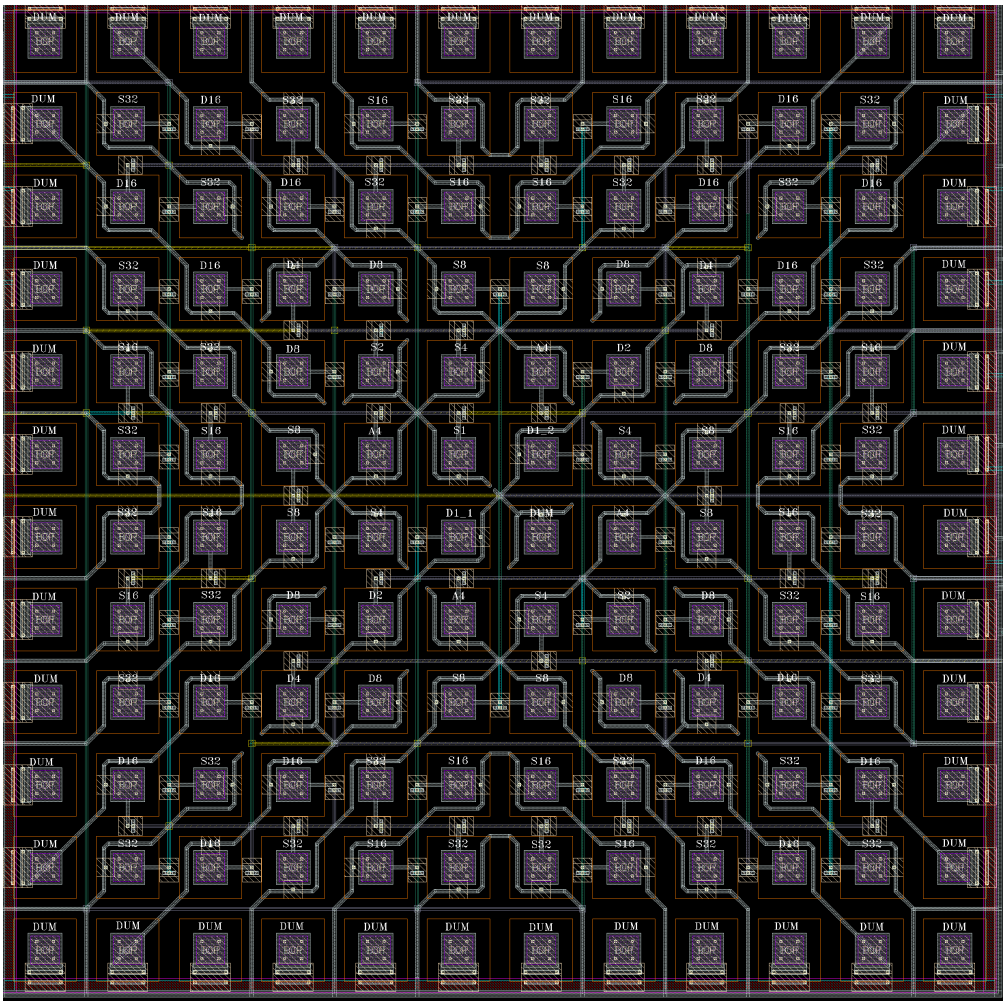


Figure 6.19: Charge distribution capacitor layout.

in Fig. 6.20. To test the performance of the H-LDO, a custom PCB is manufactured. The

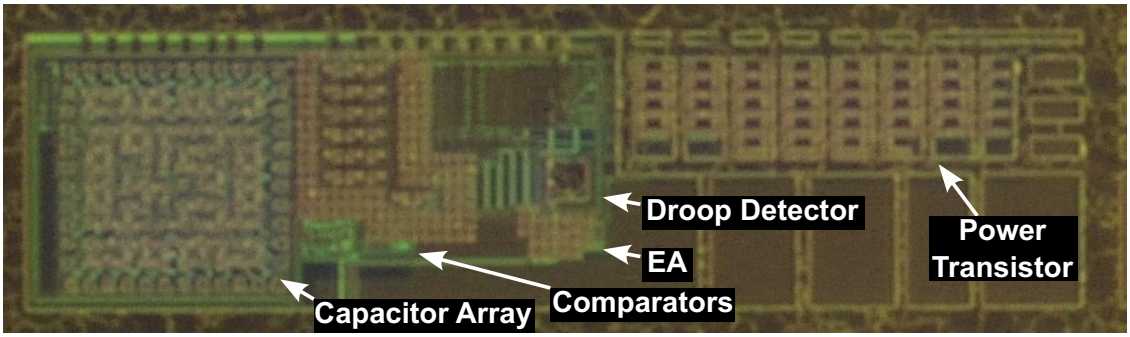


Figure 6.20: Manufactured die micro graph of the hybrid LDO regulator.

PCB contains similar functionality as the one designed for the dual loop LDO in Chapter 5. There are 3 current sources for the comparator, EA and delay cells. The input and output current is monitored using a shunt resistor coupled with a high precision amplifier. The load is applied using a current mirror and a variable resistor. A constant current is applied to I_{L1a} and is then replicated at the output of the H-LDO using 2 bjt transistors. The load is varied using the trim potentiometer RV_3. RV_2 is used to linearize the load. The base load of the H-LDO can be adjusted using the variable resistor RV_1. Fig. 6.21 show the diagram of the custom PCB. The manufactured test PCB with the DIP-40 package

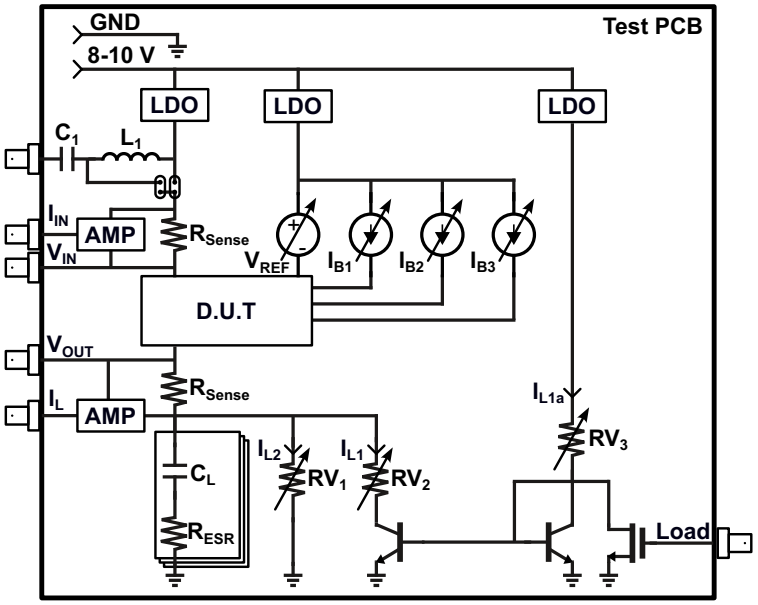


Figure 6.21: H-LDO test PCB diagram.

and all the components is shown in Fig. 6.22. Using the test PCB the load regulation is tested and shown in Fig. 6.23. A load regulation performance of 0.146 mV/mA @ 1.8 V is measured. The transient measurements are analysed next using a 10 MHz clock, a 1.8 V supply voltage and a 1.2 V output voltage. With the droop detector deactivated, the transient response of the H-LDO is analysed using a half load and full load current step. The results are presented in Fig. 6.24. The transient measurement show the fast response of the approximation algorithm where only 2 clock cycles are required at full load to return

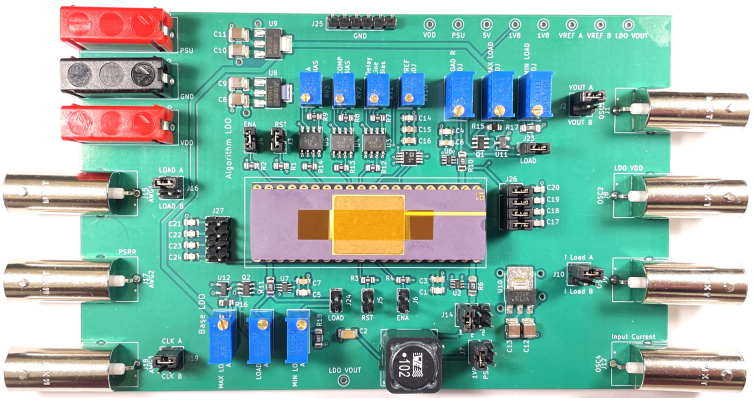


Figure 6.22: H-LDO test PCB.

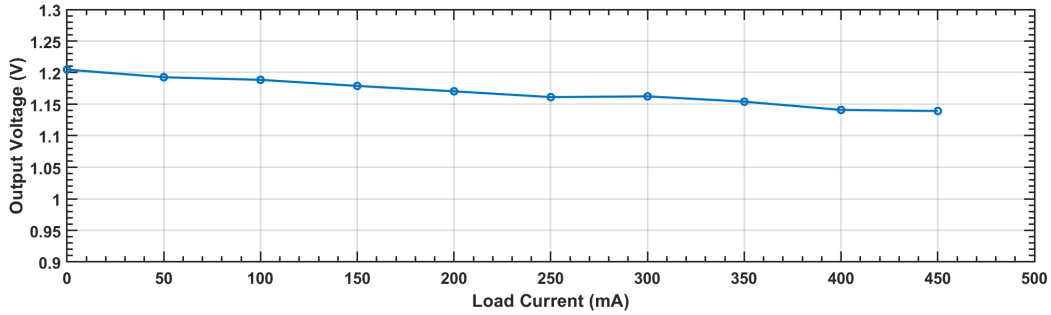


Figure 6.23: Load regulation measurements of the H-LDO.

the output to the desired voltage. On average, the transient response time is 393 ns across all the tests performed. Due to the low sampling frequency, the droop voltage is quite high where during a full load step, the output voltage is reduced to 151 mV. This shows the importance of the droop detector in the circuit. The droop detector is activated and the transient measurements taken shown in Fig. 6.25. Using the droop detector, the undershoot is fixed to 480 mV over the entire load range. The droop voltage is set by the threshold voltage of the PMOS, using a lower threshold technology would reduce the droop voltage further. The settling time using the droop detector is improved to 290 ns on average. The performance of the H-LDO is summarized in Table 6.2 along with other state of the art comparison.

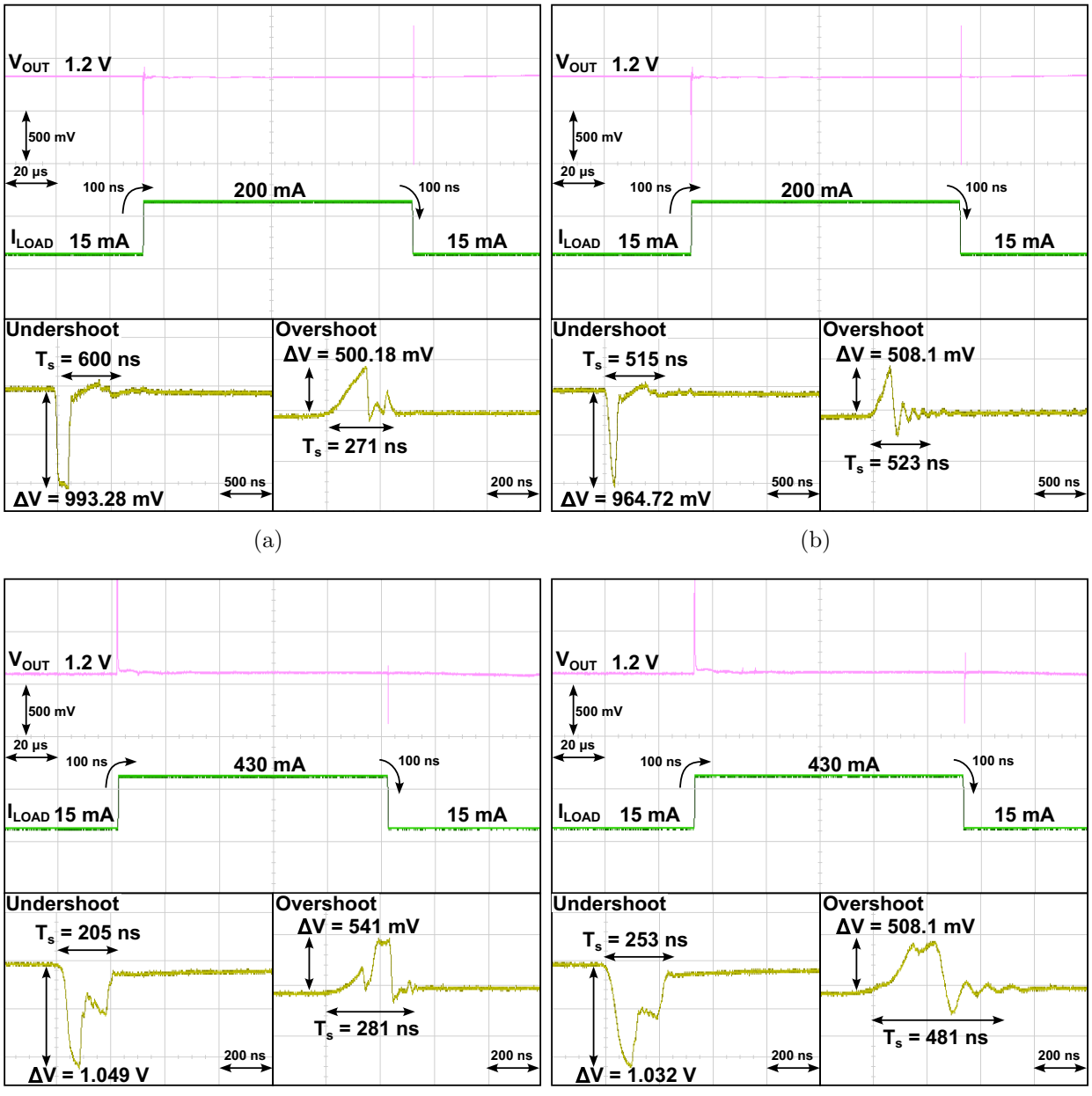
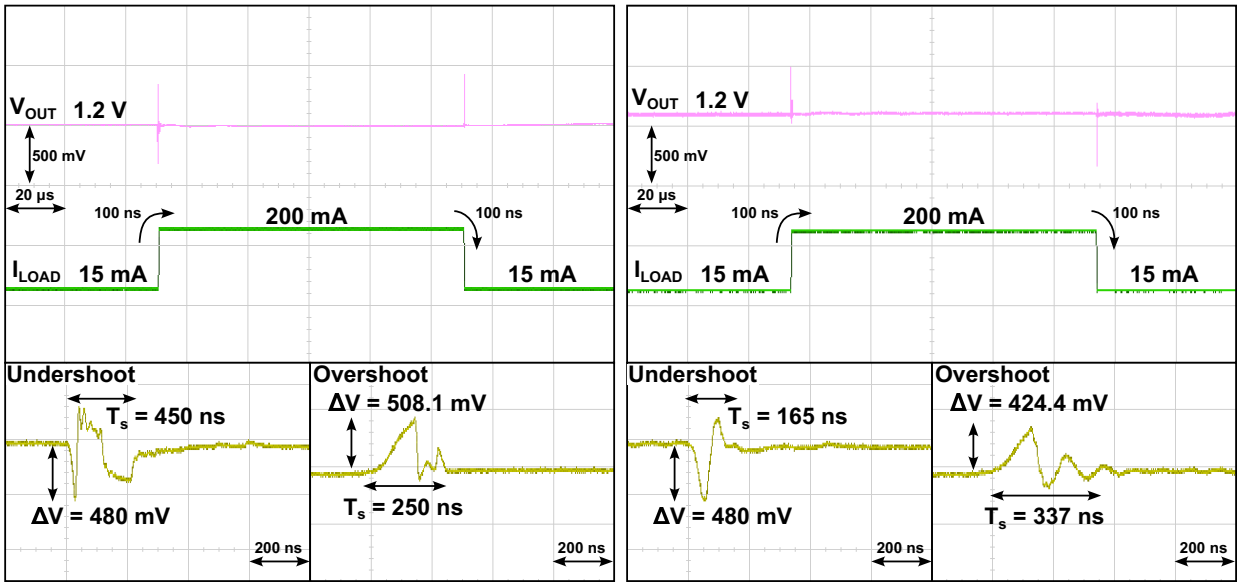
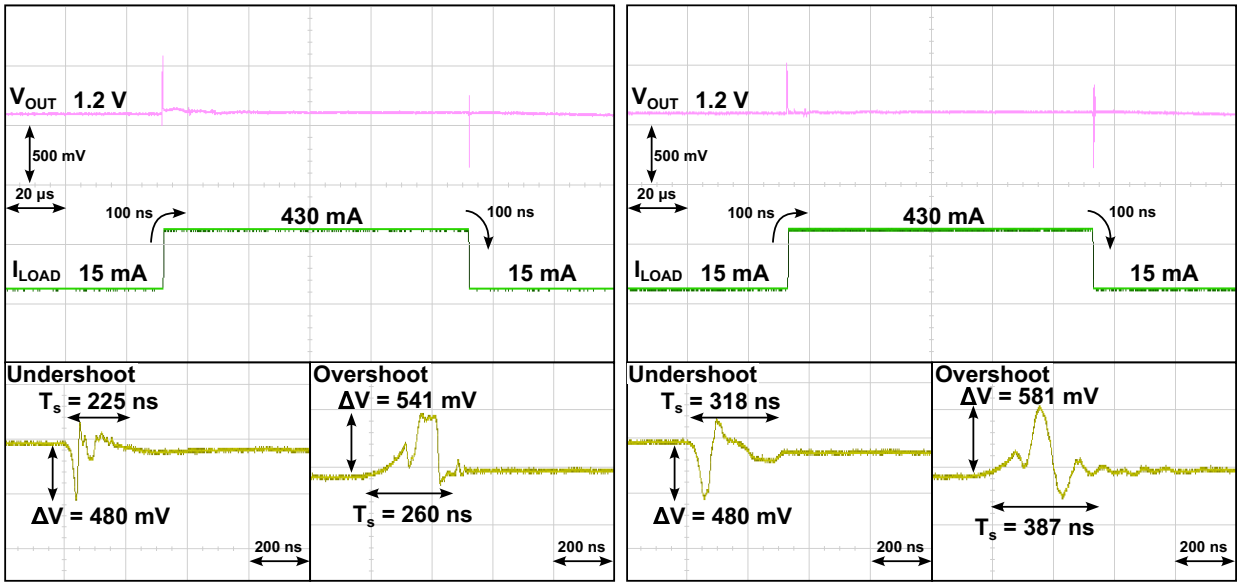


Figure 6.24: Measured transient results without droop detector at a) I_L = 0 - 200 mA, C_L = 0 pF b) I_L = 0 - 200 mA, C_L = 2 nF c) I_L = 0 - 430 mA, C_L = 0 pF d) I_L = 0 - 430 mA, C_L = 2 nF. Test conditions of V_dd = 1.8 V, 27 C° and V_{DO} = 600 mV, t_r = 100 ns.



(a)

(b)



(c)

(d)

Figure 6.25: Measured transient results with droop detector at a) I_L = 0 - 200 mA, C_L = 0 pF b) I_L = 0 - 200 mA, C_L = 2 nF c) I_L = 0 - 430 mA, C_L = 0 pF d) I_L = 0 - 430 mA, C_L = 2 nF. Test conditions of V_dd = 1.8 V, 27 C° and V_{DO} = 600 mV, t_r = 100 ns.

Table 6.2: Performance summary and comparison with state of the art designs.

	This Work	JSSC	JSSC	ISSCC	TCAS-I
Year	2024	2018	2021	2018	2023
Technology (nm)	180	65	65	28	28
V_{IN} (V)	1.8	0.5 - 1	1.2	0.4 - 0.55	0.65 - 0.85
V_{OUT} (V)	1.2	0.3 - 0.45	0.6 - 1.15	0.35 - 0.5	0.6 - 0.8
V_{DO} (mV)	300	50	50	50	50
F_s (MHz)	10	240	100	4	1
C_{LOAD} (pF)	2000	0.4	N/A	N/A	N/A
C_{TOTAL} (pF)	1	400	250	24	19.37
I_q (µA)	49	14	120	0.81	5.9
V_{Droop} (mV)	480	40	55	117	130
I_{Load} (mA)	430	2	500	20	100
Load Reg. (mV/mA)	0.146	5.6	0.03	N/A	0.6
Current Eff. (%)	99.99	99.8	99.97	99.99	99.99
T_{Edge} (ns)	100	1	100	3	1
T_{Settle} (ns)	253	0.1	0.22	9000	2.5
K	100	1	100	3	1
Area (mm^2)	0.0766	0.0023	0.36	0.0055	0.0236
FoM1 (ps)	0.00013	56.00000	0.00660	0.00569	0.00149
FoM2 (ps)	0.03218	5.60000	0.00145	51.17580	0.00371
FoM3 (mV)	5.470	0.280	1.320	0.014	0.008
FoM4	168.820	66.272	312.426	18.132	9.783

Chapter 7

Conclusion

The previous chapters discussed the design and architectures of the A-LDO, D-LDO and H-LDO including our research conducted on the topic. This chapter concludes the thesis along with some future work for our research group.

7.1 Conclusion

The architecture and design of analog, digital and hybrid LDOs were presented in Chapter 2, 3 and 4. The advantages and limitations of each design method are explored, along with some solutions from academia. Chapter 4 introduces a high transient speed, high current cap-less LDO regulator using the dual loop architecture. The amplifier's fast transient response is achieved using the high-speed current loop, while improved load and line regulation is achieved using the current loop. The post layout simulations indicated a fast transient response of 3.76 μs across a wide range of load conditions. The design is manufactured in TSMC 180 nm confirming the simulated performance. The measured load and line regulation performance of 0.0146 mA/mV and 36.36 mV/V respectively. An FoM of 0.00228 ps is achieved. This research on the dual loop LDO regulator has been published in the NEWCAS conference held in Sherbrooke QC in June 2024. Compared to other methods, the dual loop LDO demonstrated improved line and load regulation and fast transient response time. The measured FoM of the dual loop LDO indicates improved performance compared to other state of the art A-LDO regulators.

Chapter 6 demonstrated the use of a novel approximation algorithm enhancing the transient speed of low clock frequency LDO regulators. The algorithm is implemented using a charge distribution technique eliminating the need for an ADC improving the quiescent current consumption of the LDO. Theoretical analysis indicate that the algorithm is capable of improving the number of cycles to less than 5, a great improvement compared to the linear or SAR algorithms. In order to improve the performance, an EA is added improving the light load performance as well as the load and line regulation. A droop detector using a footed inverter is added in order to reduce the maximum droop voltage without increasing the current consumption of the LDO. Simulation results indicated a fast transient response as well as low droop voltage. The design is manufactured using the TSMC 180 nm technology and tested using a custom PCB board. A measured transient response of 253 ns is achieved for a full load step using only 2 clock cycle to settle to the desired output voltage. This research has been published in the MWSCAS conference held in Springfield Massachusetts in August 2024. Compared to conventional algorithms the developed approximation algorithm show a significant reduction in the number of clock cycles required to converge to the desired output resulting in a fast transient response ideal for low clock frequency applications.

7.2 Future Work

The approximation algorithm presented in Chapter 6 can be implemented in many applications one of which is the ADC. Ultra low voltage ADC designs may benefit from the use of this algorithm for faster convergence and lower power consumption compared to the traditional SAR and $\Delta\Sigma$ methods. Such applications for the developed algorithm still requires to be investigated.

Improvements on the H-LDO design must also be investigated where a dynamic approximation method could be used to improve the transient response further. Currently the implemented algorithm rounds to the nearest bit, a finer approximations can result in better transient response and improved performance. The H-LDO could also benifit from a fully

integrated system where the clock generator, reference and protection is all integrated on the IC resulting in a complete design.

Some publications based on our research has been published with more publications in progress. Table 7.1 show our previous publications on LDO's as well as the current and in progress paper on the design.

Table 7.1: LDO paper publications

Status	Title · Author List · Confrence / Journal
Published [7]	A High-Speed Capacitor Less LDO with Multi-Loop Fast Feedback and Bandwidth Enhancement Control Fu, Ximing and Zhou, Yushi and Leduc, Pierre and El-Sankary, Kamal 2023 IEEE International Symposium on Circuits and Systems (ISCAS)
Published [51]	A Dual Loop Current Mode Feedback Capacitor Less LDO for High Current Applications Leduc, Pierre and Fu, Ximing and Zhou, Yushi and El-Sankary, Kamal 2024 22nd IEEE Interregional NEWCAS Conference (NEWCAS)
Published [52]	A 3.04-fs FoM Hybrid LDO Regulator with Fast Transient Algorithm and Wide Load Range Leduc, Pierre and Fu, Ximing and Zhou, Yushi 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS)
Under Review	A 100 mA Fast-Transient Capacitor Less Low-Dropout Regulator with Multi-Path Piecewise Speed Enhancement Achieving 99.62 % Efficiency Fu, Ximing and Zhou, Yushi and Leduc, Pierre and El-Sankary, Kamal Analog Integrated Circuits and Signal Processing
In Progress	A 500 mA Dual Loop LDO with Current Feedback and Wide Load Capability Acheiving sub 0.01 ps FoM Leduc, Pierre and Fu, Ximing and Zhou, Yushi and El-Sankary, Kamal IEEE Transactions on Circuits and Systems II: Express Briefs (TCASII)
In Progress	A Hybrid LDO Using a Novel Approximation Algorithm for High Speed Low Frequncy Apllications Leduc, Pierre and Fu, Ximing and Zhou, Yushi IEEE Transactions on Circuits and Systems I: Regular Papers (TCASI)

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