Three-Phase Transformerless Series-Connected Current Source Inverter With Capacitor Voltage Balancing Control Method

By

Kechen Wu

Submitted in partial fulfillment of the requirements

for the degree of Master of Science in

Electrical and Computer Engineering

Lakehead University

Thunder Bay, Ontario

August 2026

Abstract

In medium-voltage and high-power applications, the series-connected current source converter (SC-CSC) is a good candidate. However, most existing series-connected CSCs require transformers. Recently, a single-phase transformerless series-connected current source converter has been proposed. It eliminates the bulky and costly transformer, achieving lower cost and smaller system size. In this work, the three-phase version of this inverter is proposed and investigated. Since the original single-phase topology cannot be directly extended to the three-phase system, the original topology is modified to eliminate circulating currents. In practical implementations, mismatches in capacitors can destroy the inherent voltage balance of the inverter. To address this issue, a voltage balancing control strategy is introduced to regulate the capacitor voltages under parameter mismatch conditions. The proposed control method restores the capacitor voltage balance without modifying the topology or affecting its current balancing characteristics. The operation principles of the proposed three-phase inverter and the effectiveness of its capacitor voltage balancing strategy are validated through MATLAB/Simulink simulation results.

Acknowledgments

First and foremost, I would like to express my sincere gratitude to my supervisor, Dr. Qiang Wei, for his patient guidance and invaluable support throughout my academic studies, as well as for the sincere advice he has offered me in my personal life.

I would also like to extend my thanks to my team members. I am especially grateful to Kaiwen, whose help made it possible for me to pursue this valuable learning opportunity, and to Zhiming for his companionship, support, and valuable advice throughout my studies. I would also like to thank Javad, Erfan, Milad, and other friends, whose help, advice, and encouragement have been equally important throughout this journey.

Last but not least, I would like to express my deepest gratitude to my parents. Their selfless support made it possible for me to pursue my studies abroad, and their patience, encouragement, and unwavering support have accompanied me throughout this entire journey.

Table of Contents

Abstract ii

Acknowledgments iii

List of Figures vi

List of Tables viii

List of Symbols ix

List of Abbreviations x

Chapter 1 Introduction 1

1.1 Overview of CSC 2

1.2 Configuration of the Series-Connected Current Source Converters System 4

1.2.1 Series-Connected Current Source Converter with Input Transformer ..5

1.2.2 Series-Connected Current Source Converter with Output Transformer 8

1.3 Transformerless Series-Connected Current Source Converter 11

1.4 Thesis Objectives 13

Chapter 2 Capacitor Voltage Balancing Control 14

2.1 Proposed Three-Phase Transformerless SC-CSI 14

2.1.1 Operation Principle 16

2.1.2 Modulation Scheme 18

2.1.3 Passive Element Design 19

2.2 Configuration of the Proposed Capacitor Voltage Balancing Scheme. 22

2.2.1 Voltage Unbalance Analysis 22

2.2.2 Capacitor Voltage Balancing Control Scheme 23

2.3 Simulation Result 28

2.4 Summary 32

Chapter 3 Circulating Current Elimination 33

3.1 Topology Modification for Circulating Current Elimination 33

3.2 Circulating Current Path Analysis Under Normal Operation 36

3.3 Simulation Result 38

3.4 Summary 43

Chapter 4 Conclusions 44

4.1 Contributions and Conclusions 44

4.2 Future Work 45

Reference 46

List of Figures

Fig. 1-1 A conventional two-level CSC……..…..2

Fig. 1-2 A multilevel CSC ……..3

Fig. 1-3 A parallel-connected CSC…….4

Fig. 1-4 Configuration of a SC-CSC system……...5

Fig. 1-5 SC-CSC with input transformer and diode rectifier……..7

Fig. 1-6 SC-CSC with input transformer and AFE rectifier……8

Fig. 1-7 SC-CSC with output multi-winding transformer……..9

Fig. 1-8 SC-CSC with output phase-shifting transformer……...…..11

Fig. 1-9 Single-phase transformerless SC-CSI…….12

Fig. 2-1 Proposed three-phase transformerless SC-CSI……14

Fig. 2-2 Charging mode of proposed three-phase CSI…….16

Fig. 2-3 Discharging mode of proposed three-phase CSI…….17

Fig. 2-4 Freewheeling mode of proposed three-phase CSI……..18

Fig. 2-5 Gating signal of the proposed converter……..19

Fig. 2-6 V_{Ldc} in a cycle……...20

Fig. 2-7 Simplified circuit of the CSI for filter design…….……21

Fig. 2-8 Overall control block diagram…….22

Fig. 2-9 Principle of capacitor voltage balancing with dc-link current constraint……25

Fig. 2-10 Control performance of capacitor voltage (a) phase a, (b) phase b, (c) phase c……27

Fig. 2-11 Control performance of output voltage……..29

Fig. 2-12 Control performance of output current……..……29

Fig. 2-13 Control performance of I_{dcn} in phase a (a), phase b (b), and phase c (c)…..32

Fig. 3-1 Direct three-phase extension of the single-phase SC-CSI…….…….34

Fig. 3-2 Circulating current path in the direct three-phase extension…….….36

Fig. 3-3 Representative switching-state combination for circulating current path analys is……..…….37

Fig. 3-4 Comparison of I_{wn} before and after adding S_3…….....39

Fig. 3-5 I_{dcn} and V_{cn} (without additional switch S_3) …….……..…40

Fig. 3-6 I_{dcn} and V_{cn} (after applying S_3) ……..…40

Fig. 3-7 I_{dcn}, V_{Ldcn}, V_{cn} (before introducing inductor mismatch)…….…..….41

Fig. 3-8 I_{dc}, V_{Ldcn}, V_{cn} (after introducing inductor mismatch)…….……..42

List of Tables

Table 2-1 System parameters……...…14

Table 2-2 Simulation parameters of passive components…….…...25

List of Symbols

Symbol	Meaning
C_f	filter capacitor
D	duty cycle
f_{sw}	switching frequency
I_{dc}	DC current
i_L	inductor current
i_w	PWM output current
i_s	output sinusoidal current
L_{dc}	DC inductor
L_f	load inductor
m_a	modulation index
R	load resistor
S_1-S_3	switches
Δt	dwell times
V_{in}	input voltage
V_{L_max}	maximum voltage across the inductor

List of Abbreviations

Abbreviation	Meaning
CSI	current source inverter
CSC	current source converter
SC-CSC	series-connected current source converter
SC-CSI	series-connected current source inverter
GCT	gate-commutated thyristor
GTO	gate turn-off thyristor
IGBT	insulated gate bipolar transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
MV	medium voltage
PR	proportional resonant
QPR	quasi-proportional resonant
PV	photovoltaic
KCL	kirchhoff's current law
PWM	pulse width modulation
SPWM	sinusoidal pulse width modulation
SCR	silicon-controlled rectifier
SGCT	synchronous gate-commutated thyristor
THD	total harmonic distortion

Chapter 1 Introduction

High power conversion systems are increasingly demanded in medium-voltage industrial drives, renewable energy generation, and dc transmission systems [1]. Commercial products from companies such as ABB and Rockwell Automation show that medium-voltage drive systems can cover power ratings from several hundred kilowatts to tens or even hundreds of megawatts [2][3]. In addition, medium-voltage converter technologies have also been developed for large renewable energy systems and dc transmission applications, such as ABB's PCS6000 wind converter [4] and Siemens Energy's MVDC PLUS system [5]. Therefore, compact, efficient, and reliable high-power converter topologies are becoming increasingly important.

Current source converters (CSCs) are attractive candidates for high-power conversion systems because of their inherent short-circuit protection and motor-friendly output waveforms. Existing CSC topologies can be generally classified into conventional CSCs [6]-[8], multilevel CSCs [9]-[13], parallel-connected CSCs [14]-[16], and series-connected CSCs (SC-CSCs) [17]-[25]. Among them, SC-CSC is a promising candidate for medium-/high-voltage and high-power applications.

However, existing SC-CSC topologies usually require transformers either at the input or output side. These transformers provide independent current paths for individual CSC modules and help achieve voltage boosting or isolation. Nevertheless, the use of transformers increases the system size, weight, cost, and complexity, which increases the cost and size of the system. To address this issue, recently, a transformerless SC-CSC has been proposed [26]. By eliminating the bulky transformers, transformerless SC-CSC can reduce the system size while also having current and voltage balancing capability.

At present, most studies on transformerless SC-CSC topologies focus on single-phase systems. Therefore, this thesis investigates a three-phase transformerless SC-CSC. However, parameter mismatch in the converter may cause capacitor voltage imbalance. To address this issue, a capacitor voltage balancing control method is proposed. In addition, the interphase circulating current issue of the three-phase topology is analyzed.

This chapter introduces the existing SC-CSCs, including SC-CSCs with input transformers and SC-CSCs with output transformers. Then, the transformerless SC-CSC topology is introduced. In addition, the dissertation objectives are proposed.

1.1 Overview of CSC

Existing CSC topologies can be generally classified into conventional CSCs, multilevel CSCs, parallel-connected CSCs, and series-connected CSCs.

Fig. 1-1 shows a conventional two-level CSC. The conventional CSC has a simple structure and features inherent short-circuit protection, controllable dc-link current, and low dv/dt output waveforms [1]. However, the voltage and current ratings of a single conventional CSC are limited by the ratings of semiconductor devices and passive components.

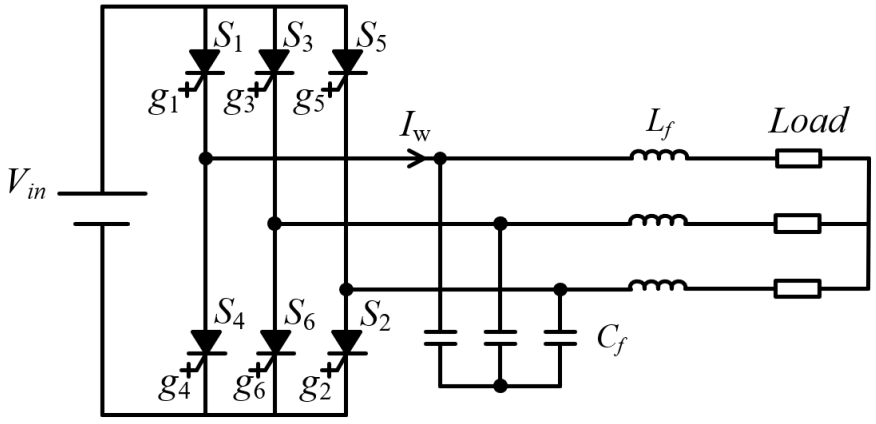

Fig. 1-1 A conventional two-level CSC.

To improve the output waveform quality, multilevel CSCs have been proposed. Fig. 1-2 shows an example of a multilevel current source inverter (CSI) in the literature [9]. By generating more output current levels, multilevel CSCs can reduce output current harmonics, current slope, electromagnetic interference, and the required filter size [10]. Some five-level CSCs also provide buck-boost capability and inductive-current balancing capability [11], while reduced-switch five-level CSI topologies have been proposed to improve power density and reduce hardware cost [12]. Compared with the conventional CSC, the unique advantage of the multilevel CSC is its improved harmonic performance and reduced device current stress.

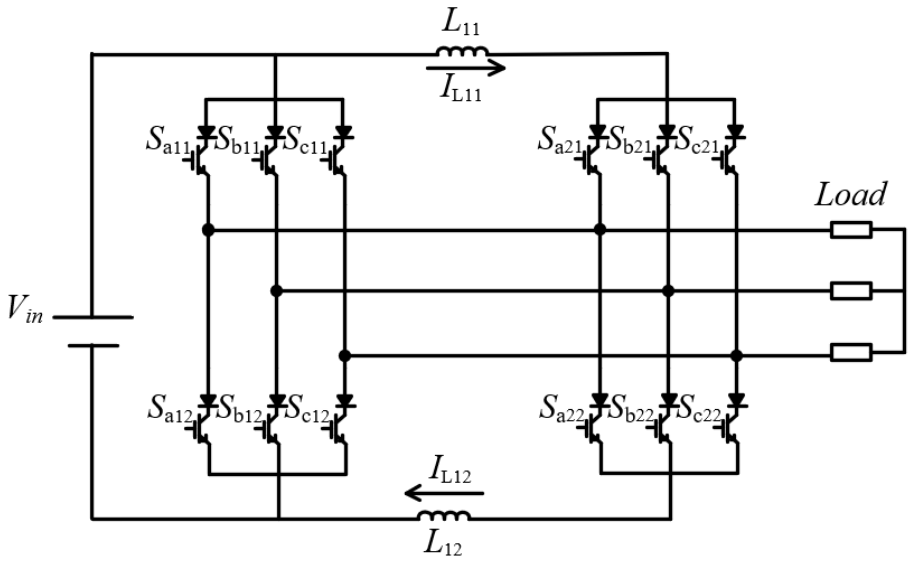

Fig. 1-2 A multilevel CSC.

Parallel-connected CSCs are usually adopted to increase the current and power rating of the converter system. Fig. 1-3 shows a parallel-connected CSC system in the paper [13]. In this structure, two or more CSC modules operate in parallel and share the output current. Therefore, the power rating of the system can be extended beyond the rating of a single CSC module. In addition, with proper interleaved modulation, the parallel-connected CSC system can generate a multilevel output current, which further improves the harmonic performance [14]. Compared with conventional and multilevel

CSCs, the unique advantage of parallel-connected CSCs is their ability to increase the current rating while maintaining modularity.

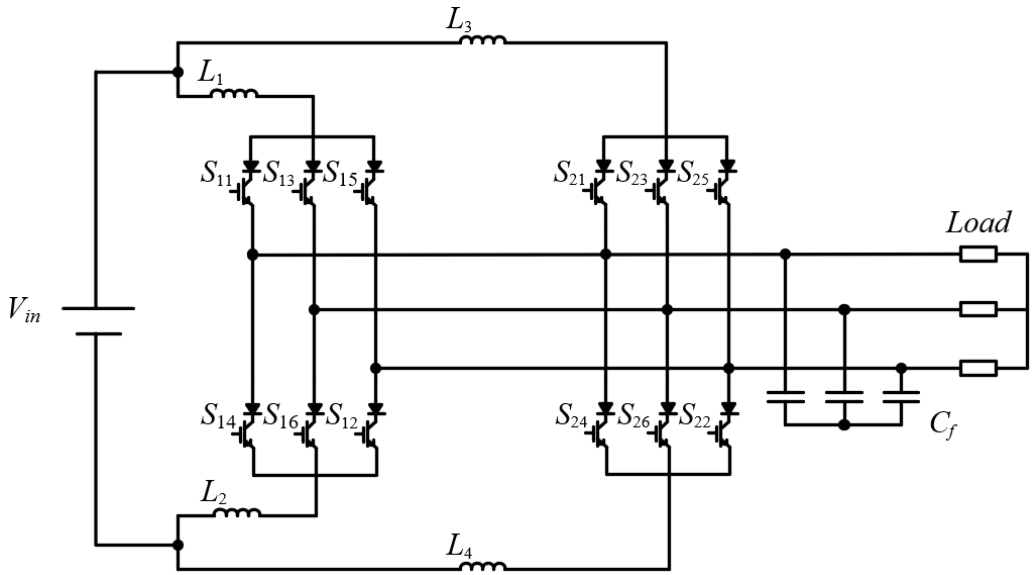

Fig. 1-3 A parallel-connected CSC.

1.2 Configuration of the Series-Connected Current Source Converters System

The SC-CSC is a modular converter structure formed by connecting multiple CSC modules in series. As shown in Fig 1-4, an SC-CSC system mainly consists of a current source, series-connected CSC modules, and the load or grid. The dc current source provides a continuous dc-link current for the whole converter system. In practical high-power applications, the dc current source can be obtained from a controlled rectifier, a diode rectifier with a front-end dc-dc stage, or other dc energy sources. The dc-link inductors are used to smooth the dc current and maintain the current-source characteristic of each converter module.

In the series-connected structure, each CSC module only withstands part of the total system voltage, while the total voltage rating of the converter is increased by the series connection.

According to the way in which independent current paths are provided for the series-connected modules, existing SC-CSC systems can be classified into transformer-based and transformerless configurations. In transformer-based SC-CSCs, transformers are usually placed either at the input side or at the output side.

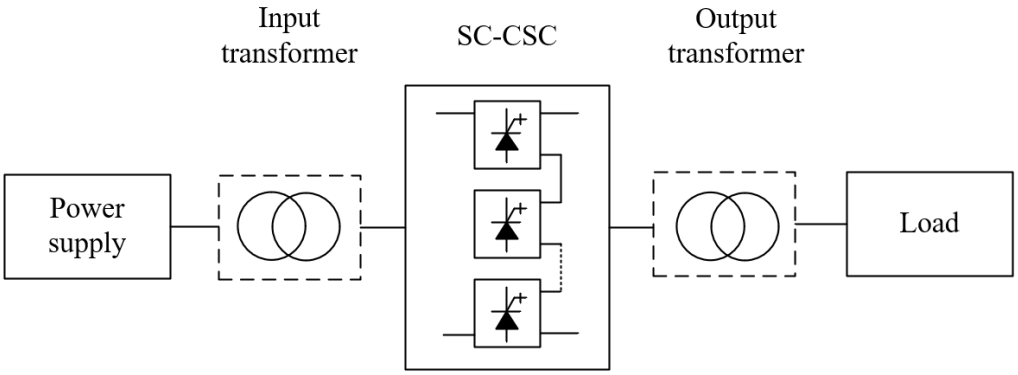

Fig. 1-4 Configuration of a SC-CSC system.

1.2.1 Series-Connected Current Source Converter with Input Transformer

In the configuration of SC-CSC with an input transformer, multiple CSC cells are connected in series at the input side to form a high-voltage phase output. Each power cell is supplied by an isolated secondary winding of the input transformer and consists of a rectifier stage, a dc-link inductor, a three-phase CSI, and an ac-side filter capacitor. The output capacitors are connected in series, which enables the output voltages of different cells to be added.

The input transformer is an essential component in this topology. It provides isolated input supplies for the individual current-source cells, which is necessary because the cell outputs are connected in series. Without isolated input supplies, the input terminals of different cells would be directly coupled, making it difficult to maintain independent cell operation and proper voltage sharing. In addition, the input transformer reduces the

voltage level from the ac mains to the required cell input voltage, allowing low-voltage semiconductor devices to be used in medium- or high-voltage applications.

Literature [19] proposes an input-transformer-based SC-CSC with diode rectifier, shown in Fig. 1-5. It consists of the phase-shifting input transformer, diode rectifiers, dc-link inductors, three-phase CSIs, and filter capacitors. When diode rectifiers are used in the power cells, the input transformer is usually designed as a phase-shifting transformer. The phase-shifted secondary windings supply different rectifier units and help cancel dominant low-order harmonics in the supply currents. For example, the phase shifts among the transformer secondary windings can reduce the 5th, 7th, 11th, and 13th harmonics generated by the rectifier stage [20]. So the input transformer can also make some harmonic components caused by the dc-link current oscillation circulate among the filters and transformer secondary windings, and therefore do not appear in the transformer primary current.

Literature [21] proposes an input-transformer-based SC-CSC with active-front-end (AFE) rectifiers, shown in Fig. 1-6. It consists of the multiwinding input transformer without phase-shifting, input filters, AFE rectifiers, dc-link inductors, three-phase CSIs, and filter capacitors.

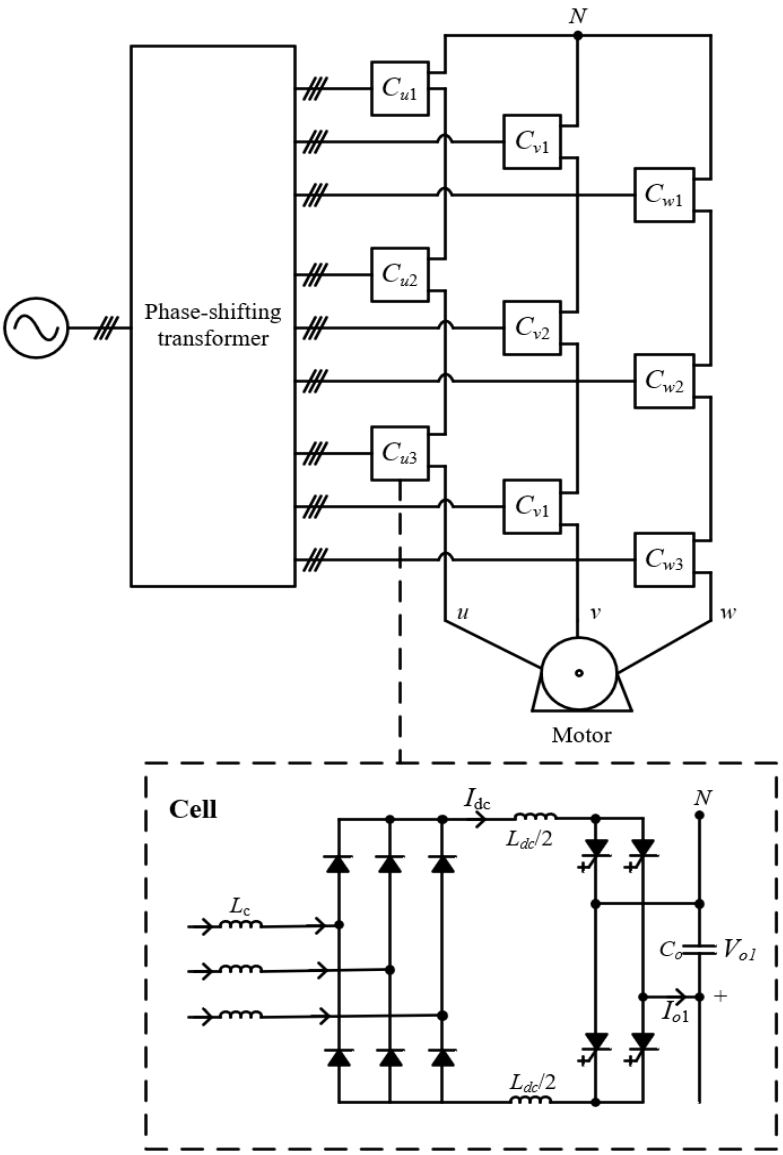

Fig. 1-5 SC-CSC with input transformer and diode rectifier.

When AFE rectifiers are used, the input transformer can be simplified because the input currents of the cells can be actively controlled. In this case, the transformer does not need to rely on complex phase-shifted secondary windings to achieve harmonic cancellation. However, an ac-side filter is normally required between the transformer secondary winding and the AFE rectifier to filter switching harmonics and shape the input current. The filter must be designed to avoid resonance and the amplification of unwanted current components.

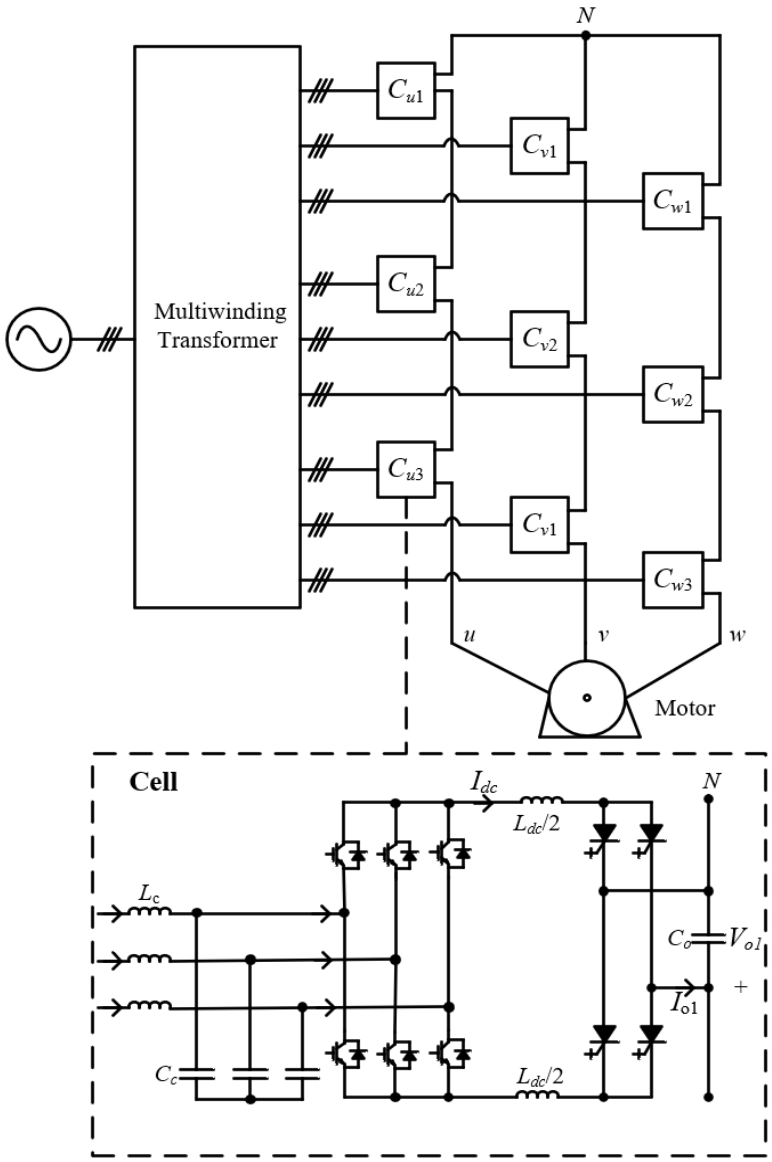

Fig. 1-6 SC-CSC with input transformer and AFE rectifier.

However, the required transformer will increase the system size, weight, cost, and design complexity. This drawback becomes more significant as the number of cells increases.

1.2.2 Series-Connected Current Source Converter with Output Transformer

Fig. 1-7 shows a proposed SC-CSC with an output transformer in the literature [20]. In this configuration, several CSI modules are connected in series at the dc side to share

the total dc-link voltage. On the ac side, the outputs of these CSI modules are connected to a common load through a multi-winding transformer. Each CSI module has its own ac-side filter capacitor, and all modules are normally controlled with the same modulation scheme to transfer power from the dc link to the ac side.

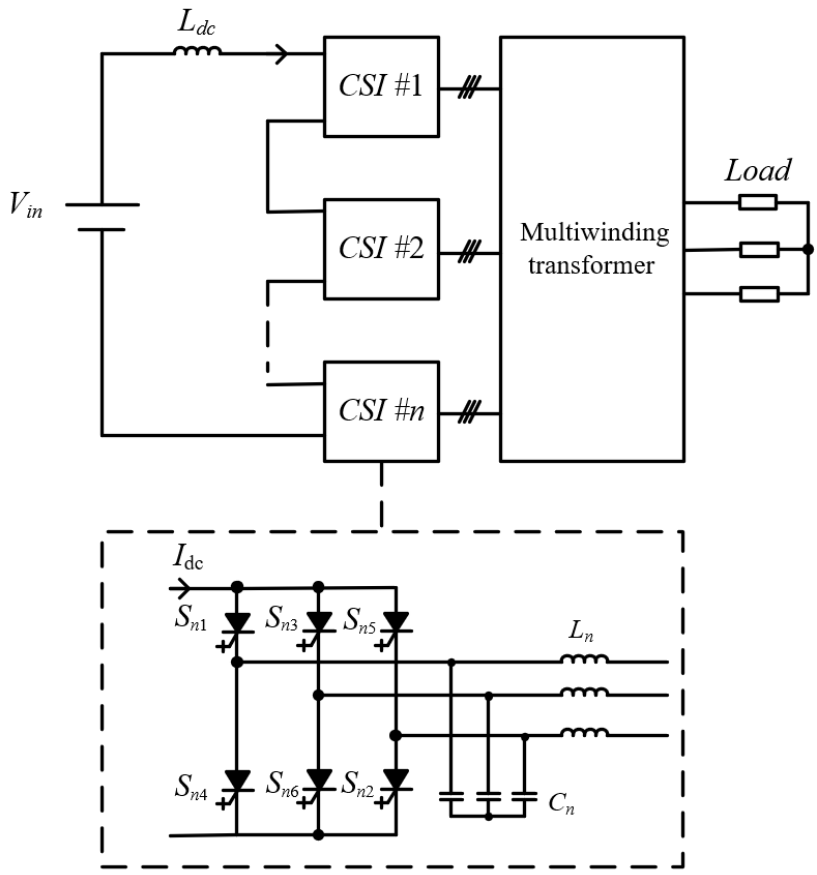

Fig. 1-7 SC-CSC with output multi-winding transformer.

The output transformer is an indispensable component in this topology. First, it provides a separate ac current path for each CSI module, which is required for the operation of series-connected CSIs. Since the characteristics of CSIs, the output current of each module must have a continuous and well-defined path. If the transformer is removed and the ac terminals of different CSI modules are directly connected together, the independent current paths of the modules cannot be guaranteed. This may cause undesired circulating currents, current distortion, and abnormal commutation among

the CSI modules. Second, the output transformer provides voltage matching or voltage step-up if required. The voltage and power rating of each transformer winding are determined by the rating of each CSI module and the number of series-connected modules. In addition, the output transformer can be implemented as a conventional multiwinding transformer or a phase-shifting transformer.

Fig. 1-8 shows a proposed SC-CSC with output transformers in the literature [22], which is a phase-shifting transformer. Different from the conventional multiwinding transformer, the phase-shifting transformer can also provide phase-shift compensation. By introducing proper phase shifts among transformer windings, the output currents of different CSI modules can be phase-shifted before the transformer and then combined after the transformer to cancel selected low-order harmonics. Therefore, phase-shifting transformers are attractive for SC-CSCs operating at low switching frequency, because they can improve output current quality and reduce the required filter size [23]. In addition, in some special SC-CSI topologies, such as less-switch SC-CSIs, the transformer winding connection is designed to cancel the phase displacement generated by the converter itself, so that the currents after the transformer remain in phase [24].

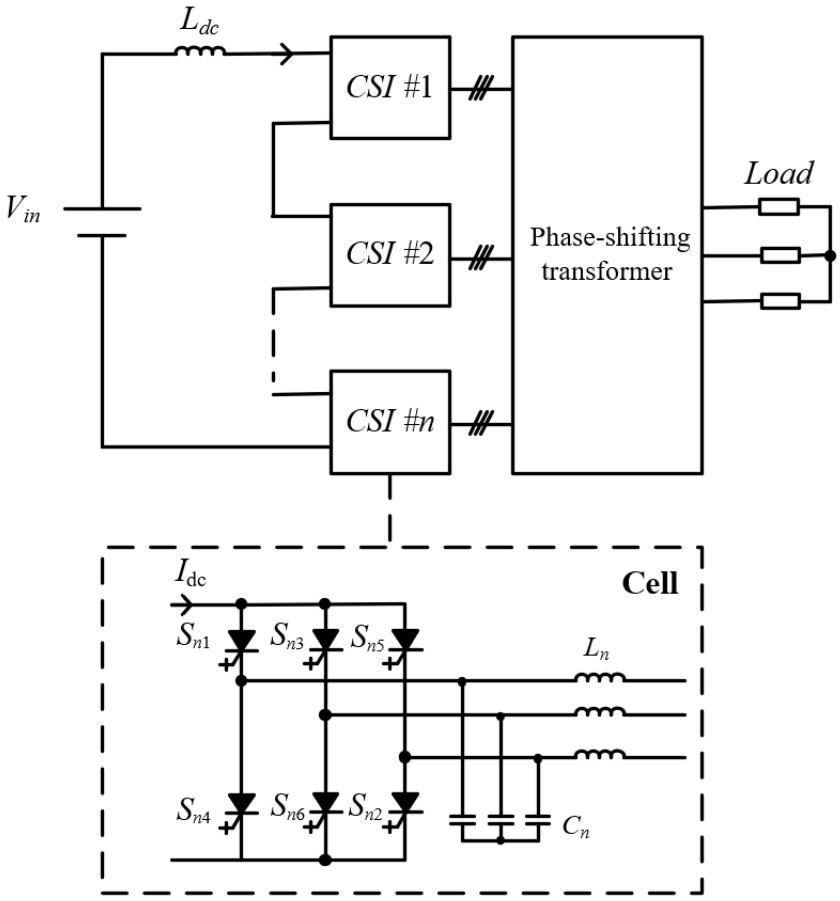

Fig. 1-8 SC-CSC with output phase-shifting transformer.

However, the output-transformer-based SC-CSC also has drawbacks. The transformer increases the size, weight, cost, and design complexity of the system.

1.3 Transformerless Series-Connected Current Source Converter

To eliminate the bulky and costly transformers used in existing SC-CSCs, a transformerless SC-CSI is proposed in the literature [26], as shown in Fig. 1-9.

Different from the input- or output-transformer-based configurations, the transformerless SC-CSC does not rely on transformers to provide independent current paths for the converter modules. Instead, each module consists of an H-bridge CSI and an additional switch. Through the designed operating modes, the dc-link inductors are

charged together and then separated to provide independent current sources for the H-bridge converter modules.

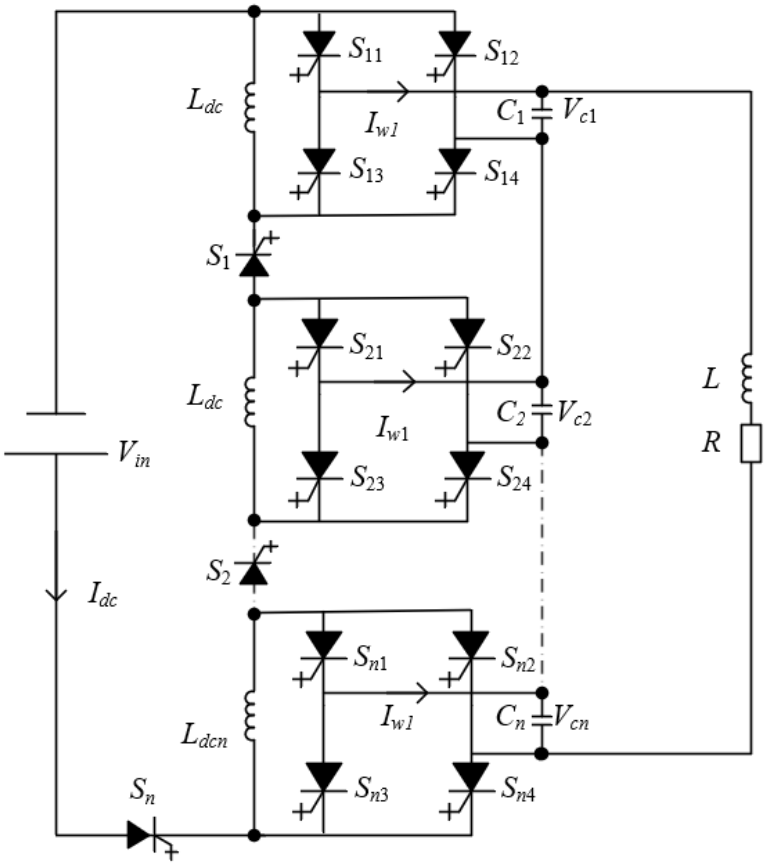

Fig. 1-9 Single-phase transformerless SC-CSI.

In addition, this transformerless SC-CSC has inherent current and voltage balancing capability. In the charging mode, the dc-link inductors of all CSI modules are connected in series, so the same current flows through all inductors and the inductor currents are forced to be equal. In the discharging mode, the switches Sn are turned off, and the dc-link inductors provide independent current sources for the H-bridge CSIs. Since all CSI modules operate synchronously, the output capacitor currents of different modules are balanced. Therefore, the output capacitor voltages are naturally balanced under ideal conditions.

1.4 Thesis Objectives

According to the above discussion, transformerless SC-CSC is a good candidate for medium-voltage and high-power applications. However, the existing transformerless SC-CSC mainly focuses on the single-phase topology. In addition, in practical implementations, parameter mismatch may destroy the inherent capacitor voltage balancing characteristic of the topology, leading to unequal voltage stress among converter modules. So, this thesis proposes and investigates a three-phase transformerless SC-CSI: the original single-phase topology is modified so that it can be applied to the three-phase system, and the main objectives of this thesis are summarized as follows:

(1) Propose a capacitor voltage balancing control strategy: In practical systems, capacitance mismatch among the series-connected capacitors can destroy the inherent voltage balancing characteristic of the converter. To solve this issue, a voltage balancing control strategy is proposed to regulate the capacitor voltages under parameter mismatch conditions. The proposed method restores capacitor voltage balance without modifying the topology or affecting the current balancing characteristic.

(2) Analyze and eliminate the circulating current issue: When the original single-phase transformerless SC-CSC is directly extended to the three-phase system, circulating currents may appear among different phases. The circulating current path and its influence on the converter operation are analyzed. Based on the analysis, the topology is modified to eliminate the circulating current.

Chapter 2 Capacitor Voltage Balancing Control

This chapter investigates the capacitor voltage unbalance issue and the corresponding balancing control method for the proposed three-phase transformerless SC-CSI, which first introduces the configuration, operation principle, modulation scheme, and passive element design of the proposed converter. Then, the capacitor voltage unbalance mechanism caused by capacitance mismatch is analyzed. Based on the analysis, a QPR-based individual cell control scheme is proposed to restore the capacitor voltage balance. Finally, simulation results are provided to verify the effectiveness of the proposed control method.

2.1 Proposed Three-Phase Transformerless SC-CSI

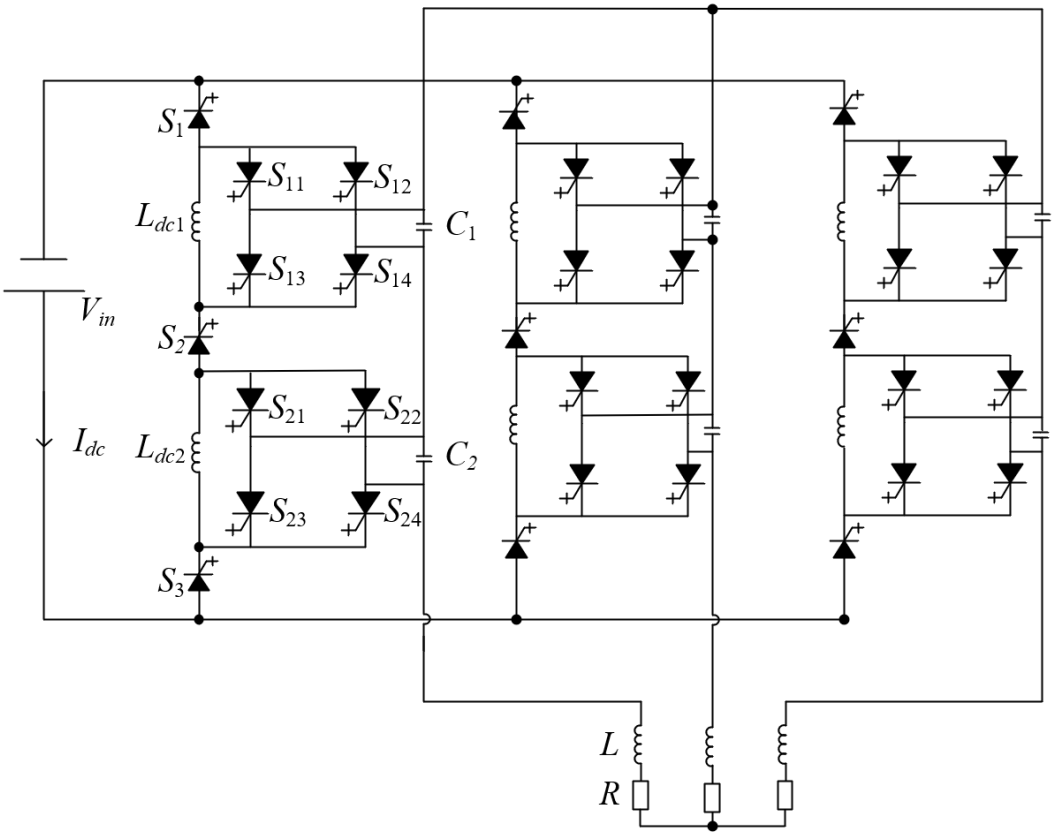

Fig. 2-1 Proposed three-phase transformerless SC-CSI.

The proposed three-phase transformerless SC-CSI is shown in Fig. 2-1, which was developed based on the single-phase version. Each phase consists of n CSI cells connected in series and n+1 series switches. In this thesis, 2 units is taken as an example. Each CSI cell includes a dc-link inductor, an H-bridge current source inverter, and an ac-side capacitor. The dc-link inductor is used to store energy and provide a continuous current source for the H-bridge, while the ac-side capacitor is used for filtering, energy transfer, and freewheeling operation. The three phases share the same dc source and generate the required three-phase ac output voltage through the series connection of the ac-side capacitors.

Compared with the original single-phase topology, the proposed three-phase topology introduces one additional switch S_3 in each phase. This additional switch is used to block the undesired interphase current path caused by the direct three-phase extension of the single-phase topology. The details will be discussed in chapter3.

Since the proposed converter is a current-source-based topology, the switching devices should be able to properly control the current path and block reverse voltage. Therefore, reverse-blocking devices are required, such as GTOs, IGCTs, and reverse-blocking IGBTs. A case study is provided to design the system parameters of the proposed three-phase transformerless SC-CSI. The system parameters used in the study are presented in Table 2-1.

Table 2-1 System parameters

Item	Parameter
Rated power	3 MVA
Rated voltage V_{LL}	4160 V
Fundamental frequency	60 Hz
Number of cells per phase	2

The rated line-to-line voltage is selected as 4160 V, which is a commonly used medium-voltage level in industrial motor drive systems. Commercial medium-voltage drives, such as the Rockwell Automation PowerFlex 7000, provide 4.16 kV drive configurations for synchronous and induction motor applications.

The rated apparent power of the studied system is selected as 3 MVA. The switching frequency is selected as 4320 Hz in this thesis, which should be carefully selected because it directly affects both harmonic performance and switching losses. A higher switching frequency can reduce current ripple and improve output waveform quality, but it also increases semiconductor switching losses and thermal stress.

2.1.1 Operation Principle

The operation of the proposed inverter can be divided into three modes: charging mode, discharging mode, and freewheeling mode.

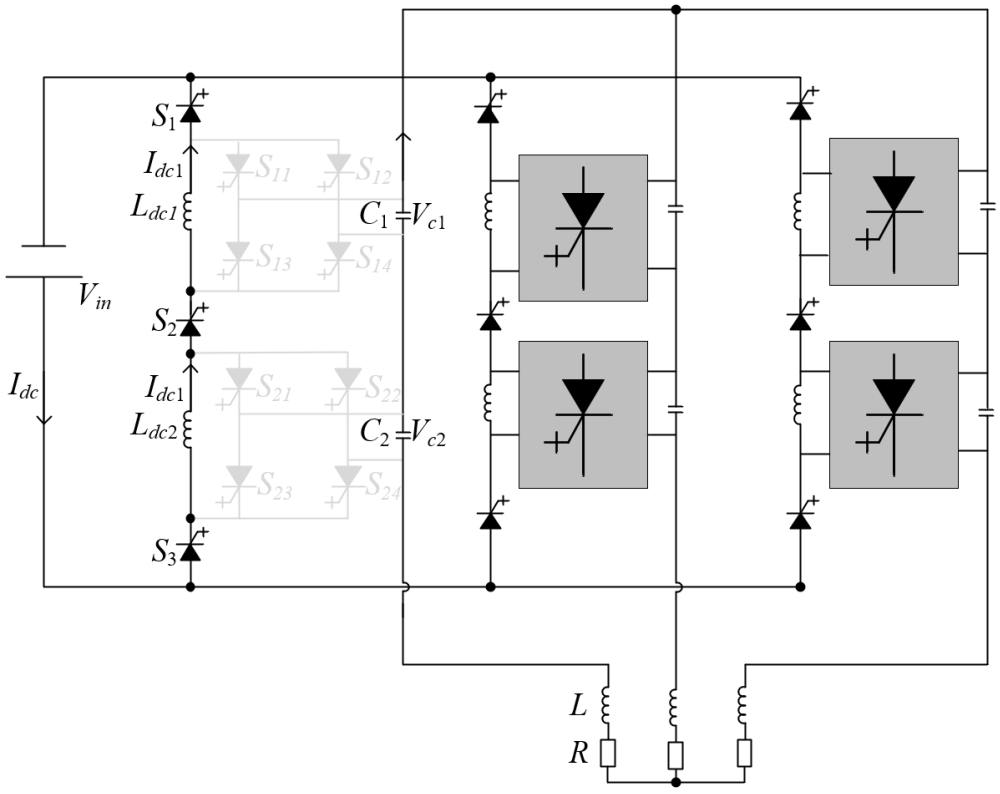

Fig. 2-2 Charging mode of the proposed three-phase CSI.

As shown in Fig. 2-2, in the charging mode, the series switches S_1 to S_3 in one phase are turned on simultaneously. Under this condition, the dc-link inductors of all CSI cells in the same phase are connected in series and are charged by the common dc source.

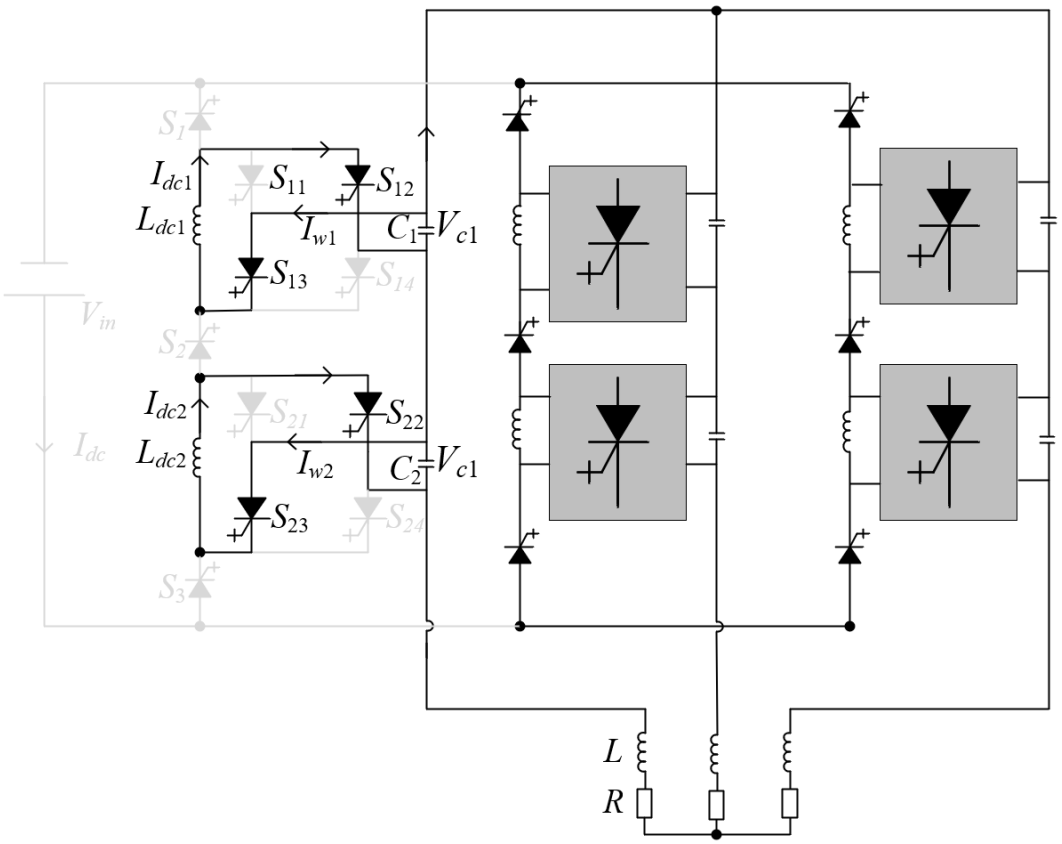

Fig. 2-3 Discharging mode of proposed three-phase CSI.

As shown in Fig. 2-3, in the discharging mode, the stored energy in the dc-link inductors is transferred to the ac-side capacitors and the load; the switch pair S_{11} and S_{14} or switch pair S_{12} and S_{13} in each H-bridge is turned on. In this mode, the dc-link inductors act as current sources, and the ac-side capacitors of different cells are connected in series to establish the required output voltage.

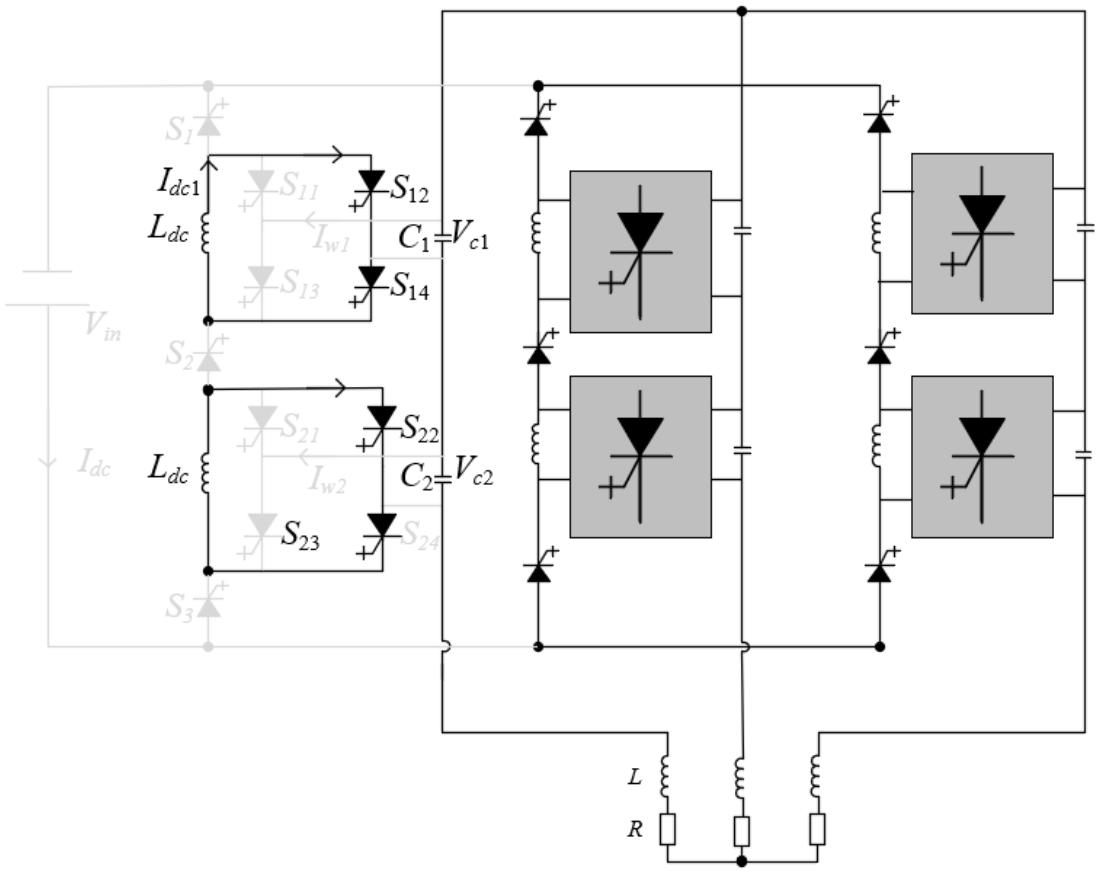

Fig. 2-4 Freewheeling mode of proposed three-phase CSI.

As shown in Fig. 2-4, in the freewheeling mode, either switch pair S_{11} and S_{13} or switch pair S_{12} and S_{14} in the H-bridge is turned on. The dc-link inductor current circulates inside the H-bridge cell. This mode provides a freewheeling path for the inductor current and maintains the current continuity of the current source inverter.

2.1.2 Modulation Scheme

The modulation scheme is used to determine the operating mode of each phase and generate the corresponding gate signals for the series switches and H-bridge switches. In the proposed three-phase transformerless SC-CSI, Sinusoidal Pulse Width Modulation (SPWM) is introduced; three sinusoidal reference signals with 120-degree phase displacement are used for phases A, B, and C, respectively.

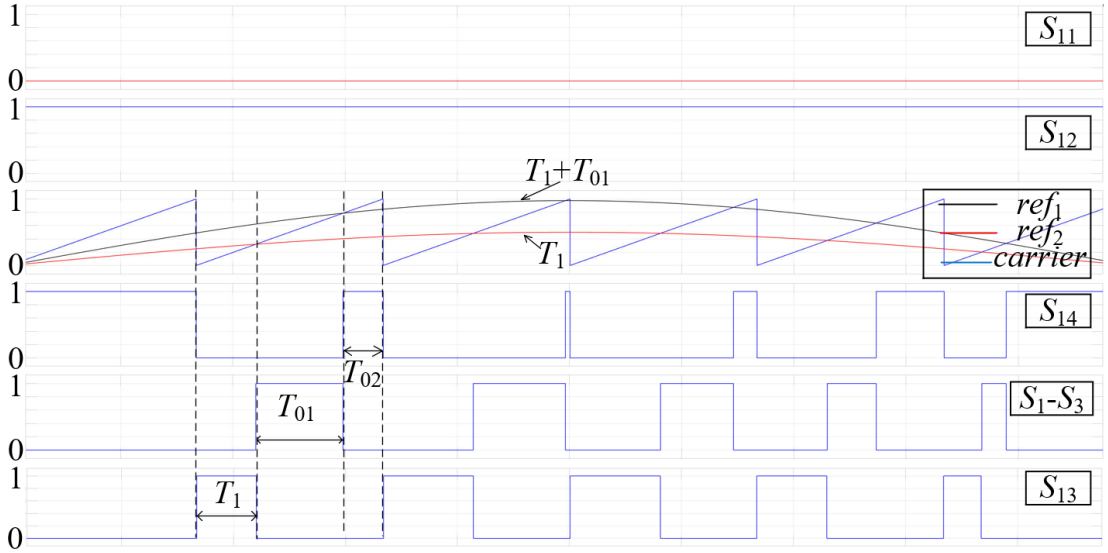

Fig. 2-5 Gating signal in the positive half-cycle.

Fig. 2-6 shows the gating signal processed by the modulation scheme. In the positive half-cycle, switches S_{11} to S_{1n} are turned on, while switches S_{21} to S_{2n} are turned off, so that the output current direction of each H-bridge CSI is determined. The switching period T_s is divided into three intervals, namely T_1, T_{01}, and T_{02}. The interval T_1 is obtained by comparing the sinusoidal modulation signal with the carrier wave. This interval is in the discharging mode. The interval T_{01} corresponds to the charging mode. The duration of T_{01} is determined according to the voltage-second balance of the dc-link inductors, so that the inductor currents can be maintained. The remaining interval T_{02} corresponds to the freewheeling mode.

In the negative half cycle, the same principle is applied with the opposite H-bridge current direction.

2.1.3 Passive Element Design

The passive components in the proposed three-phase transformerless SC-CSI should be properly designed to ensure smooth dc-link current and acceptable output harmonic performance. Therefore, this section introduces the design of the dc-link inductors and ac-side LC filters used in the simulation study. In the proposed

transformerless SC-CSI, the dc-link inductors are used to smooth the dc-link current, which means that the main objective of the dc-link inductor design is to limit the dc-link current ripple within an acceptable range. So, if the ripple of inductor current (I_{dc}) is less than a certain value, 12%, the minimum required inductance value can be expressed as equation (2-1):

$$L_{dc} = \frac{V_{L\_max} * \Delta_t}{12\% I_{dc}} \tag{2-1}$$

where V_{L_max} means the maximum voltage across the inductor, and Δt represents the corresponding dwell times. In addition, the voltage-second products of the charging, discharging, and freewheeling intervals should all be considered over the fundamental period. The dc inductor voltage (V_{Ldc}) in a cycle is shown in Fig. 2-6.

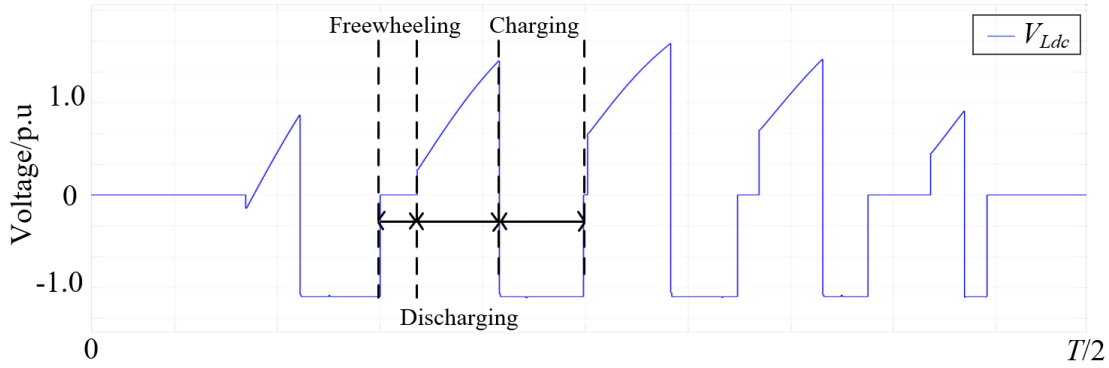

Fig. 2-6 V_{Ldc} in positive half cycle

The largest local voltage-second product appears during the discharging interval near the carrier peak. Therefore, the discharging state is selected as the worst-case condition for the DC-link inductor design. Under this condition, the L_{dc} can be further expressed as equation (2-2):

$$L_{dc} = \frac{V_{L\_discharging} * T_1}{12\% I_{dc}} \tag{2-2}$$

Furthermore, the discharging interval T_1 is determined by the sinusoidal modulation signal. It can be expressed as equation (2-3):

$$T_1 = m_a |\sin(w_t)| T_s \tag{2-3}$$

where T_s is the switching period. Therefore, a larger modulation index results in a longer discharging interval. In this thesis, the modulation index is selected as ma = 0.9 for the simulation study. The selected value is close to the upper limit of the linear modulation region, which provides high dc-link voltage utilization while avoiding overmodulation.

As for the filter design, in high-power applications, the filter inductance is usually selected to be close to 0.1 p.u. according to practical design experience [27]. A simplified circuit of the CSI for LC filter design is shown in Fig. 2-8.

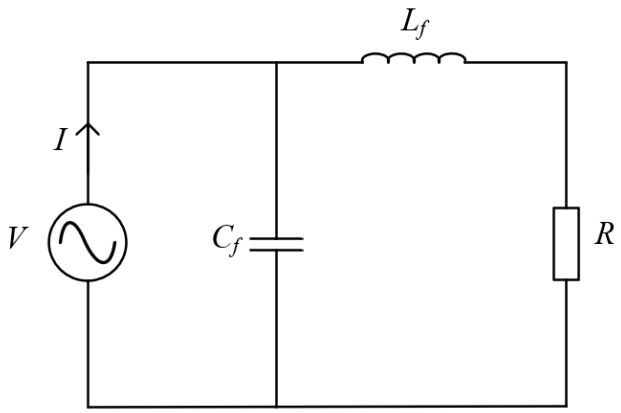

Fig. 2-7 Simplified circuit of the CSI for filter design.

Once L_f is selected, the C_f is designed based on the desired cutoff frequency of the second-order LC filter. The resonant frequency (f_0) of the LC filter should be selected between the fundamental frequency f_1 and the switching frequency (f_{sw}) [28]. It should be much higher than f_1 so that the fundamental component can pass through the filter without significant attenuation. Meanwhile, f_0 should be much lower than f_{sw} so that the switching-frequency harmonics can be effectively attenuated [29]. In this thesis, the output current THD is designed to remain below 5% as the power quality target, which is required by IEEE std 519-2022 [30].

2.2 Configuration of the Proposed Capacitor Voltage Balancing Scheme

Based on the configuration of the proposed three-phase transformerless SC-CSI, a corresponding control scheme is proposed, which is shown in Fig. 2-2.

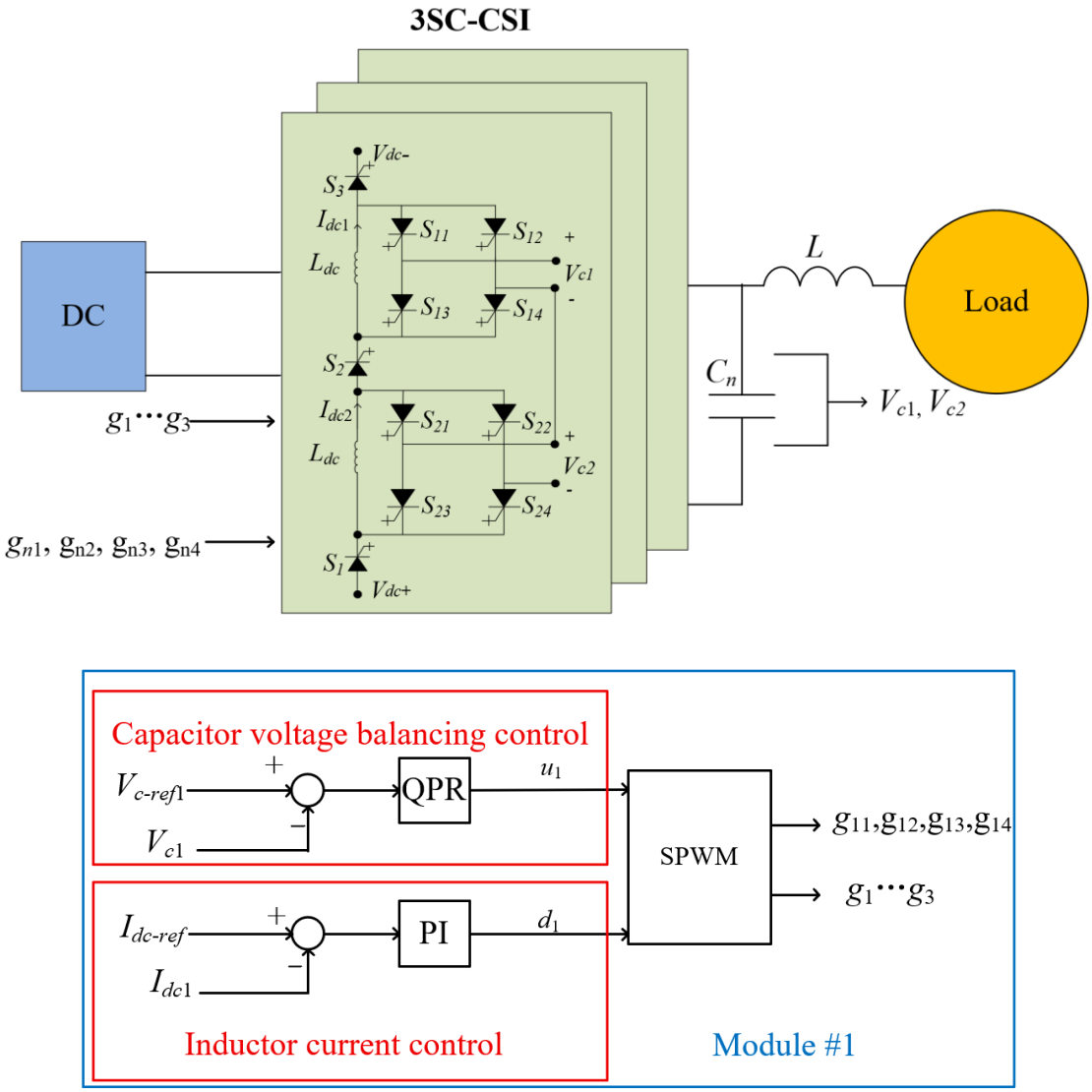

Fig. 2-8 Overall control block diagram.

2.2.1 Voltage Unbalance Analysis

Under ideal conditions, all capacitors and dc-link inductors in different cells are assumed to have identical parameters. Since the CSI cells in the same phase are controlled simultaneously, the dc-link inductors are connected in series during the

charging mode, forcing the same current to flow through all inductors. In addition, the output capacitors are connected in series during the power transfer stage, and their currents are balanced according to Kirchhoff's Current Law (KCL). Therefore, the proposed topology has inherent current and capacitor voltage balancing characteristics under ideal parameter conditions. However, in practical engineering applications, the capacitance values cannot be exactly identical due to manufacturing tolerances. The capacitor voltage dynamic equation will be expressed as equation (2-4):

$$\frac{dv_{C_i}}{dt} = \frac{i_{C_i}}{C + \Delta C_i} \tag{2-4}$$

where $C+\Delta C_i$ is the value after applying the mismatch. Therefore, the module with a smaller capacitance tends to withstand a higher voltage. In contrast, the module with a larger capacitance tends to have a lower voltage. In the proposed converter, the output voltage is the sum of each capacitor voltage of the modules in one phase. So, this capacitor mismatch will make capacitor voltages deviate from the desired value and finally break the inherent voltage balance and further bring the output voltage unbalance.

More importantly, long-term capacitor voltage unbalance may cause overvoltage stress to the switching devices [31]. This increases the risk of device failure increase the maintenance costs. Especially in medium-voltage or high-voltage systems. Therefore, an active control method is required to compensate for the capacitor mismatch.

2.2.2 Capacitor Voltage Balance Control Scheme

The control scheme directly focuses on capacitor voltage under capacitance mismatch conditions. When capacitance mismatch exists, the same series current no longer results in the same voltage variation for different capacitors. For this reason,

different cells should not be controlled with exactly the same switching intervals. Instead, each cell needs individual control. By adjusting the operating interval of each cell separately, the energy transferred to or from each capacitor can be regulated individually. So, this thesis adopts an individual control strategy for different cells instead of the simultaneous control used in the original topology.

Since the controlled capacitor voltage is a sinusoidal ac quantity, a proportional-resonant (PR) controller is suitable for the capacitor voltage balancing control. Compared with a conventional PI controller, the PR controller can track sinusoidal references in the stationary reference frame without using complex coordinate transformation [32]. The PR controller can provide a high gain at the selected resonant frequency, which helps reduce the steady-state tracking error of the sinusoidal capacitor voltage. The transfer function of an ideal PR controller is expressed as equation (2-5):

$$G_{\mathrm{PR}}(s) = K_p + \frac{2K_r s}{s^2 + \omega_0^2} \tag{2-5}$$

where K_p is the proportional gain, K_r is the resonant gain, and ω_0 is the resonant angular frequency. The proportional gain mainly affects the dynamic response, bandwidth, phase margin, and gain margin of the control system, while the resonant gain determines the tracking capability at the resonant frequency.

However, the ideal PR controller has an infinite gain at the resonant frequency and a very narrow resonant bandwidth. This may cause stability concerns and make the controller sensitive to small frequency variations. Therefore, a Quasi-PR controller is adopted in this thesis. Its transfer function is given by equation (2-6):

$$G_{\mathrm{QPR}}(s) = K_p + \frac{2K_r \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{2-6}$$

where ω_c is the cutoff angular frequency, which determines the bandwidth around the resonant frequency. Compared with the ideal PR controller, the QPR controller has a

finite resonant gain and an adjustable bandwidth. By properly selecting ω_c, the controller can maintain good tracking performance around the fundamental frequency.

An additional dc-link current control is required because individual capacitor voltage control will disturb the dc-link inductor currents. If only the capacitor voltages of the two cells in one phase are controlled independently, the charging and discharging intervals of the two cells are adjusted separately to restore the capacitor voltage balance.

However, the dc-link inductors in the same phase are connected in series, and therefore their currents are constrained to be identical. As a result, the inductor currents will become uncontrollable.

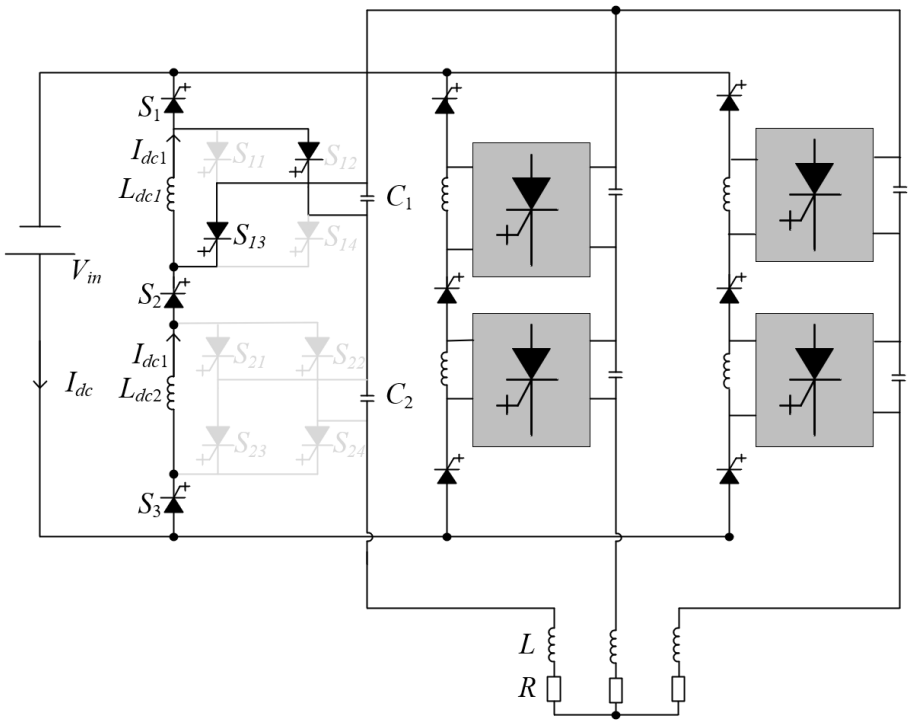

Fig. 2-9 Principle of capacitor voltage balancing with dc-link current constraint.

For example, as shown in Fig. 2-9, if V_{c2} is higher than V_{c1}, unit 2 should be controlled to discharge its capacitor, while unit 1 should be controlled to charge its capacitor. This rebalances the two capacitor voltages. However, because the dc-link inductors in the same phase are connected in series, the current through the two

inductors must be the same. Therefore, even if L_{dc1} should be discharged, it will be forced to be charged together with the other inductor. As a result, the dc-link inductor current will increase.

Therefore, an additional PI current control is introduced for each phase to regulate the overall charging duration of the dc-link inductors in the same phase, so that the capacitor voltage balancing control can be achieved while the dc-link current remains controlled.

So, the proposed control scheme is used to regulate the capacitor voltages and the dc-link inductor currents at the same time. In each phase, the two series-connected cells contribute together to the phase output voltage. Therefore, the capacitor voltage sharing between the two cells and the dc-link current of the phase both need to be controlled.

For the capacitor voltage control, the measured capacitor voltage of each cell is compared with its sinusoidal reference. The voltage error is then normalized by the voltage base. For the two cells in the same phase, the errors are divided into a common-mode part and a differential-mode part.

The common-mode part is applied to the two cells in the same direction, so it mainly helps the phase voltage follow its reference. The differential-mode part is applied to the two cells with opposite signs, so it can adjust the voltage distribution between the two cells. In this way, the capacitor voltage imbalance caused by parameter mismatch can be gradually reduced.

For the dc-link current control, the average current of the two inductors in the same phase is used as the feedback signal. A PI controller is adopted to regulate this average current. The output of the PI controller adjusts the timing command, which corresponds to $T_1 + T_{01}$. Therefore, the charging interval of the dc-link inductors can be adjusted according to the current error.

Finally, the voltage-loop command u_{n} and the current-loop command d_{n} are combined in the SPWM block to generate the gate signals. The voltage loop mainly decides how the phase voltage is shared by the two cells, while the current loop mainly controls the overall charging duration of the same phase. Although both loops affect the final switching signals, they act on different control variables, so the capacitor voltage balancing and the dc-link current regulation can be achieved together.

The tuning procedure of the QPR controller is as follows [33]. First, the cutoff angular frequency ω_c is selected to determine the bandwidth around the resonant frequency. If ω_c is too small, the resonant peak becomes very sharp and the controller becomes sensitive to frequency deviation. If ω_c is too large, the frequency selectivity of the resonant controller is reduced.

After ω_c is determined, the proportional gain K_p is tuned. The gain K_p mainly affects the overall gain and dynamic response of the control system. It is increased gradually from a small value until the capacitor voltage response becomes fast enough without large overshoot or oscillation. During this step, the resonant gain K_r is kept relatively small to avoid excessive resonance around the fundamental frequency.

Then, with K_p and ω_c fixed, the resonant gain K_r is tuned. The gain K_r mainly affects the magnitude of the resonant peak and the steady-state tracking accuracy at the fundamental frequency. A larger K_r can reduce the steady-state error of the sinusoidal capacitor voltage. However, an excessively large K_r may cause oscillation or reduce the stability margin. Therefore, K_r is increased gradually until the steady-state voltage tracking error is sufficiently small. Finally, the selected controller parameters are verified through simulation. The parameters used in this thesis are selected to achieve fast capacitor voltage balancing, small steady-state error, and acceptable THD.

2.3 Simulation Result

The feasibility of the proposed three-phase transformerless SC-CSI and the effectiveness of the capacitor voltage balancing control method are verified by simulation results based on MATLAB/Simulink. The simulations mainly focus on steady-state simulations, which are carried out under capacitance mismatch conditions to compare the system performance before and after applying the proposed capacitor voltage balancing control method. This comparison is used to verify that capacitance mismatch causes capacitor voltage imbalance and that the proposed control method can restore voltage balance among different cells.

Through these simulations, the dynamic response and parameter sensitivity of the proposed capacitor voltage balancing control method are verified. Simulation parameters of passive components are shown in Table 2-2.

Table 2-2 Simulation parameters of passive components

Item	Parameter	
L_{dc}	20 mH	
L	1.5 mH	
R	5 Ω	
C_n	800 uF	
Phase A	Phase B	Phase C
$1.2C_n$, $0.8C_n$	$1.2C_n$, C_n	$0.8C_n$, C_n

The switching devices are modeled as ideal unidirectional switches. The dc source is represented by a constant dc voltage source, and the load is modeled as a three-phase RL load. The simulation waveforms are shown in the per-unit system. To evaluate the capacitor voltage imbalance under nonideal parameter conditions, capacitance mismatch is introduced among different cells. In this simulation, different 20% capacitance mismatch conditions are applied to the three phases. Phase A is selected as the worst case for detailed analysis.

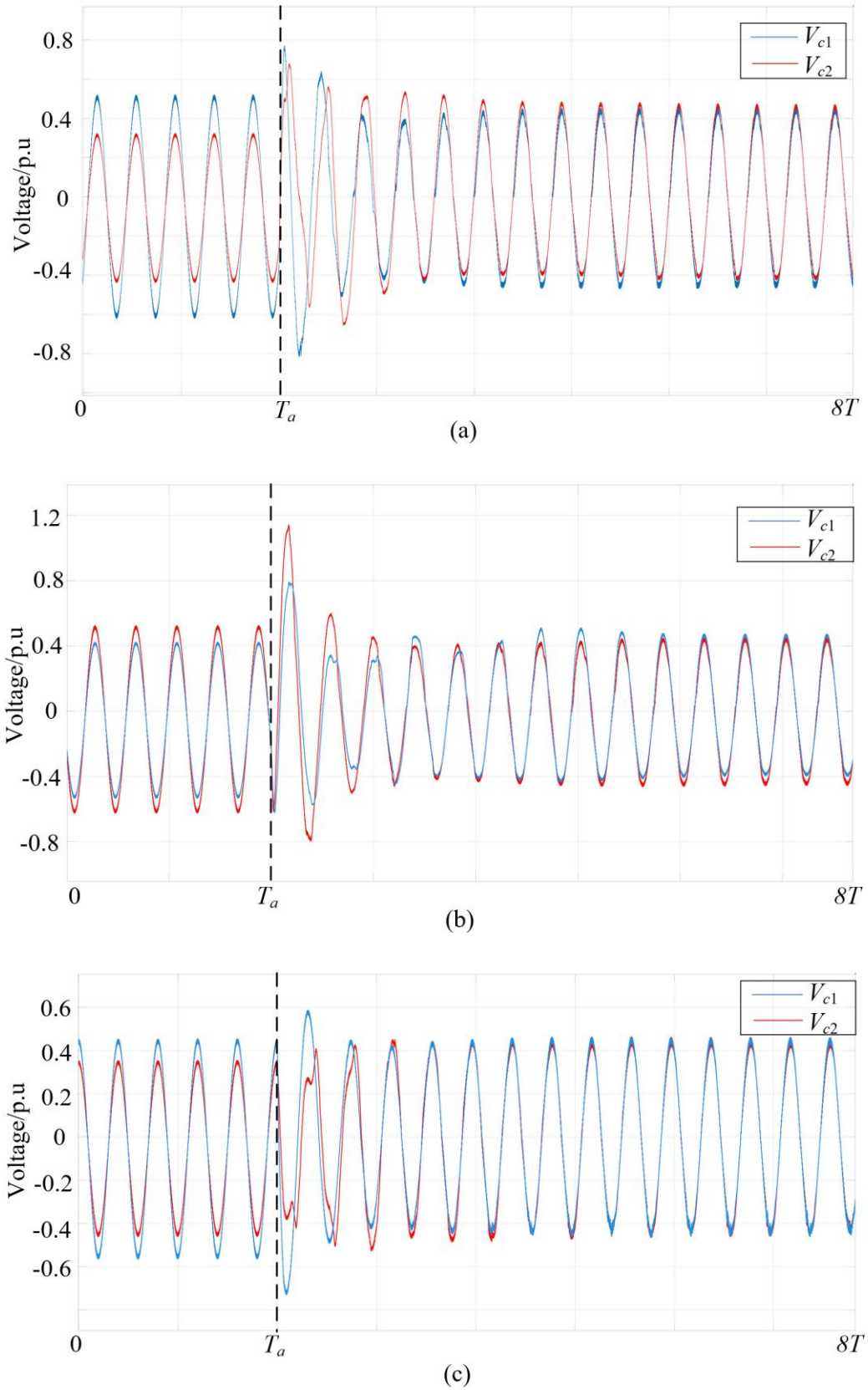

Fig. 2-10 Control performance of V_c (a) phase a, (b) phase b, (c) phase c.

Fig. 2-10 shows the capacitor voltage control performance under capacitance mismatch conditions. The capacitor voltages of the two cells in phases A, B, and C are shown in Fig. 2-9 (a), Fig. 2-9 (b), and Fig. 2-9 (c), respectively. The proposed capacitor voltage balancing control is activated at T_a. Before Ta, the proposed balancing control is not applied. Due to the capacitance mismatch, the two capacitor voltages in each phase have different amplitudes although they operate under the same modulation condition. This is because different capacitance values lead to different voltage variation rates under similar capacitor currents. As a result, the inherent voltage balancing characteristic of the topology is destroyed by the capacitance mismatch. Among the three phases, phase A shows the largest voltage difference between V_{c1} and V_{c2}, which agrees with the introduced worst-case mismatch condition.

At T_a, the proposed control is enabled. After a short transient process, the amplitudes of V_{c1} and V_{c2} gradually converge in all three phases. The voltage imbalance is significantly reduced, and the capacitor voltages are restored to balanced sinusoidal waveforms.

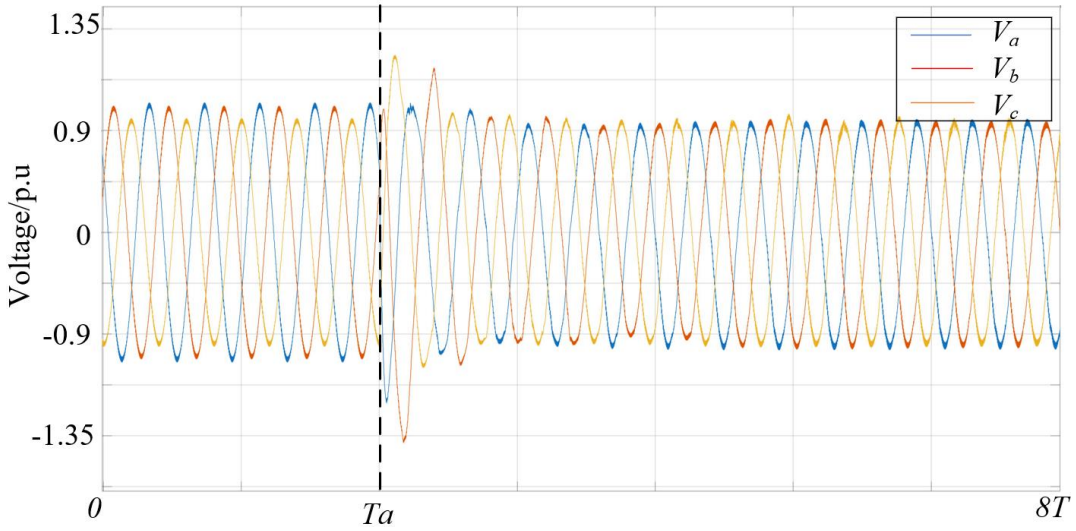

Fig. 2-11 Control performance of V_o.

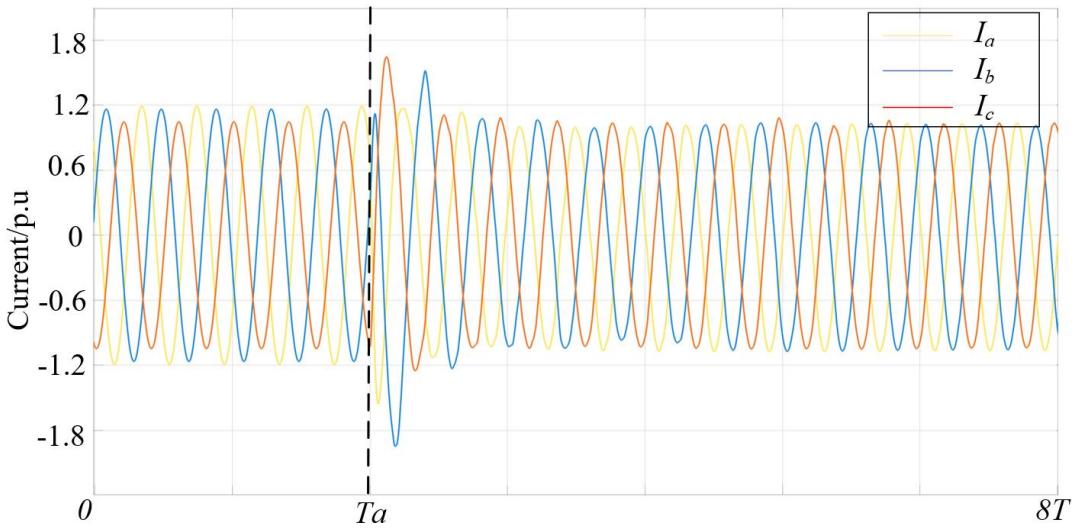

Fig. 2-12 Control performance of I_o.

Fig. 2-11 shows the three-phase output voltage before and after applying the proposed capacitor voltage balancing control. At T_a, the proposed control method is activated. After the transient process, the three-phase output voltages return to balanced sinusoidal waveforms with identical amplitudes and 120-degree phase displacement. Fig. 2-12 shows the corresponding three-phase output current waveforms. Similar to the output voltage, the output currents become balanced again and maintain sinusoidal waveforms. The results indicate that the proposed capacitor voltage balancing control can restore the capacitor voltage balance without causing steady-state distortion or imbalance in the output current.

As shown in Fig. 2-13, the inductor currents of two units in the three phases are compared after the control strategy is introduced. At the beginning of control implementation, the inductor currents increase for a short period due to the forced current-equalizing characteristic caused by the series connection of different units. Afterwards, they return to original values, which shows good inductor current control performance.

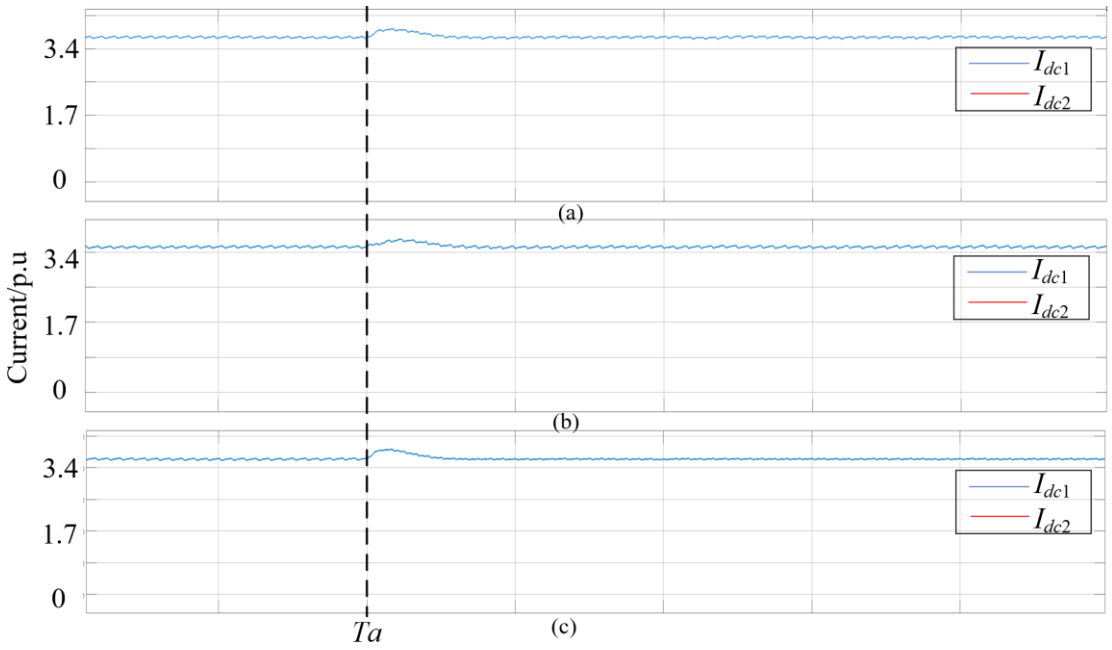

Fig. 2-13 Control performance of I_{dcn} in phase a (a), phase b (b), and phase c (c).

2.4 Summary

This chapter investigates the capacitor voltage balancing control of the proposed three-phase transformerless SC-CSI. First, the configuration, operation principle, and modulation scheme of the proposed converter are introduced. The dc-link inductor design and ac-side LC filter design are also discussed to establish the simulation system parameters.

Additionally, the capacitor voltage imbalance issue caused by capacitance mismatch is analyzed in detail. Although the capacitance mismatch may lead to different capacitor voltage variation rates and destroy the voltage balance among different cells. To address this issue, a QPR-based individual cell control method is proposed. So the Simulation results verify the effectiveness of the proposed capacitor voltage balancing control method.

Chapter 3 Circulating Current Elimination

This chapter investigates the interphase circulating current issue in the three-phase transformerless series-connected current source inverter. Since the proposed three-phase topology is extended from the single-phase topology, the operation of each phase can still be classified into charging, discharging, and freewheeling modes. However, when the original single-phase topology is directly extended to the three-phase system, undesired circulating current paths may be formed between different phases under certain switching-state combinations, which can affect the inherent current and voltage balancing characteristics of the converter. Therefore, this chapter is organized into two parts. First, the topology modification required for the proper operation of the three-phase converter is introduced and analyzed. Then, the possible circulating current paths in the modified topology are investigated under normal operating conditions.

3.1 Topology Modification for Circulating Current Elimination

The proposed three-phase transformerless SC-CSI is developed based on the single-phase transformerless SC-CSI. To apply this topology to a three-phase system, three single-phase units can be used to form phases A, B, and C. Since each phase inherits the operating principle of the single-phase topology, the operation of each phase can still be classified into charging, discharging, and freewheeling modes. Ideally, the three phases should operate independently, as shown in Fig. 3-1.

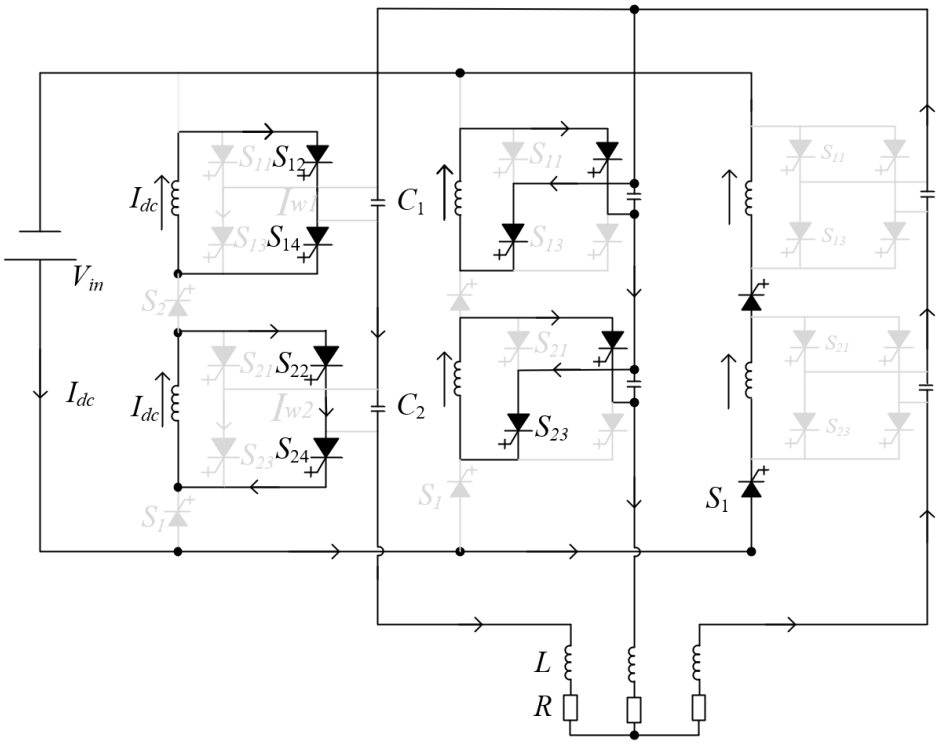

Fig. 3-1 Direct three-phase extension of the single-phase SC-CSI.

Under this condition, the series-connected inductors in each phase maintain the current balancing characteristic, and the output capacitors maintain the voltage balancing characteristic.

However, the direct extension of the single-phase topology to the three-phase system is not straightforward. Although each phase can operate normally when analyzed independently, the connection among the three-phase outputs may create additional current paths under some switching-state combinations. In particular, when one phase operates in the freewheeling mode while another phase operates in the discharging mode, an undesired interphase circulating current path can be formed, as shown in Fig. 3-3. This circulating current does not contribute to the load current, but it may disturb the dc-link inductor current balance and output capacitor voltage balance. Therefore, the direct three-phase extension must be modified before it can operate properly.

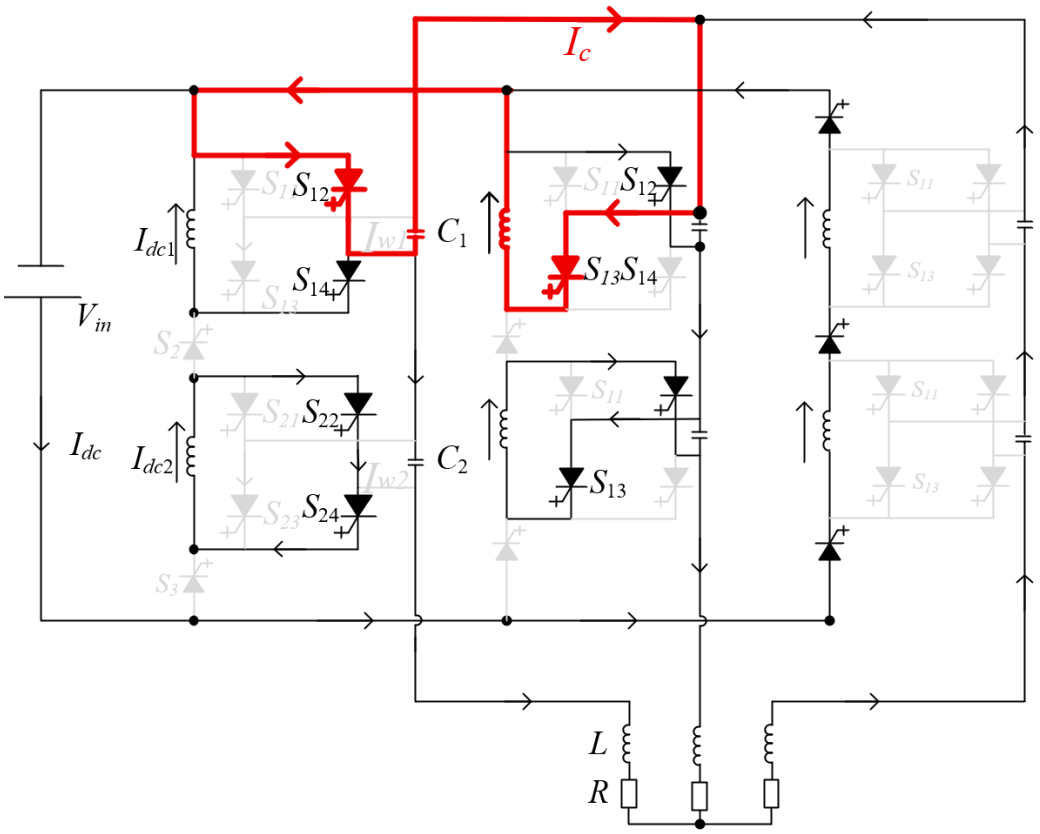

Fig. 3-2 Circulating current path in the direct three-phase extension.

Based on the above analysis, the undesired circulating current is caused by the direct electrical connection between different phases during certain switching-state combinations. Therefore, an additional switch is inserted in each phase to control the connection between the phase module and the common dc path. The additional switch is denoted as S_3 in each phase. During normal operation, S_3 is turned on or off according to the operating mode of the corresponding phase. When the phase should participate in the normal current path, S_3 is turned on to allow the required current to flow. When an undesired interphase circulating current path may be formed, S_3 is turned off to isolate the corresponding phase from the common path. In this way, the circulating current path is interrupted.

Therefore, the additional switch S_3 is controlled synchronously with the existing switches S_1 to S_3. Its main function is to control the start and end of the charging process

of the dc-link inductor L_{dc}, together with the other series-connected switches. Specifically, S_3 uses the same gating signal as S_1 and S_2. A more complicated control strategy could be developed by detecting the operating states of the other phases and determining the switching action of S_3 accordingly. However, such a strategy would increase both the switching frequency and the control complexity. Therefore, the synchronous control of S_3 is adopted to block the circulating current path while maintaining a simple control structure.

3.2 Circulating Current Path Analysis Under Normal Operation

After the additional switches are applied, the modified three-phase topology can block the circulating current path found in the direct three-phase extension. However, it is still necessary to verify whether other circulating current paths may appear under normal operating conditions.

Since each phase can operate in one of three modes, which are charging, discharging, and freewheeling, the total number of operating-mode combinations in the three-phase converter is $3^3 = 27$. In this section, all switching states within one fundamental period are analyzed to verify whether any valid interphase circulating current path exists in the proposed topology. To illustrate the analysis method, one representative switching-state combination is selected, as shown in Fig. 3-3.

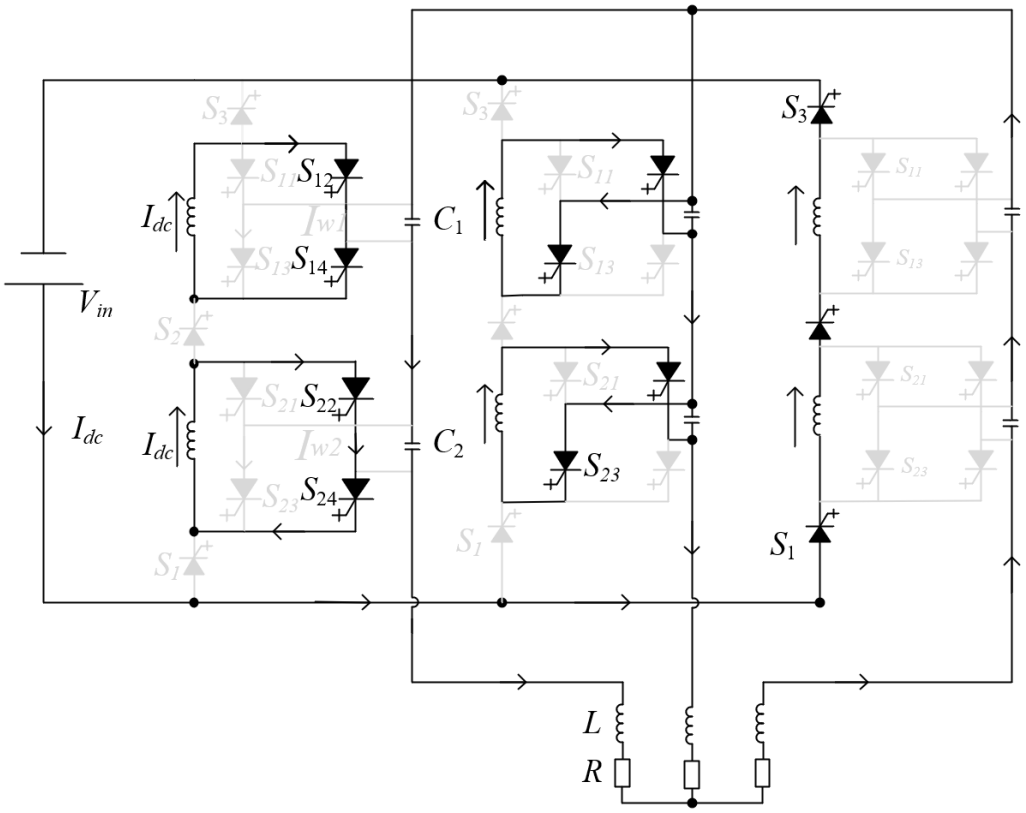

Fig. 3-3 Representative switching-state combination for circulating current path analysis.

In this case, phase A operates in the freewheeling mode, phase B operates in the discharging mode, and phase C operates in the charging mode.

For an undesired circulating current to exist, a closed current loop that does not contribute to the load current must be formed [34]-[40]. Therefore, the possible current paths between different phases are examined in this interval. The branch currents I_1 and I_2 are compared to determine whether additional current flows between the phases. In addition, the current through the branch containing the additional switch S_3 is measured. The H-bridge output current I_w is also observed during the freewheeling and charging modes. Under normal operation, these branches should not conduct current in the corresponding intervals. If a nonzero current appears in these branches, it indicates the existence of an undesired circulating current path.

It should be noted that, during the charging mode, one switch of the H-bridge remains in an idle on-state because of the switching constraints of the CSI. As a result, a potential interphase current path may be observed from the circuit connection. However, due to the unidirectional conduction characteristic of the switching devices, this path is not valid, and the circulating current is blocked.

Following the same analysis procedure, all operating-state combinations within one fundamental period are investigated. The results show that no valid closed current loop is formed between different phases in the proposed topology. Therefore, it can be concluded that no valid interphase circulating current path exists under normal operating conditions after the additional switches are introduced.

In addition, in practical implementations, the dc-link inductances of different modules may not be exactly identical due to manufacturing tolerances. Therefore, dc-link inductance mismatch is introduced to further verify whether interphase circulating current exists in the proposed topology. If an interphase circulating current path exists, the mismatch in dc-link inductance may cause unequal inductor currents or disturbance in the capacitor voltages. In this thesis, 20% dc-link inductance mismatch is introduced. The two dc-link inductor currents I_{dc1} and I_{dc2}, as well as the capacitor voltages V_{c1} and V_{c2}, are compared to evaluate the influence of the inductance mismatch. The simulation results show that even with 20% inductance mismatch, no interphase circulating current is introduced.

3.3 Simulation Result

The feasibility of the proposed three-phase transformerless SC-CSI and the circulating current analysis are verified by simulation results based on MATLAB/Simulink. The simulations are classified into three parts: (1) the simulation

of the direct three-phase extension without additional switches to verify the existence of the interphase circulating current, (2) the comparison simulation before and after applying the additional switches to verify the effectiveness of the topology modification, and (3) the simulation under dc-link inductance mismatch to verify that no interphase circulating current exists in the proposed topology under parameter mismatch conditions.

The switch devices are modeled by ideal unidirectional switches Gate turn-off thyristor (GTO). The load is represented by a three-phase RL load. The H-bridge output current W_i is used to identify the existence of undesired circulating current. Because it is the most direct indicator under the critical switching condition. In most branches of the converter, current flows during normal operation.

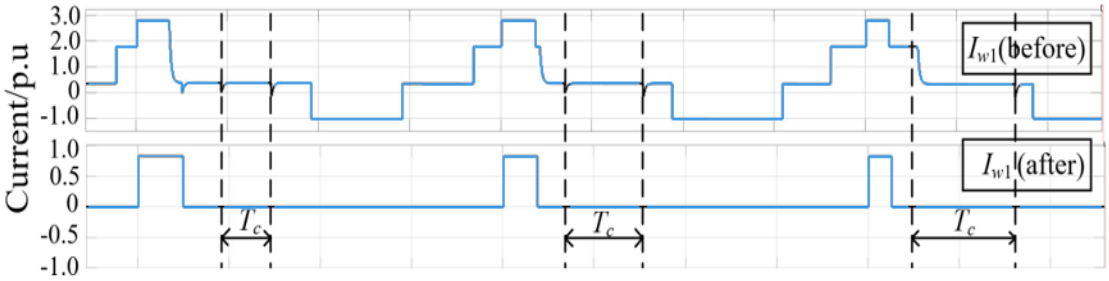

Fig. 3-4 Comparison of I_{wn} before and after adding S_3.

Fig. 3-4 compares the H-bridge output current I_{w1} before and after introducing the additional switch. The corresponding switching signals of phases A and B are also shown to identify the critical switching-state interval. The interval T_c represents the condition where one phase operates in the freewheeling mode while another phase operates in the discharging mode. According to the normal operating principle, the H-bridge output current of the freewheeling phase should be zero during this interval.

Before the additional switch is introduced, an undesired current appears in I_{w1} during T_c. This current is not generated by the normal discharging operation of the

corresponding H-bridge. Instead, it is caused by the undesired interphase current path formed between different phases under this switching-state combination. Therefore, the nonzero I_{w1} during T_c directly verifies the existence of the interphase circulating current. After the additional switch is introduced, I_{w1} remains zero during the same T_c interval. This indicates that the undesired current path is blocked by the additional switch. Therefore, no circulating current flows through the H-bridge output branch under the same switching condition. The comparison verifies that the proposed topology modification effectively blocks the interphase circulating current path.

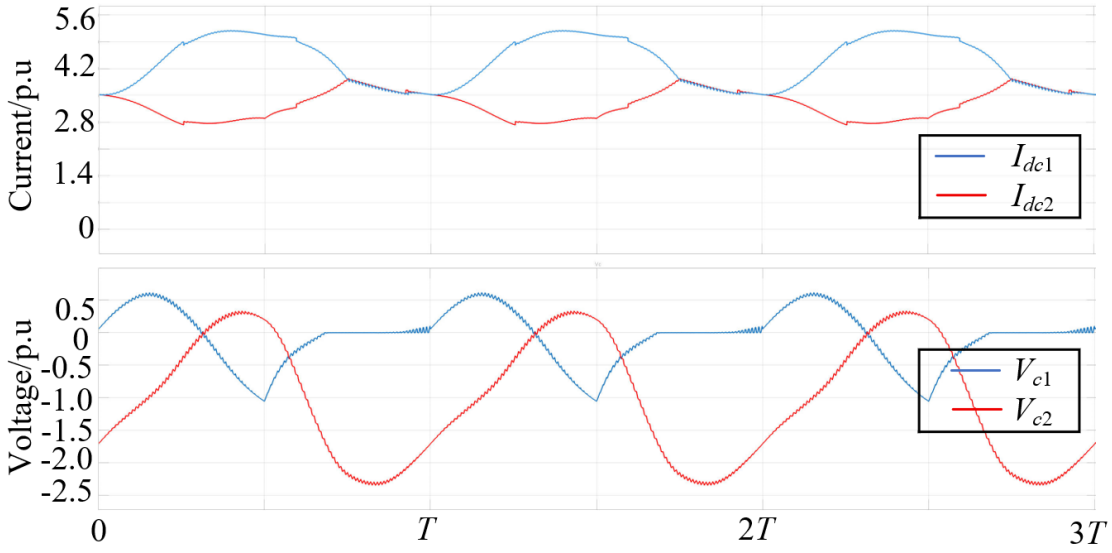

Fig. 3-5 I_{dcn} and V_{cn} (without S_3).

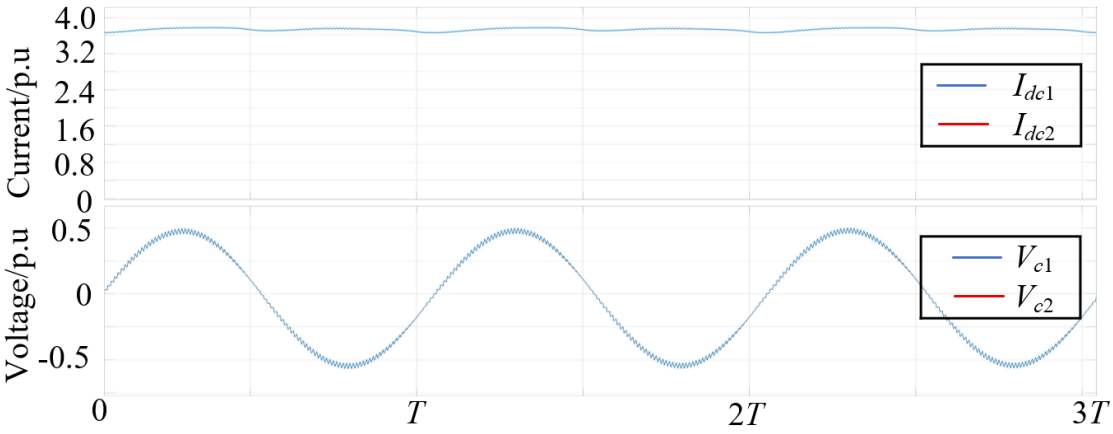

Fig. 3-6 I_{dcn} and V_{cn} (after applying S_3).

Fig. 3-5 shows the dc-link inductor currents and capacitor voltages of the direct three-phase extension without the additional switch S_3. However, the two dc-link inductor currents I_{dc1} and I_{dc2} are still seriously unbalanced. This indicates that an undesired interphase circulating current path is formed in the direct three-phase extension. The two capacitor voltage waveforms have different amplitudes and dc offsets, and the voltage balancing characteristic of the original single-phase topology is destroyed. This result verifies that the direct three-phase extension of the single-phase transformerless SC-CSI cannot operate properly without topology modification. Fig. 3-6 shows the corresponding waveforms after the additional switches S_3 are introduced. With the additional switches, the undesired interphase current path is blocked. As a result, the dc-link inductor currents I_{dc1} and I_{dc2} remain balanced and almost overlap with each other. Meanwhile, the capacitor voltages V_{c1} and V_{c2} also become balanced sinusoidal waveforms.

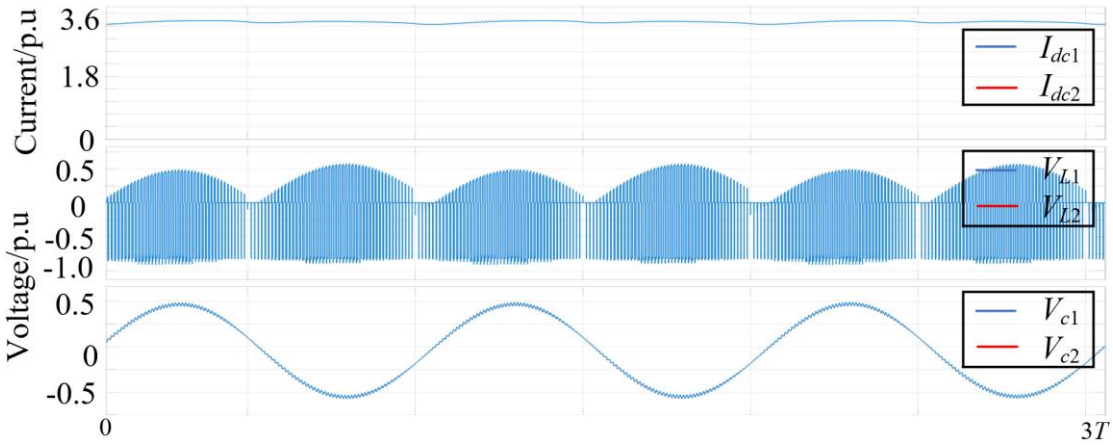

Fig. 3-7 I_{dc}, V_{Ln}, V_{cn} (before introducing inductor mismatch).

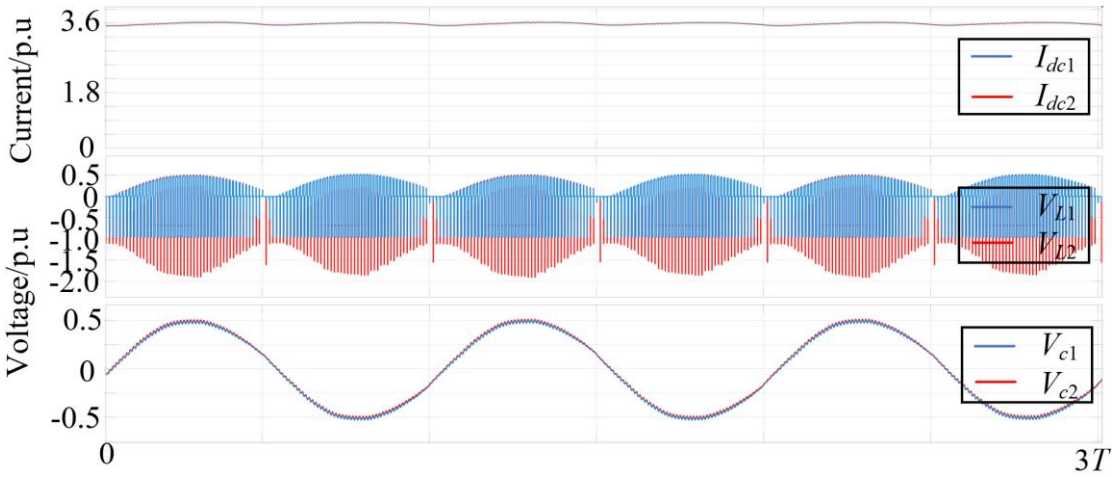

Fig. 3-8 I_{dc}, V_{Ln}, V_{cn} (after introducing inductor mismatch).

Fig. 3-7 shows the simulation results under dc-link inductance parameter mismatch. The dc-link inductor currents, dc-link inductor voltages, and capacitor voltages are compared to verify whether the inductance mismatch introduces undesired interphase circulating current. Before the inductance mismatch is introduced, the two dc-link inductor currents I_{dc1} and I_{dc2} are well balanced. The capacitor voltages V_{c1} and V_{c2} also remain balanced. This indicates that the proposed three-phase topology with the additional switches operates normally and maintains its inherent current and voltage balancing characteristics.

After 20% dc-link inductance mismatch is introduced, the inductance values of the two cells are no longer identical. As shown in Fig. 3-8, the inductor voltage waveforms V_{L1} and V_{L2} become different because different inductance values require different voltage responses under the same current variation. However, the dc-link inductor currents I_{dc1} and I_{dc2} still remain overlapped. This result indicates that the inductance mismatch does not generate an additional interphase circulating current path. Although the inductor voltages are affected by the parameter mismatch, the charging path of the dc-link inductors is still connected in series. Therefore, the same current is forced to flow through the two inductors. Since no independent closed current loop is formed

between different phases, the inductance mismatch only changes the local inductor voltage distribution and does not create circulating current.

3.4 Summary

This chapter investigates the interphase circulating current issue in the three-phase transformerless SC-CSI. First, the direct extension of the single-phase transformerless SC-CSI to the three-phase system is analyzed. It is found that undesired circulating current paths may be formed under certain switching-state combinations, which can break the inherent current and voltage balancing characteristics of the converter. To address this issue, an additional switch is introduced in each phase to block the undesired current path and ensure the proper operation of the three-phase topology.

In addition, the possible circulating current paths in the proposed topology are analyzed under normal operating conditions. Based on the analysis of all switching-state combinations, no valid interphase circulating current path exists. Finally, simulation results verify the circulating current issue in the direct three-phase extension and confirm the effectiveness of the proposed topology modification.

Chapter 4 Conclusions

4.1 Contributions and Conclusions

This thesis investigates a three-phase transformerless series-connected current source inverter for medium-voltage and high-power applications. Based on the previously proposed single-phase transformerless SC-CSI, the topology is extended to a three-phase system. Two main issues are studied in this thesis: capacitor voltage imbalance caused by parameter mismatch and interphase circulating current caused by the direct three-phase extension.

First, the configuration, operation principle, and modulation scheme of the proposed three-phase transformerless SC-CSI are introduced. Under ideal conditions, this converter has inherent voltage and current balance capability.

Second, the capacitor voltage imbalance issue caused by capacitance mismatch is analyzed. Since different capacitance values lead to different capacitor voltage variation rates, the inherent voltage balancing characteristic may be destroyed in practical implementations. To address this issue, an individual cell control method is proposed. Simulation results show that the proposed control method can restore capacitor voltage balance under capacitance mismatch conditions while maintaining balanced three-phase output voltage and current.

Third, the interphase circulating current issue is investigated. It is shown that the direct three-phase extension of the single-phase topology may form undesired current paths under certain switching-state combinations. Therefore, an additional switch is introduced in each phase to block the circulating current path. Simulation results verify

that the proposed topology modification eliminates the undesired circulating current and restores the inherent current and voltage balancing characteristics.

Finally, the modified topology is further analyzed under all operating-state combinations and dc-link inductance mismatch conditions. The results show that no valid interphase circulating current path exists after the additional switches are applied, even when 20% dc-link inductance mismatch is introduced.

4.2 Future Work

Future work can be conducted in the following aspects. First, hardware experiments should be carried out to validate the proposed topology and control method under practical operating conditions. Second, in addition to capacitor voltage balancing control, dc-link inductor current control can be further investigated to achieve more accurate power regulation of the proposed topology. Finally, more practical operating conditions, such as load variation, grid disturbance, unbalanced operation, and fault conditions, can be considered.

Reference

[1] B. Wu, High-Power Converters and AC Drives. New York, NY, USA/Piscataway, NJ, USA: *Wiley/IEEE Press*, 2006.

[2] Rockwell Automation Power Flex 7000 report. [Online]. Available: https://www.rockwellautomation.com/en-ca/products/hardware/vfds-variable-frequency-drives/powerflex-7000-ac-drive.html.

[3] ABB Medium Voltage AC Drives report. [Online]. Available: https://www.abb.com/global/en/areas/motion/drives/medium-voltage-ac-drives.

[4] ABB's PCS6000 wind converter report. [Online]. Available: https://www.abb.com/global/en/areas/renewable-power/wind-converters/full-power-medium-voltage-converters/pcs6000.

[5] Siemens Energy's MVDCPLUS system report. [Online]. Available: https://www.siemensenergy.com/global/en/home/products-services/product-offerings/medium-voltage-direct-current.html.

[6] X. Guo, D. Xu, J. M. Guerrero, and B. Wu, “Space vector modulation for DC-link current ripple reduction in back-to-back current-source converters for microgrid applications,” IEEE Trans. Ind. Electron., vol. 62, no. 10, pp. 6008–6013, Oct. 2015.

[7] J. He et al., “A fault-tolerant operation approach for grid-tied five-phase current-source converters with one-phase supplying wire broken,” IEEE Trans. Power Electron., vol. 34, no. 7, pp. 6200–6218, Jul. 2019.

[8] J.D.Ma, B.Wu, N.R.Zargari, and S.C.Rizzo, " A space-vector-modulated CSI-based AC drive for multirotor applications,” IEEE Trans. Power Electron., vol. 16, no. 4, pp. 535–544, Jul. 2001.

[9] Z.Bai, Z.Zhang, and X.Ruan, “A natural soft-commutation PWM scheme for current source converter and its logic implementation,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2772–2779, Jul. 2011.

[10] S. Suroso and T. Noguchi, “Multilevel current waveform generation using inductor cells and H-bridge current-source inverter,” IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1090–1098, Mar. 2012.

[11] P. Barbosa, H. Braga, M. Rodrigues, and E. Teixeira, “Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems,” IEEE Trans. Power Electron., vol. 21, no. 4, pp. 1116–1124, Jul. 2006.

[12] F. Gao, P. Loh, F. Blaabjerg, and D. Vilathgamuwa, “Five-level current source inverters with buck-boost and inductive-current balancing capabilities,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2613–2622, Aug. 2010.

[13] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, “An eight-switch five-level current source inverter,” IEEE Trans. Power Electron., vol. 34, no. 9, pp. 8389–8404, Sep. 2019.

[14] Z.Bai and Z.Zhang, “Conformation of multilevel current source converter topologies using the duality principle,” IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2260–2267, Sep. 2008.

[15] D. Xu, N. R. Zargari, B. Wu, J. Wiseman, B. Yuwen, and S. Rizzo, “A medium voltage AC drive with parallel current source inverters for high power applications,” in Proc. IEEE36th Power Electron. Specialists Conf., 2005, pp. 2277–2283.

[16] L. Ding, Z. Quan, and Y. W. Li, “Common-mode voltage reduction for parallel CSC-fed motor drives with multilevel modulation,” IEEE Trans. Power Electron., vol. 33, no. 8, pp. 6555–6566, Aug. 2018.

[17] L. Ding and Y. Li, “Multilevel CSC system based on series-parallel connected three-phase modules with optimized carrier-shift SPWM,” IEEE Trans. Power Electron., vol. 36, no. 4, pp. 3957–3966, Apr. 2021.

[18] P. E. Melin et al., “Analysis and design of a multicell topology based on three-phase/single-phase current-source cells,” IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6122–6133, Sep. 2016.

[19] C. Baier, P. Melin, J. Espinoza, J. Munoz, and J. Guzman, “A novel multi-level topology based on current source power cells for high performance applications,” in Industrial Technology (ICIT), 2010 IEEE International Conference on, March 2010, pp. 1333–1338.

[20] C.R.Baier, P.E.Melin, J.I.Guzman, M.Rivera, J.A.Munoz, J.Rothen and J.Espinoza, “Current-source cascaded multilevel converters based on single-phase power cells,” in Proc. IEEE Ind. Electron. Conf. (IECON 2013), Vienna, 2013, pp.6207-6212.

[21] Q.Wei, B.Wu, D.Xu, and N.Zargari, " A medium-frequency transformer-based wind energy conversion system used for current source converter-based offshore wind farm,” IEEE Trans. Power Electron., vol. 32, no. 1, pp. 248–259, Jan. 2017.

[22] Q. Wei, B. Wu, D. Xu, and N. R. Zargari, “Power balancing investigation of grid-side series-connected current source inverters in wind energy conversion systems,” IEEE Trans. Power Electron., vol. 64, no. 12, pp. 9451–9460, Dec. 2017.

[23] L. Xing and Q. Wei, “Series-connected current-source inverters: F_{sw} = 60 hz,” IEEE Trans. Power Electron., vol. 35, no. 9, pp. 8882–8885, Sep. 2020.

[24] L. Xing and Q. Wei, “Series-connected current source inverters with less switches,” IEEE Trans. Power Electron., vol. 35, no. 6, pp. 5553–5556, Jun. 2020.

[25] M.Popat, B.Wu, F.Liu, and N.Zargari, “Coordinated control of cascaded current source converter-based offshore wind farms,” IEEE Trans. Sustain. Energy, vol. 3, no. 3, pp. 557–565, Jul. 2012.

[26] L. Xing, Q. Wei, and Y. Li, “Transformerless series connected current source converter,” IEEE Trans Power Electron, vol. 37, no. 8, pp. 8811–8815, 2022.

[27] M. Hassani and Q. Wei, “Transformerless modular current source inverter for hig h power medium-voltage PV system,” in Proc. IEEE 10th Int. Power Electron. Motion Control Conf., (IPEMC 2024 ECCE Asia), 2024, pp. 1937–1942.

[28] G. Ertasgin, D. Whaley, W. Soong, and N. Ertugrul, “Low-pass filter design of a c urrent-source 1-ph grid-connected PV inverter,” in *2016 57th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUC ON)*, 2016.

[29] S. Jayalath and M. Hanif, “CL-filter design for grid-connected CSI,” in *2015 IEE E 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics C onference (COBEP/SPEC)*, 2015.

[30] IEEE std 519-2022.

[31] H. Sheng, F. Wang, and C. W. Tipton IV, “A Fault Detection and Protection Sche me for Three-Level DC-DC Converters Based on Monitoring Flying Capacitor Voltag e,” *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 685-697, Feb. 2012.

[32] M.Parvez “Performance analysis of PR current controller for single-phase inverters, ” *4th IET Clean Energy and Technology Conference (CEAT 2016)*, *Kuala Lumpur, Malaysia*, pp 1-8. 2016.

[33] T.Ye, N. Dai, C. -S. Lam, M. -C. Wong and J. M. Guerrero, “Analysis, Design, and Implementation of a Quasi-Proportional-Resonant Controller for a Multifunctional

Capacitive-Coupling Grid-Connected Inverter," *IEEE Trans. Ind. Applicat*., vol.52, no.5, pp. 4269-4280, Sep.-Oct. 2016.

[34] L. Ben-Brahim, A. Gastli, M. Trabelsi, K. A. Ghazi, M. Houchati, and H. Abu-Rub, "Modular Multilevel Converter Circulating Current Reduction Using Model Predictive Control," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3857–3866, Jun. 2016.

[35] H. Zhan, Z. Q. Zhu, and M. Odavic, "Analysis and Suppression of Zero Sequence Circulating Current in Open Winding PMSM Drives With Common DC Bus," *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3609–3620, Jul./Aug. 2017.

[36] L. Ding, Z. Quan, and Y. W. Li, "Common-Mode Voltage Reduction for Parallel CSC-Fed Motor Drives With Multilevel Modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6555-6566, Aug. 2018.

[37] J. He, Q. Li, H. Wang, Y. Lyu, H. Jia, and C. Wang, "SVM Strategies for Simultaneous Common-Mode Voltage Reduction and DC Current Balancing in Parallel Current Source Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8859-8871, Oct. 2018.

[38] L. Ding and Y. W. Li, "Simultaneous DC Current Balance and Common-Mode Voltage Control With Multilevel Current Source Inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9188-9197, Nov. 2018.

[39] Z. Ye, D. Boroyevich, J. Choi, and F. C. Lee, "Control of Circulating Current in Two Parallel Three-Phase Boost Rectifiers," *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 609-615, Sep. 2002.

[40] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Common-Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source

Converters With Discontinuous Space-Vector Modulation," *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3925-3935, Dec. 2011.