HIGH–POWER MEDIUM–VOLTAGE MOTOR DRIVE: CONVERTER TOPOLOGY, MODULATION, AND CONTROL

By

Hoang Le

B. Eng., Danang University of Science and Technology, Vietnam, 2018

A thesis
presented to Lakehead University
in partial fulfillment of the
requirements for the degree of
Master of Science
in the program of
Electrical and Computer Engineering

Thunder Bay, Ontario, Canada, 2021

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I authorize Lakehead University to lend this thesis to other institutions or individuals for the purpose of scholarly research.

I further authorize Lakehead University to reproduce this thesis by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

I understand that my thesis may be electronically available to the public.

HIGH–POWER MEDIUM–VOLTAGE MOTOR DRIVE: CONVERTER TOPOLOGY, MODULATION, AND CONTROL

Hoang Le
Master of Science
Electrical and Computer Engineering
Lakehead University, Thunder Bay, 2021

ABSTRACT

THE output power quality, device voltage sharing, power converter flying capacitor voltage ripple and motor torque ripple at low-frequency/speed operation are the major issues in high-power medium-voltage (MV) motor drives. In this thesis, a new four-level multilevel converter (4L-MLC) is proposed for MV drive applications. The proposed converter does not require series connection of devices, thereby the voltage sharing problems will be eliminated. Also, the new MLC does not require any isolated direct current (DC) sources and eliminates the need of complex phase-shifting transformer. Furthermore, the proposed MLC is also suitable for back-to-back operation due to the presence of a common DC-link.

In addition, a simple voltage balancing approach with reduced complex-

ity is proposed to regulate the flying capacitors voltage in the proposed MLC. The proposed approach eliminates the unwanted device switchings, thereby the device switching frequency is limited to the carrier frequency only. Also, a generalized pulse width modulator is developed to integrate the proposed voltage balancing approach with different multi-carrier pulse width modulation schemes (PWM) to control the MLC. The performance of the proposed voltage balancing approach is verified with phase-disposition PWM (PD-PWM) scheme.

The MLC flying capacitors will have very high voltage ripple under low-frequency/speed operation. To minimize these ripples, a modified multi-carrier PWM scheme is proposed. With this approach, the converter flying capacitors can handle a wide range of frequency/speed operation with a smaller capacitance value. Hence, the overall system cost and required space for installation will be low. The proposed converter and modified multi-carrier PWM scheme are applied to variable-speed motor drive application. The field-oriented control (FOC) in synchronous reference frame is implemented to control the motor speed/torque and flux. Finally, the simulation studies are presented to validate the dynamic and steady-state performance of the proposed variable-speed MV drive.

Index Terms

- Capacitor voltage balancing.
- Capacitor voltage ripple.
- Field oriented control.
- Multilevel converters.
- Motor drive system.
- Pulse width modulation schemes.
- Reference frame theory.
- Total harmonic distortion.

ACKNOWLEDGEMENTS

First and foremost, I would like to express a deep sense of gratitude and whole-hearted thanks to my supervisor, Dr. Apparao Dekka for his invaluable guidance, unwavering support, constant encouragement, and consistent kindness throughout the course of this work. His enthusiasm, vision, and profound technical insight have been the greatest source and motivation to make possible the accomplishment herein. It has been a genuine privilege to have worked with him, and I am very grateful that I have pursued my Master's studies under his excellent supervision.

I am highly obliged to my parents for their incessant love and sacrifice all throughout my life. Their unconditional assistance and lucid guidance can not be depicted by words, particularly in my periods of hardships and difficulties. Special thanks to my brother Thanh Le who helped me in tough times and provided me with encouraging words to achieve my goals. Without their help, the completion of my studies may not have been possible.

Last but not least, financial support from Dr. Apparao Dekka and Lakehead University is immensely acknowledged.

Thunder Bay, Ontario, Canada
December, 2021.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

2L	Two-level
3L	Three-level
4L	Four-level
5L	Five-level
AC	Alternating current
ANPC	Active neutral point clamped
APOD	Alternate phase-opposition disposition
CHB	Cascaded H-bridge
CMV	Common-mode voltage
CNPC	Cascaded neutral-point clamped
CSC	Current source converter
CSI	Current source inverter
DC	Direct current
DCC	Diode-clamped converter
DFOC	Direct field oriented control
DTC	Direct torque control
FCC	Flying capacitor converter
FOC	Field oriented control
GTO	Gate turn-off thyristor
HANPC	Hybrid active neutral point clamped
HCC	Hybrid clamped converter
HP	Horse power

HV	High voltage
HVDC	High-voltage direct current
IFOC	Indirect field oriented control
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
LSC-PWM	Level-shifted carrier pulse width modulation
MLC	Multilevel converter
MMC	Modular multilevel converter
MV	Medium voltage
NNPC	Nested neutral point clamped
NTC	Nested T-type converter
PD	Phase-disposition
PF	Power factor
PI	Proportional-integrator
POD	Phase-opposition disposition
PSC-PWM	Phase-shifted carrier pulse width modulation
PWM	Pulse width modulation
RMS	Root mean square
RPM	Revolutions per minute
SCIM	Squirrel cage induction motor
SFCC	Single flying capacitor converter
SHE	Selective harmonic elimination
SM	Submodule
SVM	Space vector modulation
THD	Total harmonic distortion
VSC	Voltage source converter
VSI	Voltage source inverter

LIST OF SYMBOLS

Superscript

$\widehat{\ }$	Peak quantity
$*$	Reference quantity

Subscript

j	Capacitor index number
$x \in \{a, b, c\}$	AC output quantities
r	Motor rotor quantities
s	Motor stator quantities
d	d-axis quantity
q	q-axis quantity

System Quantities

m_a	Amplitude modulation index
m	Number of voltage levels
f_o	Fundamental frequency (Hz)
θ_x	Phase angle of phase-x (rad)
θ_f	Rotor flux vector position (rad)
$C_{rx1}, C_{rx2}, C_{rx3}$	Carrier comparison output
f_{cr}	Carrier frequency (Hz)
P	Motor pole pairs

System Quantities

λ_r	Rotor flux linkage
T_e	Motor electromagnetic torque (N-m)
T_m	Motor load torque (N-m)
N_r	Motor rotor speed (RPM)
$\mathbf{S_x}$	Phase-x state
ω	Rotating reference frame speed (rad/sec)
ω_r	Rotor angular speed (rad/sec)
ω_s	Stator angular speed (rad/sec)
ω_{sl}	Motor slip-speed (rad/sec)

Voltage and Current Quantities

V_{dc}	DC-link voltage (V)
v_{Cx1}, v_{Cx2}	Flying capacitor voltages in phase-x (V)
V_{xN}	Pole voltage of phase-x (V)
v_{ab}, v_{bc}, v_{ca}	Three-phase line-to-line voltages (V)
v_{cmr}, v_{og}	Rectifier common-mode voltage (V)
v_{cmi}, v_{no}	Inverter common-mode voltage (V)
v_{cmv}, v_{ng}	Common-mode voltage (V)
v_{ds}, v_{qs}	Stator dq-axis voltages (V)
v_{sa}, v_{sb}, v_{sc}	Stator abc-axis voltages (V)
i_x	AC output current of phase-x (A)
i_{ds}, i_{qs}	Stator dq-axis currents (A)
i_{dr}, i_{qr}	Rotor dq-axis currents (A)
i_x	AC output current of phase-x (A)
i_{Cx1}, i_{Cx2}	Flying capacitor currents in phase-x (A)

Passive Elements

L_x	Load Inductor of phase-x (H)
r_x	Internal resistance of load inductor of phase-x (Ω)
R_x	Load resistor of phase-x (Ω)
C_{dc}	DC-link capacitance (F)
C_{x1}, C_{x2}	Flying capacitor capacitance of phase-x (F)

CHAPTER 1

OVERVIEW OF MEDIUM-VOLTAGE DRIVES

HIGH -power converters and medium-voltage (MV) drives have enjoyed an increasing attention since the invention of high-voltage semiconductor devices such as gate turn-off thyristor (GTO), integrated gate-commutated thyristor (IGCT), and insulated gate bipolar transistors (IGBT) [1]. These switching devices are widely used in high-power electronic applications owing to their optimal characteristics, low power losses, ease of gate control, and snubber less operation [2].

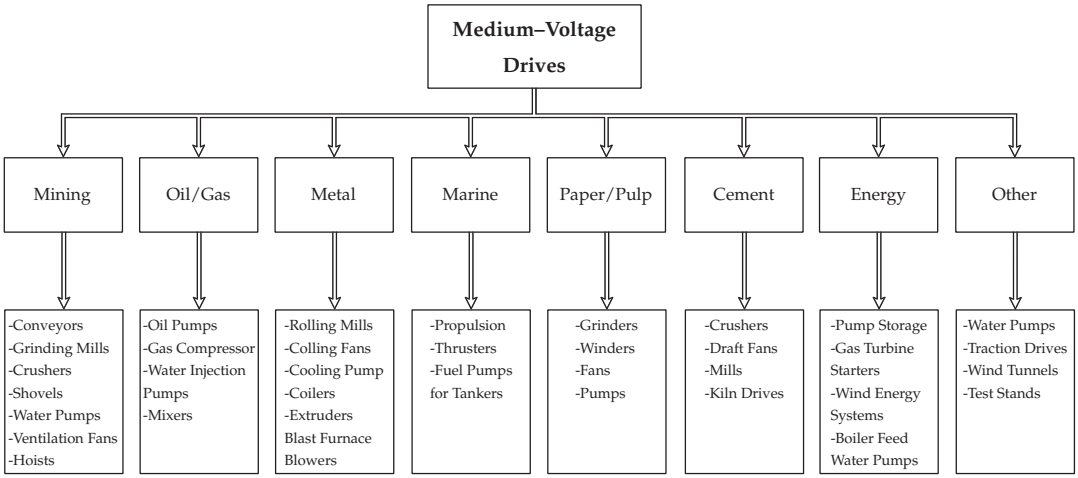


Figure 1.1. Applications of MV drives.

The MV drives have witnessed a great deal of development since 1980 in terms of power capacity and voltage rating, boosting their presence in almost all industrial sectors. MV drives are commercially available in single or parallel modules ranging from a power capacity of 0.4–40 MW at a voltage level of 2.3–13.8 kV. Nevertheless, the installed MV drives dominated the commercial applications with a power rating of 1–4 MW at a voltage level of 3.3–6.6 kV [3]. The MV drive applications cover a wide range of industry sectors such as mining, oil/gas, metal, paper/pulp, cement, power/energy, and other emerging areas as shown in Fig. 1.1. Around 85% of MV drives are used in pumps, fans, compressors, and conveyors as their technical requirements are relatively simple and can be achieved with standard MV drives [4].

The MV drives are available in both fixed and variable speed operations. With the advancement of high-power converters, the variable speed operation of MV drives is widely accepted in industry due to the increase in productivity together with significant saving of energy cost. However, the variable speed MV drives need a sophisticated and reliable power converters to handle MV operation, pulse width modulation (PWM) schemes to improve the output power quality and reduce the common-mode voltage stress, and high-performance closed-loop control methods [5].

In this thesis, a new multilevel converter (MLC) topology is proposed for high-power MV drive. The new topology eliminates the need of phase-shifting transformer and device voltage sharing problems, and reduces the control complexity. Several conventional and advanced PWM schemes which can improve power quality, reduce common-mode voltage stress, and minimize capacitor voltage ripple are developed and studied for new high-power MV drive. Also, a simple voltage balancing method is proposed to control the new MLC topology.

This chapter is organized as follows: the structure and technical challenges of MV drive are presented in Sections 1.1 and 1.2, respectively. In MV drive, the power converter plays a key role to attain various objectives along with power conversion process. The overview of power converters

and PWM schemes for MV drive are presented in Sections 1.3 and 1.4, respectively. The thesis objectives are given in Section 1.5. In Section 1.6, the outline of thesis is presented.

1.1 Medium-Voltage Drive Structure

The medium-voltage (MV) drive system consists of AC-DC power conversion (rectification) and DC-AC power conversion (inversion) stages as shown in Fig. 1.2. The rectification stage includes an AC-grid, line-side filter, phase-shifting transformer, and AC-DC converter (rectifier). On the other hand, the inversion stage includes a DC-link filter, DC-AC converter (inverter), motor-side filter, and MV motor [6]. The line-side and motor-side filters are optional, and their presence depends on the type of power converter employed and system harmonic requirements. The phase-shifting transformer with multiple secondary windings is employed, thereby the lower order harmonics such as 5^{th}, 7^{th}, 11^{th}, and 13^{th} will be cancelled to minimize the line-side harmonic distortion to meet the IEEE-519 harmonic standards and to block the drive common-mode current [7, 8]. The rectifier converts utility AC-grid voltage to DC voltage with fixed or adjustable magnitude. The commonly used rectifier topologies are multipulse diode-bridge rectifiers, multipulse thyristor rectifiers, and PWM rectifiers.

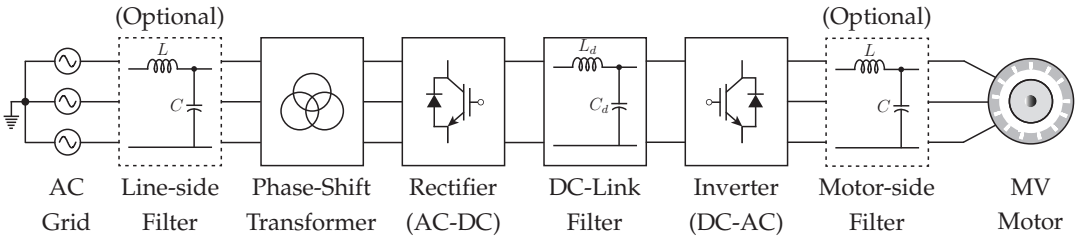


Figure 1.2. Structure of MV drive.

The DC-link filter is formed with either capacitor or inductor as shown in Fig. 1.2. The capacitor provides a stiff DC voltage to the inverter and it is referred to as voltage source inverter (VSI), whereas the inductor provides a

smooth DC current to the inverter and it is referred to as current source inverter (CSI). The VSI converts DC voltage to AC voltage with adjustable magnitude and frequency [9]. On the other hand, the CSI converts DC current to three-phase AC currents with adjustable magnitude and frequency [10]. The selection of inverter topology depends on the motor-side requirements, available switching devices, and type of control and PWM scheme employed.

1.2 Requirements of MV Drive

The demand for variable speed MV drives is continuously growing in industry due to their efficiency and sustainability along with economical benefits. However, the design and control of MV drives are still a challenging task as they need to fulfil various requirements related to power quality and grid interaction of line-side converters, design and control of motor-side converters, switching device constraints, and drive system requirements [11].

1.2.1 Line-Side Requirements

The current and voltage distortion, poor power factor, and LC resonance are the major issues on the line-side of the MV drive. Normally, the MV drives are connected to AC-grid through a line-side converter, which draws a distorted current and produces notches in voltage waveform. These waveforms cause false tripping of computer-controlled industrial processes, malfunction of control and protection circuits, heating of transformers, and equipment failure. Particularly, the false tripping of industrial process and protection circuits cause a longer downtime leading to a loss of production and revenue. Hence, the line-side converters are designed with LC filters or phase-shifting transformer to meet the harmonic standards such as IEC 1000-3-2 and IEEE-519, 2014 [7, 12].

Furthermore, the high power factor on the line-side is an important requirement in high-power MV drives as it represents the efficiency of energy

utilization. The use of capacitor banks is a simple and cost-effective solution to improve the line-side power factor [13]. However, the capacitor banks form LC resonant circuit with line inductance of the system. Due to the low resistance of MV system, the lightly damped LC resonance cause oscillations leading to overheating and excessive noise when the drive is not running [14]. Therefore, the design and control of line-side converters are key aspect in MV drive to achieve an efficient and reliable operation [15].

1.2.2 Motor-Side Requirements

The higher dv/dt, common-mode voltage (CMV), motor derating, and LC resonance are the major issues on motor-side of the MV drives. The motor-side converters are switched at a faster rate leading to high dv/dt at the falling and rising edge of motor-side converter output voltage [16]. The high dv/dt can cause premature failure of the motor winding insulation due to partial discharges. It also induce rotor shaft voltage due to stray capacitance between stator and rotor, which produces a current flowing to the shaft bearing leading to their premature failure [17]. The high dv/dt cause a voltage doubling effect due to the wave reflections in long cables. This may increase the voltage stress on the motor.

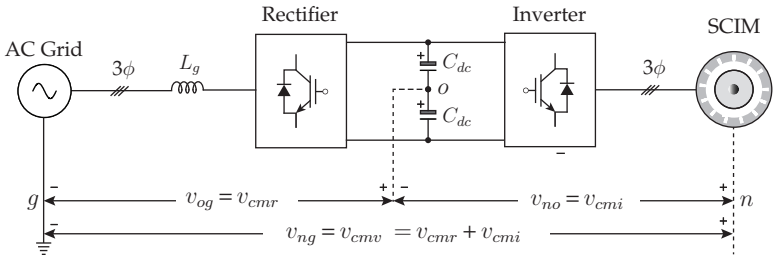


Figure 1.3. Common mode voltage in MV drive.

The switching action of line-side and motor-side converters generate CMV, which is normally a zero-sequence voltage superimposed with switching noise. If the CMV is not mitigated, it appears on the motor neutral with respect to the ground as shown in Fig. 1.3. The CMV increases the motor volt-

age stress leading to the premature failure of the motor winding system [18]. The replacement of a damaged MV motor is costly. Some of the CMV minimization methods are the use of isolation transformer and CMV filters, but they are costly and require extra space to install in the drives. On the other hand, the PWM schemes with flexible switching sequences are developed to minimize the CMV [19–21]. However, these methods are not effective and unable to mitigate it completely. Hence, the minimization of CMV is one of the research issues in MV drives.

In addition, the switching action of motor-side converters generate a large amount of harmonics in voltage and current waveforms. These harmonics cause power losses in the motor winding and magnetic core. As a consequence, the motor is derated and cannot operate at its full capacity. Thereby, the filters are installed at the motor terminals to reduce the dv/dt and harmonics [22]. However, the filters form LC resonant circuit with the motor inductances. Even though, the winding resistance provides damping, but this problem should be addressed at the design stage of the drive [23].

1.2.3 Switching Device Constraints

The higher switching frequency of semiconductor devices in line-side and motor-side converters cause significant power losses in MV drive. These power losses increase the MV drive cooling requirements along with physical size, and manufacturing and operating cost. In addition, the higher switching frequency affects the device thermal resistance that may prevent efficient heat transfer from the device to its heatsink [24]. Hence, the switching frequency is limited to less than 1 kHz in MV drives. However, the low switching frequency operation leads to higher harmonic distortion in voltage and current waveforms [25].

Furthermore, the switching devices are often connected in series for MV operation. However, they may not share the total voltage equally due to different static and dynamic characteristics of devices and gate drivers [26, 27]. Hence, the voltage equalization circuits are needed to protect the switching

devices and enhance the system reliability.

1.2.4 Drive System Requirements

The general requirements of MV drive are low manufacturing cost, high efficiency and reliability, small physical size, easy installation, fault protection, and minimum downtime for repairs [28]. In addition, the MV drive should meet various application requirements such as high dynamic response, regenerative braking capability, and four-quadrant operation [29].

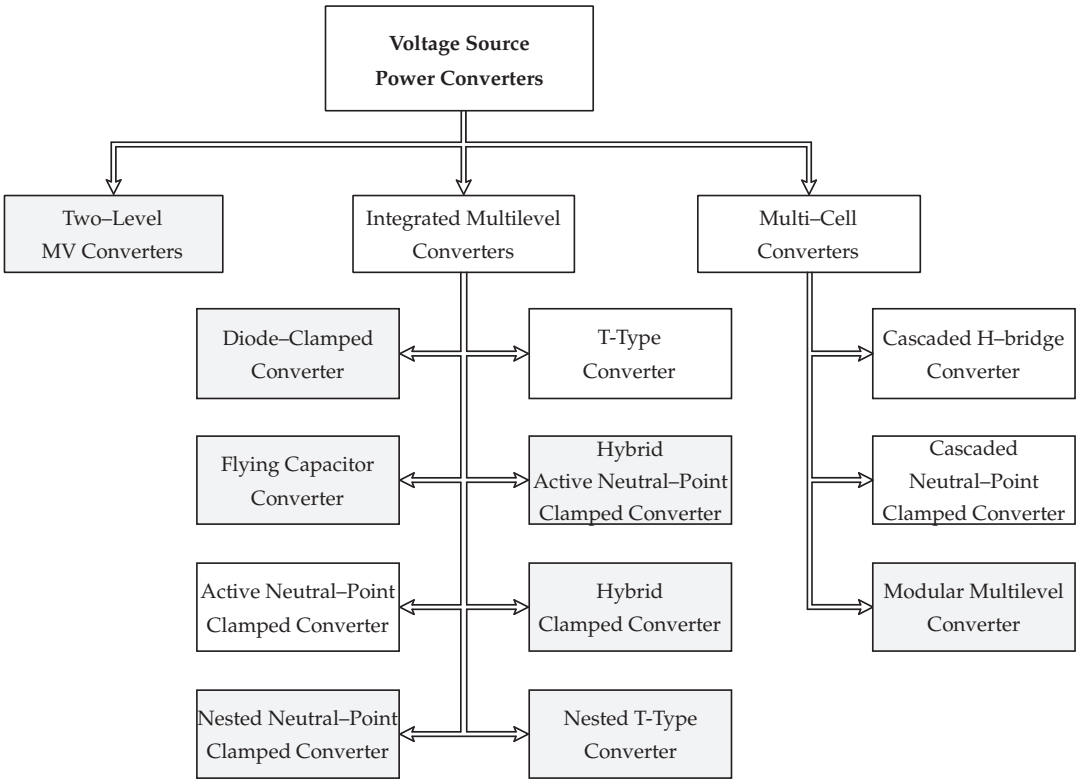


Figure 1.4. Classification of voltage source power converters for MV drives.

1.3 Power Converters for MV Drive

The power converters play a key role in the development of high-performance MV drives. These converters are categorized into current source converters (CSCs) and voltage source converters (VSCs) depending on the DC-link filter. Among them, the VSC technology is highly matured and exhibited higher market penetration compared with CSC technology [30].

Some of the developments in VSC technology are shown in Fig. 1.4. The two-level (2L) converter is a standard VSC, and it is widely used for low-voltage (LV) and low-power applications. For high-power applications, the 2L-VSC requires either devices in parallel to increase the current carrying capacity at LV operation or devices in series to achieve MV operation at low current carrying capacity [31]. The latter approach is highly preferred due to the availability of semiconductor devices and the reduction of power losses as shown in Fig. 1.5. However, this approach does not reduce the dv/dt, CMV, and power quality on the motor-side. Furthermore, they need output LC filters to meet the motor-side requirements, but it causes LC resonance problem. Also, the voltage equalization circuits are needed to ensure the equal voltage sharing among the devices during blocking mode [32].

On the other hand, the power converters which use low-cost semiconductor devices; known as multilevel converters are developed for high-power applications. These converters effectively meet the MV drive requirements including low dv/dt and harmonic distortion, low common-mode voltage, high efficiency due to low switching losses, elimination of output filters and series connection of devices [33]. There are several developments in multilevel converter technology, and they are categorized into integrated and multi-cell converters depending on their structure. The integrated multilevel converters are available in three-level (3L) to five-level (5L) operation and can handle an operating voltage of 2.3–4.16 kV. These converters need either a significant amount of modifications or step-up transformer to increase their operating voltage, and it is not cost-effective. Also, they have a longer down-

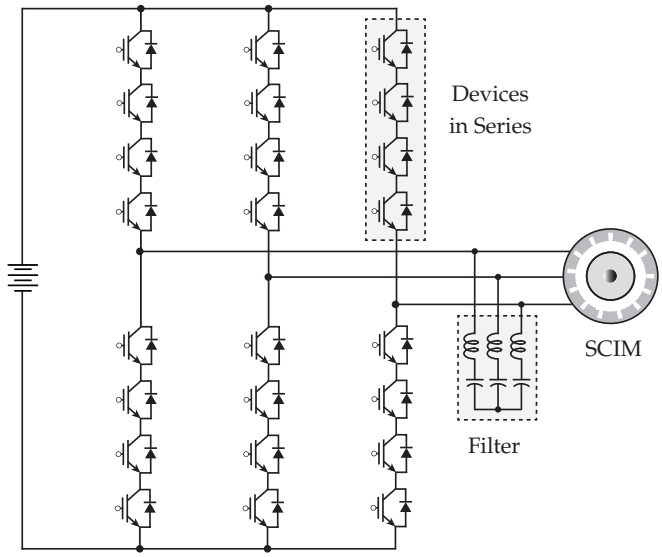


Figure 1.5. Two-level converter fed MV drive.

time under faults leading to a loss of production and revenue [34]. Some of the integrated multilevel converters are diode-clamped converter (DCC), flying capacitor converter (FCC), active neutral-point clamped (ANPC) converter, nested neutral-point clamped (NNPC) converter, T-type converter, hybrid ANPC converter, hybrid clamped converter (HCC), and nested T-type converter [35].

The multi-cell converters have a modular structure and can reach an operating voltage up to 13.8 kV. Moreover, the multi-cell converter output voltage levels are easy to increase by connecting identical modules in series. Also, they can continuously operate with reduced capacity even under faults [9]. Some of the popular multi-cell converters are cascaded H-bridge (CHB) converter, cascaded neutral-point clamped (CNPC) converter, and modular multilevel converter (MMC) [36]. Among them, the CHB and CNPC converters are available in odd voltage level operation. These topologies require isolated DC sources, which are generated with the help of multiple secondary phase-shifting transformer and rectifier system. The transformer increases the physical size and cost of the system [37]. On the other hand, MMC can reach an operating voltage up to 400 kV without transformer, and it does not

require isolated DC sources. Also, MMC is suitable for fault-tolerant operation, and reduce dv/dt and harmonic distortion without output filters [38]. However, it requires a large number of semiconductor devices and passive components.

This thesis mainly focused on the four-level (4L) operation of integrated and multi-cell converters, and their limitations and challenges for MV drive applications.

1.3.1 Diode Clamped Converter

Diode clamped converter (DCC) is one of the most popular and established standard multilevel converters. It is commercially available in three-level with an operating voltage of 2.3–3.3 kV. For higher operating voltages, the DCC requires a higher number of output voltage levels to meet the motor-side requirements [39]. Fig. 1.6 shows the 4L-DCC fed MV drive, which generates a voltage waveform with four-levels of 0, $V_{dc}/3$, $2\,V_{dc}/3$, and V_{dc}. The number of clamping diodes, DC-link capacitors, and control complexity of DCC drastically increases with output voltage levels [40].

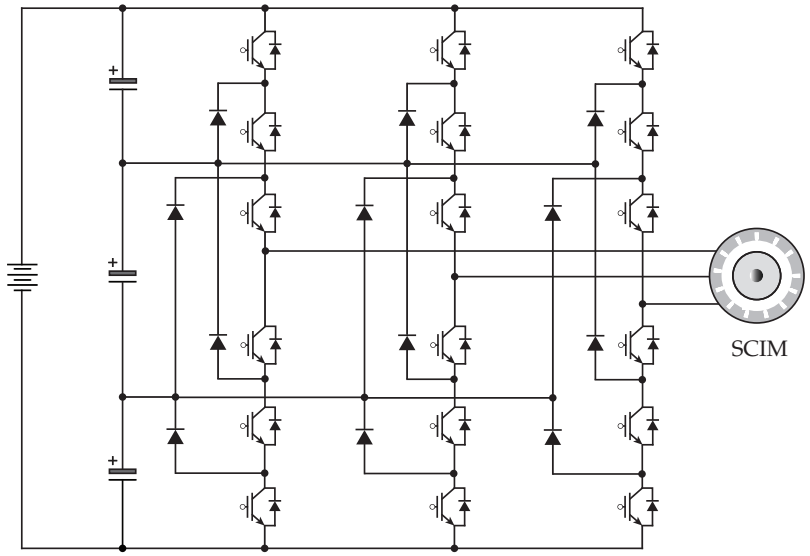


Figure 1.6. Four-level DCC fed MV drive.

The 4L-DCC consists of a DC-link with multiple neutral points, thereby it is not attractive for back-to-back operation. Also, it is difficult to achieve the DC-link voltage balancing with multi-carrier PWM schemes due to the lack of redundancy switching states [41]. This topology also exhibits unequal device power losses and requires a complex PWM scheme such as space vector modulation (SVM) scheme to overcome the above problems [42,43]. Thereby, the 4L-DCC is not commercially popular for more than three-level operation.

1.3.2 Flying Capacitor Converter

Fig. 1.7 shows the structure of a four-level flying capacitor converter (4L-FCC), in which each flying capacitor together with a pair of semiconductor devices form a power cell. The output voltage levels can be increased by adding power cells to the converter, thus it is considered as a modular structure converter [44]. Unlike 4L-DCC, the 4L-FCC topology does not require any clamping diodes, thereby the DC-link neutral points are eliminated to form a common DC-link bus for back-to-back operation.

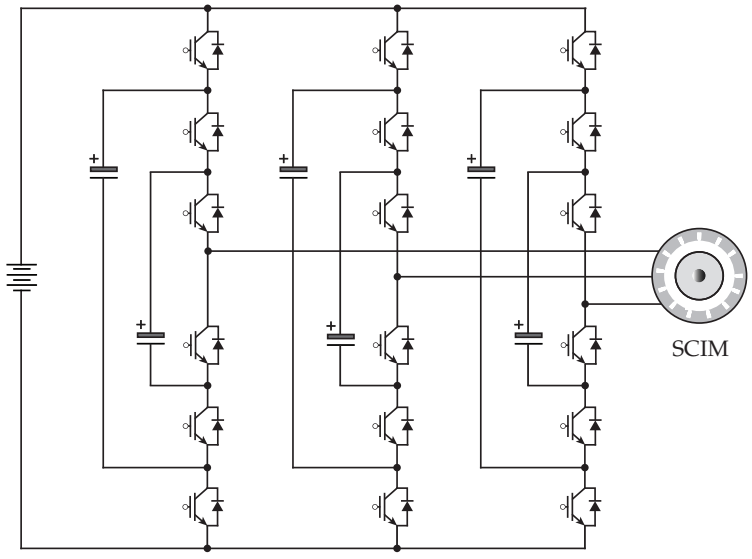


Figure 1.7. Four-level FCC fed MV drive.

The 4L-FCC requires two flying capacitors with different voltage ratings.

These capacitors have zero initial voltage and should be pre-charged during the startup process of the converter. Hence, the 4L-FCC needs additional pre-charging circuits or switching method to charge the flying capacitors [45]. In addition, it needs a voltage balancing method to regulate the flying capacitor voltages at their nominal values during steady-state [46, 47]. The natural balancing of voltage balancing can be achieved with a phase-shifted carrier PWM (PSC-PWM) scheme with high switching frequency [48]. In addition, the PSC-PWM scheme ensures equal loss distribution among the devices and makes the topology is more attractive for high-speed applications.

However, the capacitor voltage ripple at low-frequency operation is a severe issue in the 4L-FCC fed MV drive. These converters need either a large capacitance value or a high-switching frequency operation [49, 50]. The former solution increases the cost and physical size of the system, whereas the latter solution increases the power losses and affects the system efficiency. These issues limit the 4L-FCC to the medium switching frequency applications only. The 4L-FCC is commercially available for traction and water pump applications.

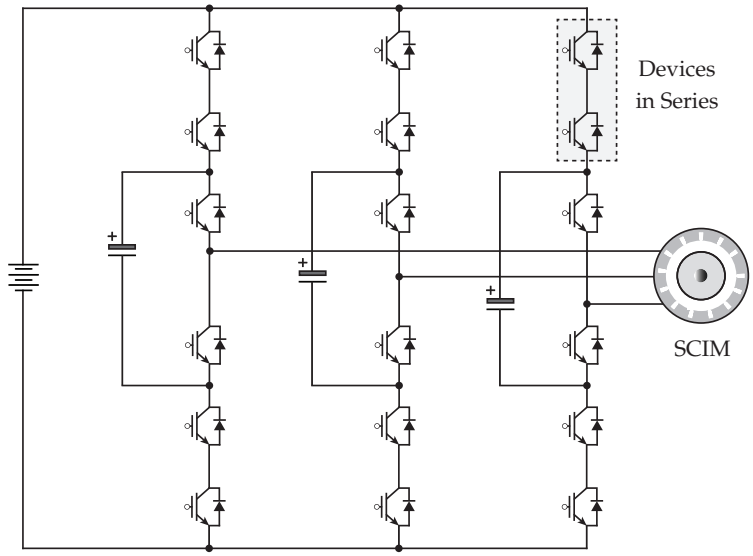


Figure 1.8. Four-level SFCC fed MV drive.

The outer flying capacitors in the conventional 4L-FCC topology are eliminated and resulting in a new topology named as a four-level single flying capacitor converter (4L-SFCC) as shown in Fig. 1.8. The elimination of flying capacitor improves reliability, and reduce the cost and physical size of the converter. However, this approach leads to the series-connection of switching devices and causes the device voltage sharing problems [51]. Also, the 4L-SFCC loose the redundancy switching states and increases the complexity of flying capacitor voltage balancing capability with conventional multicarrier PWM scheme [52].

1.3.3 Nested Neutral-Point Clamped Converter

Fig. 1.9 shows the structure of a four-level nested neutral-point clamped converter (4L-NNPC). This topology combines the structure of DCC and FCC, where the clamping diodes split the flying capacitors into two equal parts as shown in Fig. 1.9. The 4L-NNPC uses an identical rating of clamping diodes, semiconductor devices, and flying capacitors, thereby its manufacturing and maintenance cost is low [53].

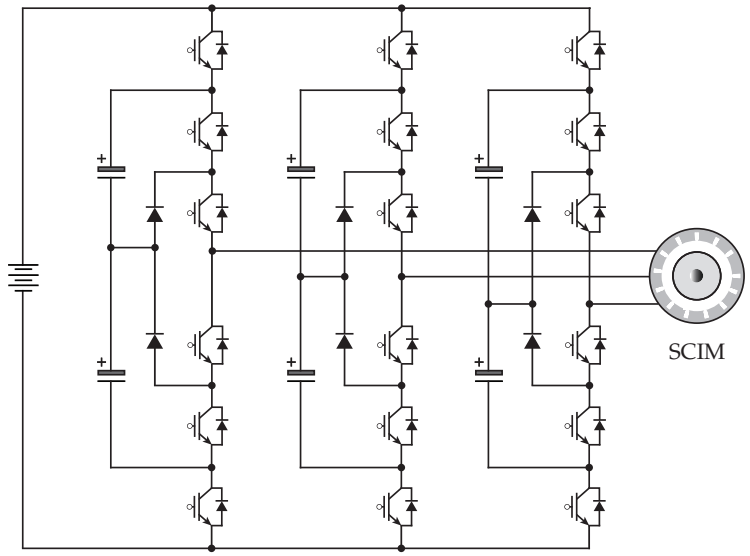


Figure 1.9. Four-level NNPC converter fed MV drive.

In addition, the 4L-NNPC has redundancy switching states to achieve the voltage balancing with multi-carrier PWM schemes. However, the balancing capability is limited to higher power factors and fundamental frequency only [54]. Furthermore, the flying capacitor voltage ripples are quite high during low-frequency operation [55]. Several modified PWM schemes based on the carrier and space vector philosophies are developed to improve the balancing capability while minimizing capacitor voltage ripple at low-frequency operation [56, 57]. However, these methods increase the device switching frequency leading to higher switching power losses and poor converter efficiency.

1.3.4 Hybrid Active Neutral-Point Clamped Converter

The structure of a four-level hybrid active neutral-point clamped converter (4L-HANPC) is shown in Fig. 1.10. This topology requires a lesser number of switching devices and no need of clamping diodes and flying capacitors. Unlike DCC topology, the DC-link neutral points in HANPC converter are formed with active semiconductor devices and require DC-link neutral point voltage balancing only [58].

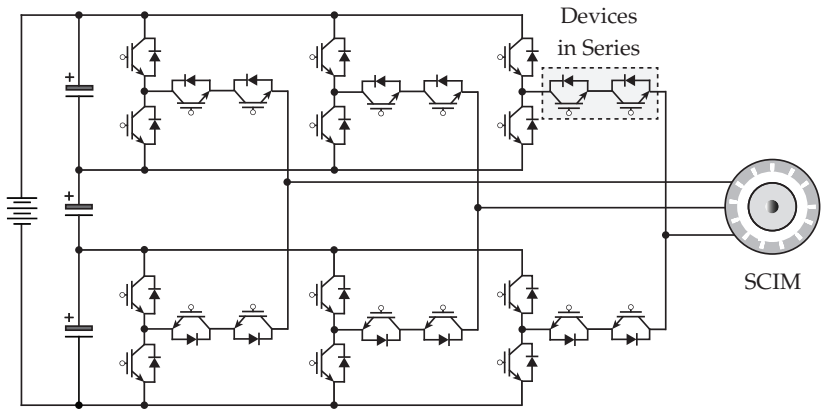


Figure 1.10. Four-level HANPC converter fed MV drive.

Due to the lack of redundancy switching states, it is difficult to achieve DC-link voltage balancing with conventional multi-carrier PWM schemes.

The zero-sequence voltage injection with a modified carrier PWM scheme is developed to control the DC-link capacitor voltages. However, the injected zero-sequence voltage increases the converter CMV magnitude leading to the failure of bearing and winding insulation. In addition, the 4L-HANPC require a series-connection of switching devices to manufacture the converter with identical voltage rating devices [58]. This will lead to voltage sharing problems and require additional voltage equalization circuits.

1.3.5 Hybrid Clamped Converter

The hybrid clamped converter (HCC) is realized by connecting a flying capacitor across the series connected switches in each phase of the HANPC converter. Fig. 1.11 shows the configuration of a 4L-HCC fed MV drive system. Due to the presence of flying capacitors, the series-connection of devices will be eliminated, and there is no need of voltage equalization circuits.

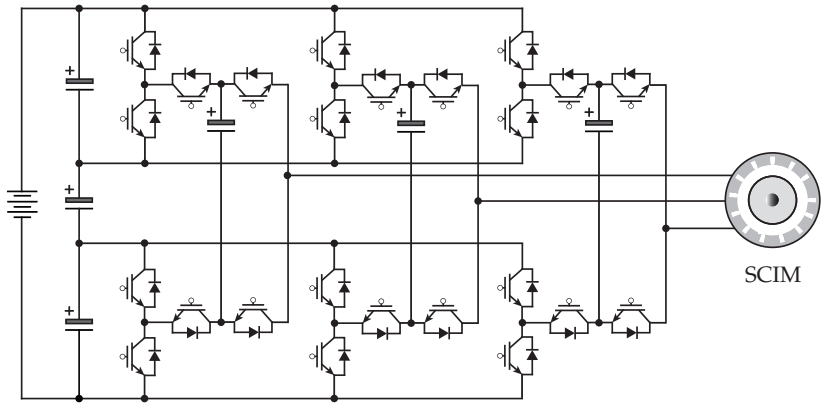


Figure 1.11. Four-level HCC fed MV drive.

Unlike HANPC, the redundancy switching states are available in HCC for flying capacitors voltage regulation [59]. However, the need of additional voltage sensors to measure flying capacitors voltage will increase the converter cost and affect its reliability. The flying capacitors have higher voltage ripples at low-frequency operation, which will be minimized by injecting common-mode voltage [60]. The injected common-mode voltage is also used

to regulate the DC-link neutral point voltage similar to the HANPC [61]. The injected common-mode voltage increases the voltage stress on the winding insulation and leading to its failure over a long run.

1.3.6 Nested T-type Converter

Fig. 1.12 shows the structure of a four-level nested T-type converter [62]. This topology combines the structure of FCC and T-type converter, where the anti-series connection of semiconductor devices splits the flying capacitors into two equal parts as shown in Fig. 1.12. The anti-series connection of devices needs voltage equalizing circuits to ensure equal voltage sharing during blocking mode. The nested T-type converter does not require clamping diodes and it uses identical voltage rating of semiconductor devices and flying capacitors only [63]. Thereby, it is easy to manufacture and conduct maintenance during faults.

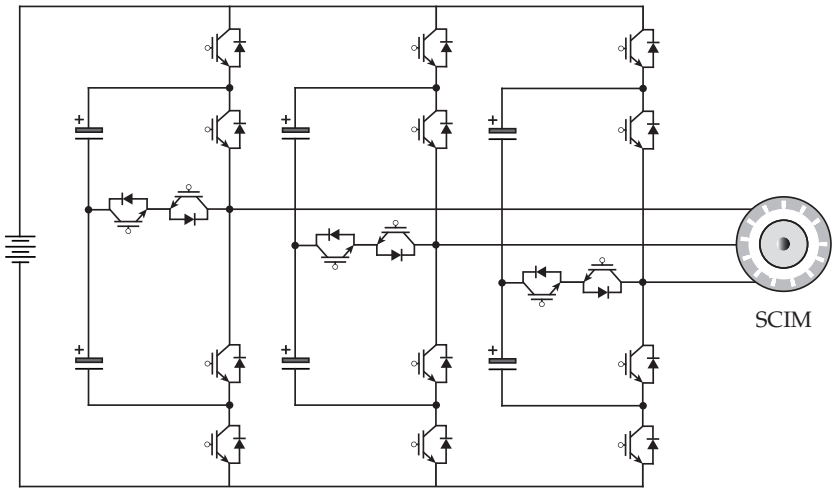


Figure 1.12. Four-level nested T-type converter fed MV drive.

The control philosophy of nested T-type converters is similar to 4L-NNPC, where the redundancy switching states are utilized to achieve the flying capacitor balancing with multi-carrier PWM scheme [53]. However, the voltage balancing capability is limited to higher power factors and fundamental fre-

quency. In addition, the nested T-type converter has a voltage ripple problem under the low-frequency operation, which make them less attractive for MV drive applications. The predictive control methods are investigated for low-frequency operation of nested T-type converter. Even though, these methods are highly effective but they cause variable switching frequency operation which is not desirable for high-power MV drives [64].

1.3.7 Modular Multilevel Converter

Fig. 1.13 illustrates the structure of modular multilevel converter (MMC). Modular multilevel converter is one of the most promising topologies for medium to high-voltage (HV) and high-power applications. Some of the main features are modular construction, voltage and power scalability, fault-tolerant operation with submodule (SM) redundancy, and direct connection to HV networks without line-frequency transformers [65]. These features attracted a wide range of industry applications including high-voltage direct current (HVDC) transmission, motor drives, power quality, railway power supplies, wind energy, and photovoltaic systems [66]. Each phase of MMC is realized by connecting identical SMs in cascade, and these modules does not require any isolated DC sources unlike CHB topology. Moreover, it is possible to use various SM configurations to realize MMC depending on the application requirements [67].

On the other hand, design constraints, SM capacitor voltage control, minimization of circulating currents, SM capacitor voltage ripple, and SM capacitor pre-charging process are the major technical challenges associated with the operation and control of MMC [68]. Hence, MMC requires a complex control system to achieve these control objectives. Moreover, MMC requires a larger number of semiconductor devices and passive components, which will increase the cost and affect the system reliability and efficiency. Besides, when applied in MV drives, the MMC suffers from low-frequency fluctuation in the SM floating capacitors [69, 70]. The high-frequency circulating current and common-mode voltage are injected into the system to minimize

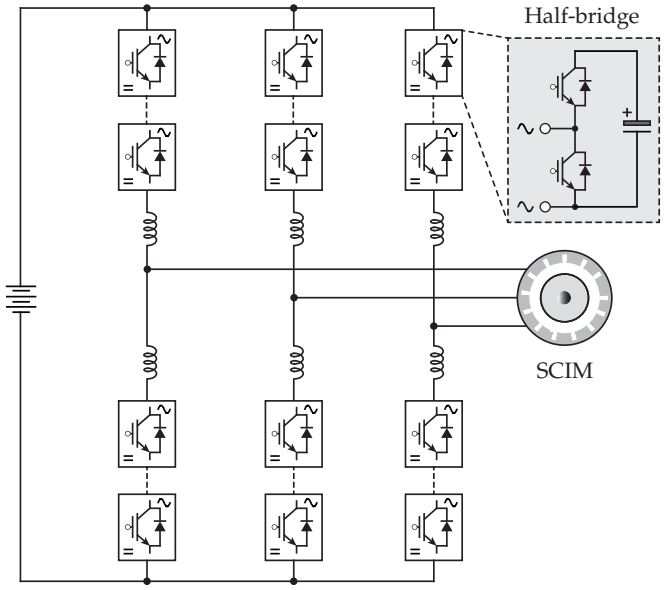


Figure 1.13. Four-level MMC fed MV drive.

the low-frequency fluctuation [71, 72]. This leads to higher device current stress and power losses along with an increase in voltage stress on motor winding. Hence, the MMC is not an attractive solution for MV drives.

1.4 Pulse Width Modulation Schemes

Pulse width modulation (PWM) schemes play a key role in generating AC output voltage with adjustable magnitude and frequency. This is achieved by controlling the turn-on and turn-off process of the switching devices in the power converters. In AC drives, the PWM schemes are selected based on the machine type, power level, type of switching devices used in the power converters, performance, and cost [73]. Furthermore, the PWM schemes are designed to achieve control objectives of AC drives such as power converters DC-link/flying capacitor voltage balancing, drive common-mode voltage minimization, and output power quality improvement.

PWM schemes have been an intensive research topic during the past few

years, and several methods are developed to meet the MV drive requirements. Some of the popular PWM schemes are carrier-based PWM, space vector modulation (SVM), selective harmonic elimination (SHE), staircase modulation, and optimal PWM methods [25]. Among them, the carrier-based PWM and SVM schemes are widely used for MLC-fed MV drive applications due to the ease of digital implementation, flexibility in switching vector selection, and excellent steady-state and dynamic response.

1.4.1 Multi-carrier PWM Schemes

The carrier PWM scheme is also referred to as sine-triangle PWM, and it is well established for two-level converters. In this scheme, the three-phase modulation signals are compared with a single triangular carrier signal to generate the gating signals for the switching devices in two-level converters. This approach is relatively easy to implement using digital control platforms [74]. The carrier PWM schemes are extended to multilevel converters and they are referred to as multi-carrier PWM schemes. In this approach, the three-phase modulation signals are compared with multiple triangular carrier signals to generate the gating signals for the switching devices in multilevel converters. The multi-carrier PWM schemes are categorized into level-shifted carrier (LSC-PWM) and phase-shifted carrier (PSC-PWM) PWM depending on the carrier arrangement [75,76].

The LSC-PWM is further categorized into phase-disposition (PD-PWM), phase-opposition disposition (POD-PWM), and alternate phase-opposition disposition (APOD-PWM) schemes [75]. Among them, the PD-PWM generates output voltage with the lowest harmonic distortion compared to POD-PWM and APOD-PWM schemes. However, the LSC-PWM schemes do not have natural flying capacitor voltage balancing capability and cause uneven loss distribution among the devices. Recently, the modified LSC-PWM schemes are studied, focusing on low-frequency operation, even loss distribution, and natural voltage balancing of MLC flying capacitors [77,78]. However, these methods increase the effective switching frequency of the converter leading

to higher switching losses.

On the other hand, the PSC-PWM scheme can achieve natural voltage balancing capability with high carrier frequency and is widely studied for multi-cell converters [79, 80]. With an optimal selection of phase-shift, it is possible to achieve harmonic cancellation with PSC-PWM thereby the output power quality of MLCs can be improved [81–83]. However, the higher carrier frequency increases the effective switching frequency of the converter. Moreover, the elimination/minimization of drive common-mode voltage is difficult to achieve with multi-carrier PWM schemes.

1.4.2 Space Vector Modulation Schemes

Space vector modulation (SVM) is one of the preferred real-time modulation schemes and is widely used for the digital control of two-level and multilevel converters. The SVM scheme allows the direct control of converter line-to-line voltages, which in turn produces the phase voltages [84]. SVM has the flexibility of selecting the best switching vector from the redundant switching vectors, which can be used to achieve multiple control objectives such as DC-link/flying capacitor voltage control, elimination/minimization of common-mode voltage, and minimization of switching frequency [85, 86].

Furthermore, the SVM provides better DC-link bus utilization and harmonic performance compared with carrier PWM schemes [87]. However, the SVM is quite difficult to implement for more than three-level converters due to the presence of a large number of switching vectors. There are several simplified multilevel SVM methods in abc-coordinates, gh-coordinates, and two-level SVM-based philosophy are developed to address the computational complexity issues. The simplified SVM methods do not involve the selection of redundancy switching vectors, hence these methods will loose the inherent features of conventional multilevel SVM [88–92].

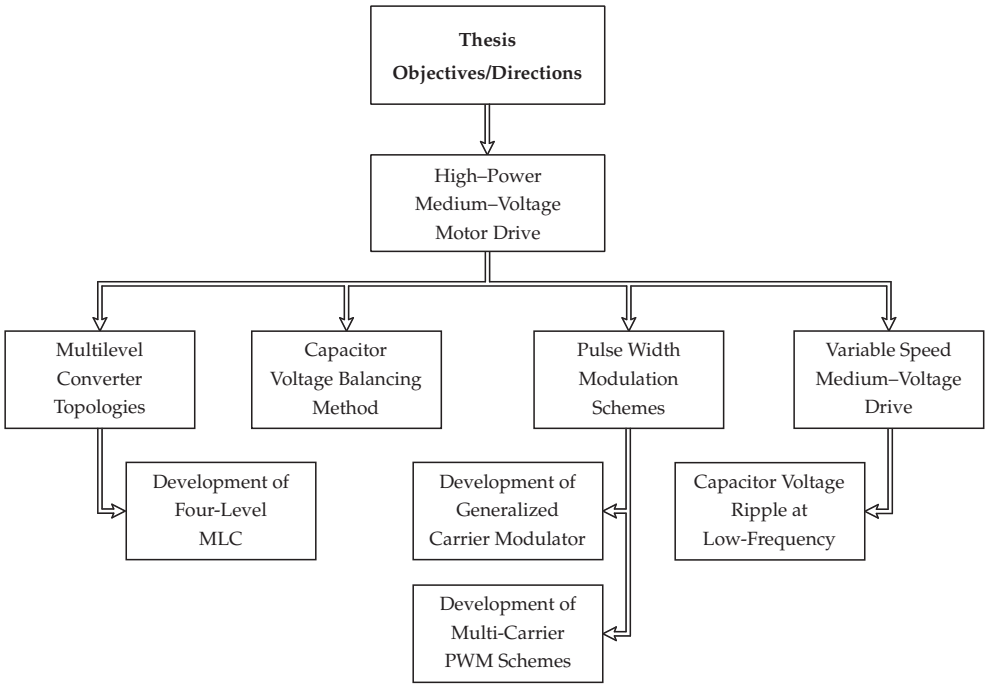


Figure 1.14. Summary of thesis directions/objectives.

1.5 Thesis Objectives

Aforementioned technical issues and requirements of high-power multilevel converters and MV drives are addressed in this thesis. The research objectives and contributions of this thesis are summarized in Fig. 1.14. The first problem addressed in this thesis is the development of a four-level multilevel converter (4L-MLC) to handle an operating voltage up to 4.16 kV without using the transformer and series connection of switching devices. The second important aspect is the development of high-performance voltage balancing methods with reduced complexity for 4L-MLCs. The third aspect is the development of a generalized pulse width modulator to integrate the voltage balancing method with different carrier-based PWM schemes to control the 4L-MLC. Finally, the challenges associated with the low-speed operation of MV drives are addressed through the development of a modified pulse width modulation scheme. The main contributions of this thesis are as follows:

1) Research on Four-Level Multilevel Converter Topologies for MV Applications

The existing 4L-MLCs need a series-connection of devices, which leads to device voltage sharing problems. These converters have a complex structure with a large number of semiconductor devices, clamping diodes, and flying capacitors. Hence, their manufacturing and maintenance cost are quite high. Also, the existing MLCs need a complex control scheme due to the lack of redundancy switching states. Some of the topologies have multiple DC-link neutral points, which makes them less attractive for back-to-back operation.

Considering the above issues, a new 4L-MLC without a series-connection of devices is proposed for MV applications. Hence, the proposed topology does not require voltage equalization circuits. It also requires a lesser number of semiconductor devices and flying capacitors, and they do not need any clamping diodes. Furthermore, the proposed topology has redundancy switching states, which can be used to achieves the voltage balancing objective. Hence, it does not require a complex control system. Moreover, the proposed topology is suitable for back-to-back operation due to the presence of a common DC-link.

2) Research on Voltage Balancing Methods for 4L-MLCs

In the existing 4L-MLCs, the DC-link/flying capacitor voltage balancing is necessary for reliable operation. The voltage balancing is achieved at the modulation stage with zero-sequence voltage injection or by using an external balancing method with redundancy switching states. The former method increases the load voltage stress leading to their premature failure over a long run. The latter method balancing capability is limited to higher power factors and fundamental frequency only. In addition, the existing methods cause unwanted device switchings leading to higher switching frequency operation, thereby higher switching power losses in the converter.

Considering the above issues, a new voltage balancing method is proposed for 4L-MLC. The proposed method uses redundancy switching states

to achieve the balancing of flying capacitors voltage. This method does not cause unwanted device switchings unlike existing methods. Moreover, its balancing capability is extended to low power factors and low fundamental frequencies as well. The proposed method is designed such that it can be implemented with both multi-carrier PWM and SVM schemes.

3) Research on Pulse Width Modulation Schemes for 4L-MLCs

Multi-carrier PWM and SVM schemes are the preferred choices for MLC control. Among them, the multi-carrier PWM schemes are widely used and easy to implement for 4L-MLC compared with SVM scheme. However, there is no unique structure of pulse width modulator in the literature to study the various multi-carrier arrangements for 4L-MLC. The carrier arrangement directly affects the converter output voltage and current harmonic distortion, and flying capacitor voltage ripple.

Considering the above issues, an unique structure of the pulse width modulator is proposed to control the 4L-MLC. With the proposed structure, it is easy to integrate the proposed voltage balancing method and study the performance of various multi-carrier arrangements for 4L-MLC.

4) Research on Low-Speed Operation of MV Drives

Several industrial applications need MV drives with the capability of developing rated torque under a wide range of rotational speeds. In MV drives, the power converters generate AC voltages/currents with adjustable magnitude and frequency at the motor terminals, thereby the motor rotational speed and torque production is varied as per the load requirements. The quality of output AC voltages/currents directly depends on flying capacitor voltage ripple, which in turn causes motor speed and torque ripple leading to a poor load performance. To achieve high-performance MV drive, it is necessary to limit the converter flying capacitor voltage ripple (peak-to-peak) within 5% of their nominal voltage.

Considering the above issues, a modified multi-carrier PWM scheme is proposed to keep the flying capacitor voltage ripple within its limits throughout the MV drive operation. By doing so, the converter generates voltage/current waveforms with a less harmonic distortion, which in turn leads to a smaller ripple in motor speed and torque. The field-oriented control (FOC) in the rotor flux reference frame is applied to achieve the closed-loop control of motor speed/torque and flux in the proposed 4L-MLC fed MV drive system.

1.6 Thesis Outline

The research presented in this thesis is organized into four chapters. The research outline of the thesis is summarized in Fig. 1.15. The work carried out in each chapter is summarized as follows:

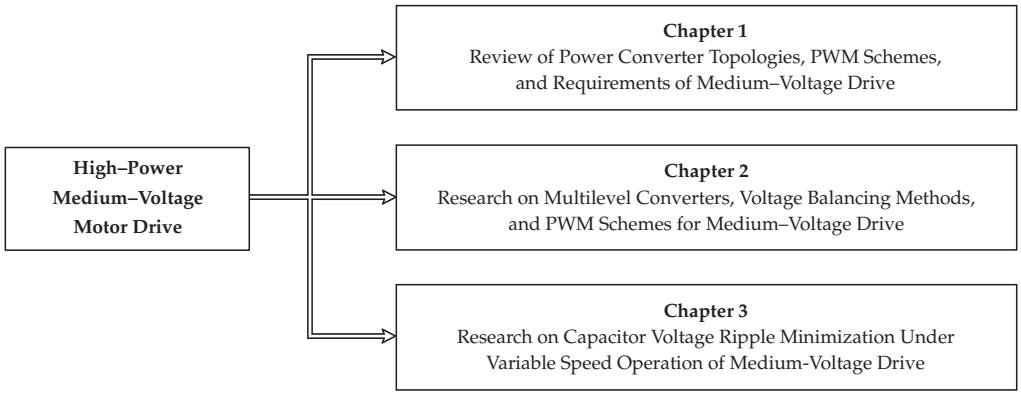


Figure 1.15. Summary of the thesis.

- **Chapter-1:** In this chapter, the fundamentals of MV drives and their requirements are presented. Also, the existing four-level multilevel converters, pulse width modulation schemes and their issues are discussed. Finally, the research objectives and outline of this thesis are presented.

- **Chapter-2:** In this chapter, a new 4L-MLC is proposed for MV applications. Also, a new voltage balancing approach along with a simple pulse width modulator structure is proposed. The dynamic and steady-state performances of the proposed balancing approach are verified on 4L-MLC with the PD-PWM scheme. To handle low-frequency operation, a modified carrier PWM is scheme is proposed and its performance is compared with the PD-PWM scheme.

- **Chapter-3:** In this chapter, a new 4L-MLC fed MV drive is proposed. A modified multi-carrier PWM scheme is proposed to limit the flying capacitor voltage ripple within 5% of their nominal voltage. Finally, the FOC scheme is implemented to achieve closed-loop control of motor speed/torque and flux. The start-up, steady-state and dynamic performances of the MV drive are presented with modified multi-carrier PWM scheme.

- **Chapter-4:** The main contributions and conclusions of this thesis are summarized in this chapter. The future directions to the research presented in this thesis are also suggested.

CHAPTER 2

VOLTAGE BALANCING AND MODULATION OF FOUR-LEVEL MULTILEVEL CONVERTER

MULTILEVEL converters (MLCs) have significant advantages compared with two-level converters at medium-voltage operation. These converters generate high-quality output voltage with low dv/dt, output current with a smaller ripple, and low common-mode voltage (CMV). MLCs have higher energy conversion efficiency and use low-cost and low-voltage semiconductor technology to handle medium-voltage (MV) operation. Furthermore, the MLCs use a smaller size of output filters (if needed) due to their superior harmonic performance [36, 37, 39, 93].

In this chapter, a new four-level MLC (4L-MLC) without a series connection of switching devices is proposed for MV applications. The new MLC uses flying capacitors to achieve multilevel operation. These flying capacitors are pre-charged to their nominal values during start-up operation and maintained at their nominal values during normal operation. To achieve the voltage balancing, a simple balancing method based on logical functions is proposed for 4L-MLC. This method guarantees the voltage balancing without an increasing device switching frequency and eliminates the unwanted device switchings compared with existing methods. In addition, a simple carrier-based pulse width modulator is developed to implement the

balancing approach with different carrier arrangements. The steady-state and dynamic performances of the proposed 4L-MLC and voltage balancing approach are verified through simulation studies. The conventional carrier PWM scheme leads to a larger capacitor voltage ripple at low-frequency operation. In this chapter, a modified carrier PWM scheme is proposed to reduce the capacitor voltage ripple at low-frequency operation. The simulation studies are presented to verify the effectiveness of the proposed modified carrier PWM scheme.

2.1 New Four–Level Multilevel Converter

The circuit configuration of a new four-level multilevel converter (4L-MLC) and its operation and switching states are discussed in the following subsections. Also, the detailed comparison of new 4L-MLC with existing multilevel converters is presented.

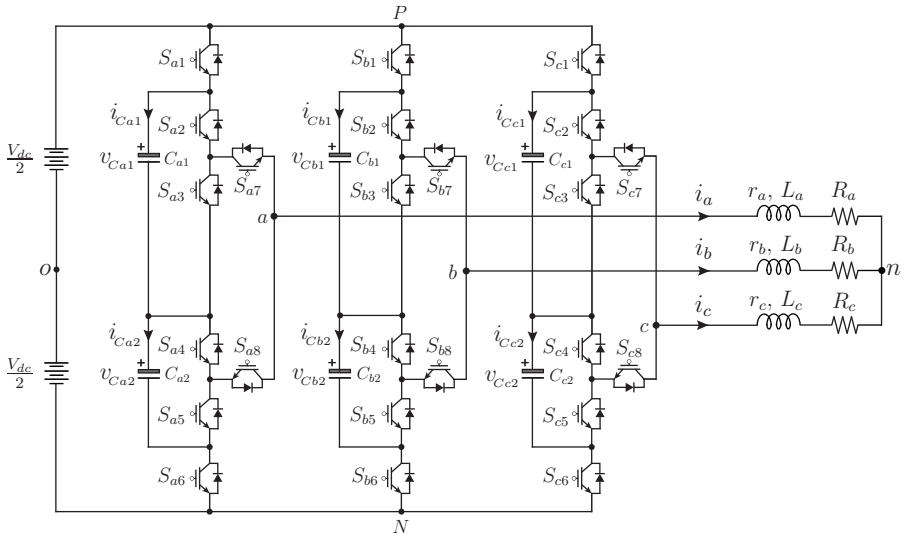


Figure 2.1. Proposed 4L-MLC with a passive load.

2.1.1 Converter Configuration

The configuration of the proposed 4L-MLC connected to a passive load is shown in Fig. 2.1. Each phase of the proposed topology is designed with eight switching devices (S_{x1}–S_{x8}) of $V_{dc}/3$ rating each, and two flying capacitors (C_{x1}–C_{x2}) with a nominal voltage of $V_{dc}/3$ each, where $x \in \{a, b, c\}$ denotes the phase. In the proposed 4L-MLC, the switching devices are not connected in series, hence the voltage equalization circuits are not needed. The positive (P) and negative (N) DC-link terminals are connected to a DC-source of V_{dc} rating. The DC source is divided into two equal parts and its midpoint is denoted as o. The three-phase AC terminals of the proposed 4L-MLC are connected to a balanced three-phase star-connected passive load. Each phase of the passive load is realized using a series connection of resistive (R_x) and inductance (L_x) with internal resistance (r_x) as shown in Fig. 2.1.

Table 2.1. Switching states of a new 4L-MLC

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	v_{xN}	**Level (S_x)**	**State**
1	1	0	0	0	0	1	0	V_{dc}	**3**	**D**
0	1	0	0	0	1	1	0	$2V_{dc}/3$	**2**	**C2**
1	0	1	0	0	0	1	0			**C1**
1	0	0	0	1	0	0	1	$V_{dc}/3$	**1**	**B2**
0	0	0	1	0	1	0	1			**B1**
0	0	0	0	1	1	0	1	0	**0**	**A**

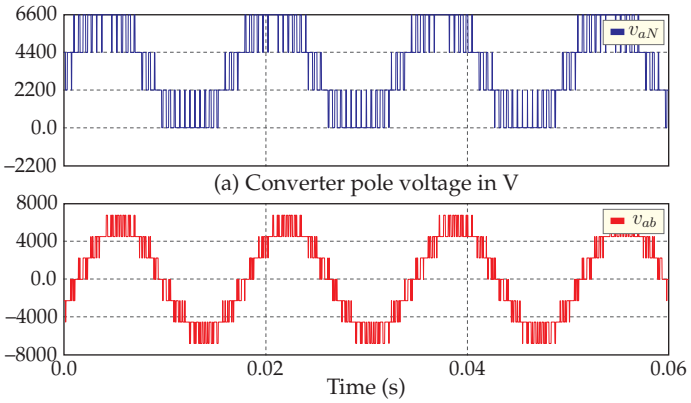
2.1.2 Operation and Switching States

The proposed 4L-MLC consists of six switching states per phase as shown in Table. 2.1. These switching states generate four distinct output voltages of 0, $V_{dc}/3$, $2V_{dc}/3$, and V_{dc} at their AC terminals corresponding to four output voltage levels of **0**, **1**, **2**, and **3**, respectively. The output phase voltage is defined as the voltage at the output terminal with respect to the negative bus (N) of the DC-link. The relationship between output phase voltage (v_{xN}) and voltage level ($\mathbf{S_x}$) can be expressed as

$$v_{xN} = \mathbf{S_x}\frac{V_{dc}}{3} \tag{2.1.1}$$

As shown in Table 2.1, the output voltage levels **0** and **3** do not have any redundant switching states, whereas the voltage levels **1** and **2** both have two redundant switching states. The redundant switching states **B1** [00010101] and **B2** [10001001] will give the same output voltage of $V_{dc}/3$ with different ON and OFF switches. Similarly, the redundant switching states **C1** [10100010] and **C2** [01000110] will give the same output voltage of $2\,V_{dc}/3$ with different ON and OFF switches. These redundant switching states will be employed in achieving flying capacitor voltage balancing, thereby the proposed 4L-MLC can generate a four-level voltage waveform with a step of $V_{dc}/3$.

Fig. 2.2 shows the voltage waveform of the new 4L-MLC at a modulation index (m_a) of 0.99 and fundamental frequency (f_o) of 60 Hz. Apparently, the pole voltage waveform has consisted of four levels with a step of $V_{dc}/3$ = 2200 V. This voltage is measured between phase terminal and the negative bus of DC-link. On the other hand, the line-to-line voltage has seven levels with a step of $V_{dc}/3$ = 2200 V. It is proven that the switching states given in Table 2.1 are valid and can produce four-level voltage waveform at output terminals of 4L-MLC.



(a) Converter pole voltage in V

(b) Converter line-to-line voltage in V

Figure 2.2. Basic operation of 4L-MLC.

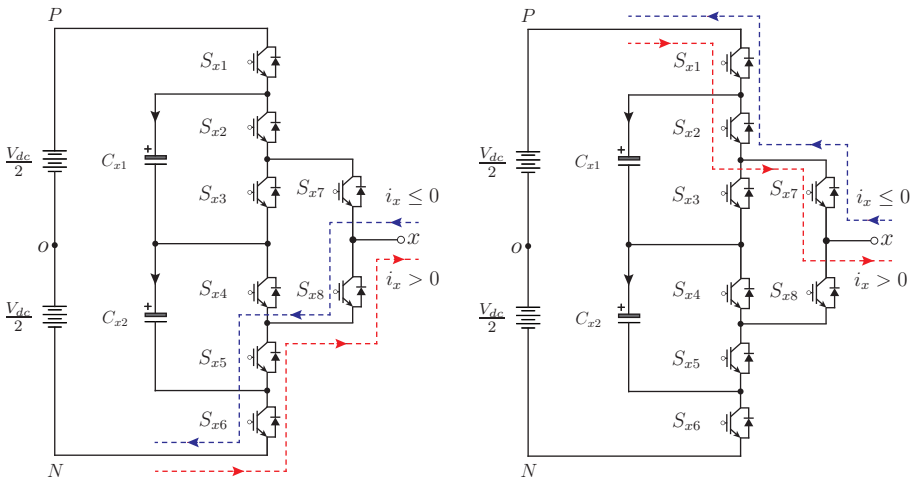
2.1.3 Analysis of Flying Capacitors Voltage

As shown in Table 2.2, each state has different impact on flying capacitors C_{x1} and C_{x2} voltages depending on the current direction. The analysis of these impacts are illustrated in Figs. 2.3, and 2.4, in which all the six switching states are analyzed. Each phase of the new 4L-MLC has two flying capacitors C_{x1} and C_{x2}, whose voltages are denoted by $v_{_{Cx1}}$ and $v_{_{Cx2}}$. The behavior of these flying capacitor voltages depends on the state $\mathbf{S_x}$ and phase current i_x.

For example, the switching states "**A**" and "**D**" corresponding to the voltage levels 0 and V_{dc} respectively do not have any impacts on the flying capacitors voltage as shown in Fig. 2.3. On the other hand, the switching "**B1**" corresponding to the voltage level $V_{dc}/3$ will discharge the flying capacitor C_{x2} for positive direction of current, whereas it will charge for negative direction of current, and there is no affect on the flying capacitor C_{x1} irrespective of the current direction as shown in Fig. 2.4. Similarly, the switching state "**B2**" will charge both flying capacitors C_{x1} and C_{x2} for positive direction of current, whereas they will discharge for negative direction of current. Hence, the direction of current plays a key role in the selection of redundancy switching states.

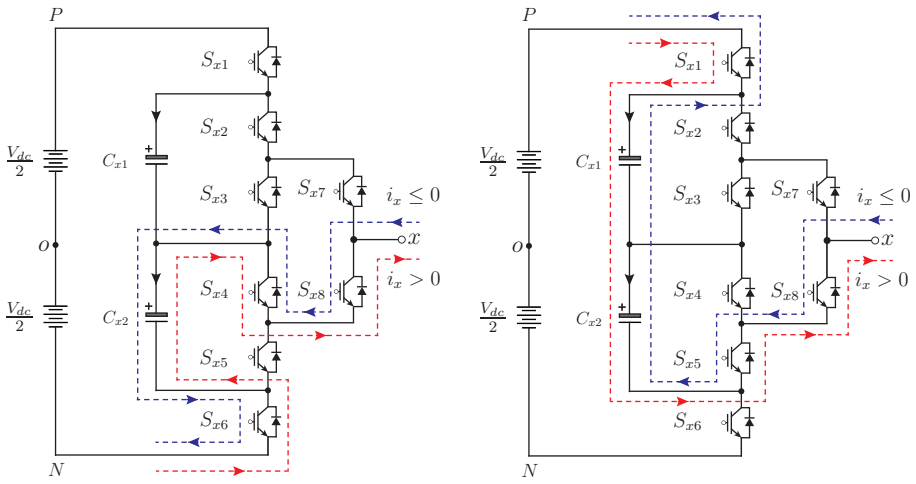
Table 2.2. Flying capacitors voltage variation

Level (S_x)	v_{xN}	**State**	v_{Cx1}	v_{Cx2}
3	V_{dc}	**D**	No Impact	No Impact
2	$2V_{dc}/3$	**C2**	Discharge ($i_x > 0$) Charge ($i_x \leq 0$)	Discharge ($i_x > 0$) Charge ($i_x \leq 0$)
		C1	Charge ($i_x > 0$) Discharge ($i_x \leq 0$)	No Impact
1	$V_{dc}/3$	**B2**	Charge ($i_x > 0$) Discharge ($i_x \leq 0$)	Charge ($i_x > 0$) Discharge ($i_x \leq 0$)
		B1	No Impact	Discharge ($i_x > 0$) Charge ($i_x \leq 0$)
0	0	**A**	No Impact	No Impact



(a) **State = A** (b) **State = D**

Figure 2.3. Impact of states **A** and **D**, and phase current on flying capacitor voltages.



(a) **State = B1** (b) **State = B2**

Figure 2.4. Impact of states **B1** and **B2**, and phase current on flying capacitor voltages.

2.1.4 Comparison of 4L–MLCs

Table 2.3 illustrates the comparison of the proposed 4L-MLC with the existing four-level multilevel converter. Obviously, the proposed MLC requires only 24 switches, which is much lesser compared with the 4L-MMC of 36 switches. The new 4L-MLC requires a 33.33% lesser number of switches compared to 4L-MMC, thereby lowering the cost and size of the system. The proposed topology employs the same number of switches with the 4L-HCC and requires 33.33% higher number of switches compared with DCC, FCC, SFCC, NNPC, and NTC. In terms of clamping diodes, the proposed 4L-MLC does not require any clamping diodes compared with DCC and NNPC as shown in Table 2.3. Also, it requires a lesser number of flying capacitors compared with FCC and MMC.

A 3-ϕ, 3 kW, 208 V, 60 Hz proposed converter cost is compared with existing converters considering the IGBT module of SKM100GB12T4 ($55/module), gate driver of SKHI 22B H4 R ($100/module), clamping diodes of SKKD 75F12 ($45/module), and flying capacitors of EPCOS 2200 μF/450 V ($80/ca-

Table 2.3. Comparison of four-level converters

Topology	Number of Switches	Number of Diodes	Flying Capacitors	Components in Series	Common DC-link	Components Cost ($)
DCC	18	18	–	Yes	No	1800
FCC	18	–	9	Yes	Yes	2115
SFCC	18	–	3	Yes	Yes	1635
NNPC	18	6	6	No	Yes	2010
HANPC	24	–	–	Yes	No	1860
HCC	24	–	3	No	No	2100
NTC	18	–	6	Yes	Yes	1875
MMC	36	–	18	No	Yes	4230
MLC	**24**	**–**	**6**	**No**	**Yes**	2340

pacitor) as shown in Table 2.3. The proposed converter cost is much lesser than MMC, but it is slightly higher than other converter topologies. However, the proposed topology does not require series connection components unlike existing converters, and there is no issue of voltage sharing problems. Also, it has a common DC-link and is suitable for back-to-back operation. Although, the NNPC is relatively competitive with the proposed topology, NNPC consists of three types of different components, including clamping diodes, flying capacitors, and switching devices, whereas the proposed converter comprises two types of components, involving capacitors and switches. As a result, the proposed topology requires less variation of components, leading to reduced maintenance cost and control complexity of the system.

2.2 Level–Shifted Carrier Pulse Width Modulation Scheme

A wide range of modulation strategies has already been reported in the literature to control the multilevel converters. Among them, the carrier-based and space vector modulation (SVM) schemes are the most prevalent tech-

niques. Several approaches have been presented to depict the performances and efficiencies of the SVM method affecting the system under a few particular operating conditions. However, the carrier-based strategies will remain broadly adopted owing to their inherent simplicity and reduced computational requirements [87].

The triangular carrier signals can be arranged within the linear modulation range in either vertically or horizontally. The modulation scheme with a vertical disposition of carrier signals is referred to as level-shifted carrier pulse width modulation (LSC-PWM). The LSC-PWM requires $(m-1)$ triangular carriers, where m represents the voltage level of the converter. All triangular carrier signals have the same frequency and magnitude and are vertically disposed. The amplitude modulation index of the LSC-PWM is defined as

$$m_a = \frac{\widehat{V^*}_x}{\widehat{V}_{cr}\,(m-1)} \tag{2.2.1}$$

where $\widehat{V^*}_x$ is the peak magnitude of the sinusoidal reference signals and $\widehat{V}_{\text{cr}}$ is the peak magnitude of each carrier wave.

The LSC-PWM has three different variations named as; phase disposition (PD), alternative phase opposition disposition (APOD), and phase opposition disposition (POD). In this thesis, the phase disposition pulse width modulation (PD-PWM) scheme is employed because of giving the best harmonic profile over the two remaining methodologies. The implementation of LSC-PWM scheme for the proposed multilevel converter mainly consists of the following steps:

2.2.1 Generation of Modulation Signals

Fig. 2.5 illustrates the control block diagram of the proposed 4L-MLC. This methodology consists of various stages involving the generation of modulations signal, pulse width modulator, voltage level generation, and capacitor voltage balancing. In the present approach, the three-phase modulation signals (v_a^*, v_b^*, v_c^*) are constituted by the user with the required modulation

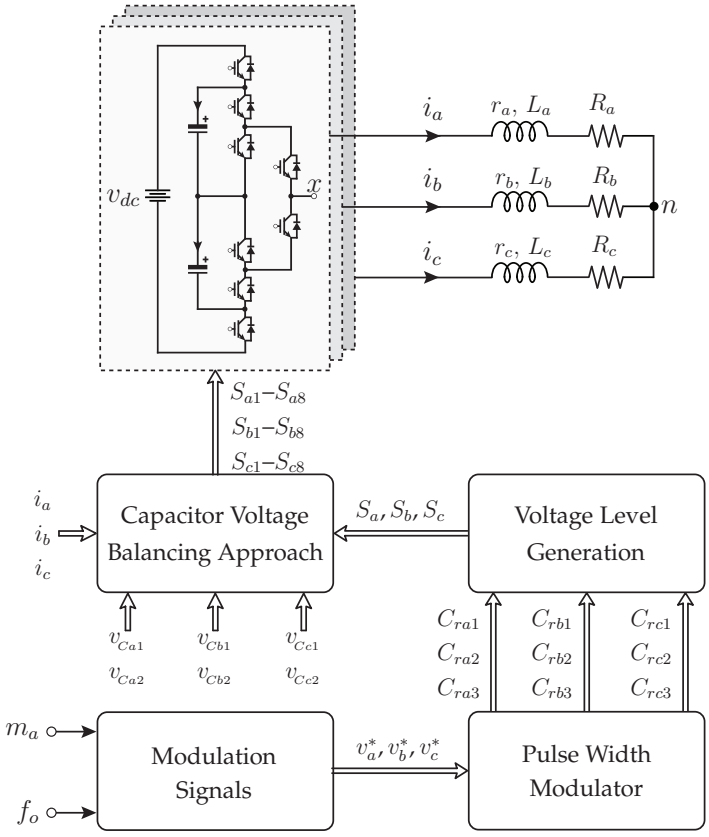


Figure 2.5. Control block diagram of the proposed 4L-MLC.

index (m_a), output frequency (f_o), and phase angle (θ_x). The mathematical expression of the modulation signal is given by,

$$v_x^* = m_a \cos(2\,\pi\, f_o\, t + \theta_x) \tag{2.2.2}$$

2.2.2 Generation of Carrier Signals

To apply the PD-PWM, the modulation scheme requires three triangular carrier signals ($m - 1 = 4 - 1 = 3$) as the proposed converter is the four-level converter. These carriers are generated with an amplitude of $\widehat{V}_{\text{cr}}$ and carrier frequency of f_{cr}, and they are vertically arranged with the same phase angle as shown in Fig. 2.6. The generated modulation signals and carrier signals are fed to the pulse width modulator.

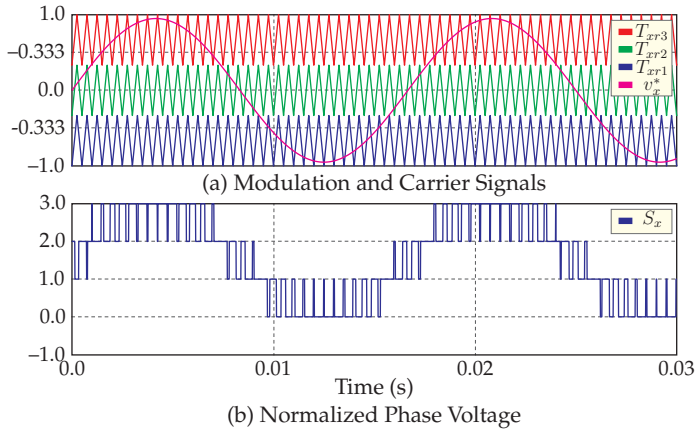


Figure 2.6. Representation of modulation and carrier signals in PD-PWM.

2.2.3 Pulse Width Modulator

The pulse width modulator is designed to generate the gating pattern for the switching devices in the proposed 4L-MLC. The modulation signals are compared with triangular carrier signals using pulse width modulator. The comparison of each phase modulation and carrier signal gives a virtual pulse (C_{rx1}–C_{rx3}). These virtual pulses are added together to realize the phase voltage level information S_x as shown in Fig. 2.6. The normalized voltage waveform is given as an input to the capacitor voltage balancing approach as shown in Fig. 2.5. The normalized voltage waveform has voltage levels of $0, 1, 2..., m$. The capacitor voltage balancing approach uses the measured output current to identify its direction and instantaneous value of capacitor voltage along with voltage level information in the selection process of redundancy switching state. The resultant switching state is applied to the converter which will generate the required output voltage at their AC terminals while maintaining flying capacitors voltage at their nominal values.

2.3 Voltage Balancing Method

The main objective of the voltage balancing approach is to control the charging and discharging period of flying capacitors by applying a proper switching state. The selection process of switching state requires current direction, deviation of instantaneous value of capacitor voltage, and voltage level information. Based on the available information, a simple voltage balancing approach is proposed for 4L-MLC, and its structure is shown in Fig. 2.7.

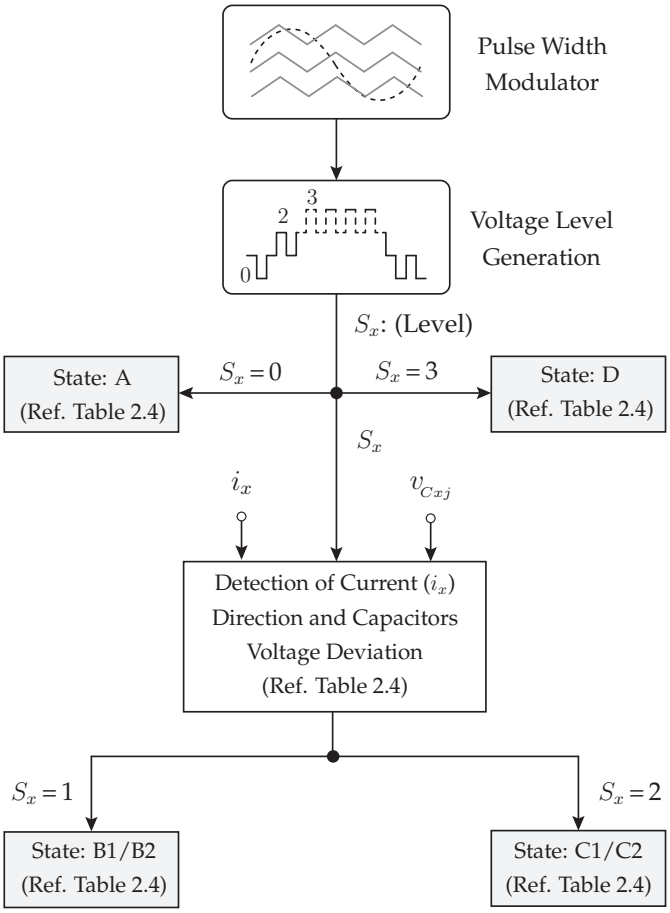


Figure 2.7. Implementation of the proposed voltage balancing approach.

2.3.1 Implementation of Voltage Balancing Method

The implementation of voltage balancing method involves following steps:

- Obtain the voltage level information (S_x) from voltage level generator;
- The voltage levels "**0**" and "**3**" do not have any redundancy switching states. Hence, the current direction and instantaneous value of capacitor voltage deviation are not required in the selection process of switching state.
- To generate voltage level "**0**", the device switching states corresponding to the state "**A**" are selected. In this state, the devices S_{x1}, S_{x2}, S_{x3}, S_{x4}, and S_{x7} are OFF, while the devices S_{x5}, S_{x6}, and S_{x8} are ON as shown in Table 2.1;
- On the other hand, the device switching states corresponding to the state "**D**" are selected and applied to the converter to generate a voltage level "**3**". In this state, the devices S_{x1}, S_{x2}, and S_{x7} are ON, while the devices S_{x3}, S_{x4}, S_{x5}, S_{x6}, and S_{x8} are OFF as shown in Table 2.1;
- The voltage levels "**1**" and "**2**" have two states each. To select the right state, the voltage balancing approach uses the current direction and capacitor voltage deviation as shown in Table 2.4. For example, if the voltage level is "**1**" and the current direction is positive ($i_x > 0$) then the device switching states corresponding to state "**B1**" are selected when the capacitor C_{x2} voltage deviation is positive ($\Delta V_{Cx2} \geq 0$). On the other hand, the device switching states corresponding to state "**B2**" are selected when the capacitor C_{x2} voltage deviation is negative ($\Delta V_{Cx2} < 0$) as shown in Table 2.4. Similarly, the states "**C1**" and "**C2**" are selected based on the criteria given in Table 2.4;
- During this process, the present voltage level is compared with the past voltage level sample. If they are equal then the balancing approach applies the device switching states corresponding to past sampling inter-

val during the present sampling interval irrespective of current direction and flying capacitors voltage deviation. Otherwise, the capacitor voltage balancing approach follows the above philosophy in the selection process of redundancy switching states corresponding to the new voltage level. By doing so, the unwanted switching actions will be eliminated such that the average device switching frequency is maintained approximately equal to the carrier frequency.

Table 2.4. Selection of redundancy switching states

S_x	**State**	$i_x > 0$	$i_x \leq 0$
3	**D**	–	–
2	**C2**	$\Delta v_{_{Cx1}} \geq 0$	$\Delta v_{_{Cx1}} < 0$
	C1	$\Delta v_{_{Cx1}} < 0$	$\Delta v_{_{Cx1}} \geq 0$
1	**B2**	$\Delta v_{_{Cx2}} < 0$	$\Delta v_{_{Cx2}} \geq 0$
	B1	$\Delta v_{_{Cx2}} \geq 0$	$\Delta v_{_{Cx2}} < 0$
0	**A**	–	–

Table 2.5. Simulation system parameters

Variable	Description	Simulation
S	Load apparent power (kVA)	5000
$v_{_{LL}}$	Load L-L RMS voltage (V)	4160
f_o	Frequency (Hz)	60
i	Load RMS current (A)	693.93
V_{dc}	Net DC-link voltage (V)	6600
$V_{_{Cxj}}$	Flying capacitor voltage (V)	2200
C_{xj}	Capacitance of flying capacitor (μF)	3000
L	Load inductance (mH)	1.8
R	Load resistance (Ω)	3.5
f_{cr}	Carrier frequency (Hz)	2000

2.3.2 Performance with Step Change in Modulation Index

Fig. 2.1 shows the system configuration under study and it is designed with the parameters given in Table 2.5. The designed system can handle a power capacity of 5 MVA and a voltage rating of 4.16 kV. The peak value of line-to-line voltage is given as $v_{LL,p} = \sqrt{2} * v_{LL} = \sqrt{2} * 4160 = 5883$ V. For a four-level inverter, the total DC-link voltage given as $V_{dc} = 1.122 * V_{LL,p} = 6600$ V. The net DC-link voltage of 4L-MLC is realized by using a constant DC source of 6600 V. The selection of the flying capacitor size can be given as follow: $C_{xj} = I_p/(f_{sw} * \Delta V_{cxj})$, where $j \in \{1, 2\}$ is the index number of flying capacitors, C_{xj} is the capacitance of the j^{th}-flying capacitor in phase-x, ΔV_{cxj} is the peak-to-peak flying capacitor voltage ripple, f_{sw} is the switching frequency, and I_p is the peak value of the output current. Typically, the capacitance of the flying capacitor is designed to limit the peak-to-peak flying capacitor voltage ripple within 5%-10% of nominal flying capacitor voltage. Based on the above formula, the calculated capacitance value is equal to (693.93*$\sqrt{2}$)/(2000*2200*0.075) = 2974 μF. Based on the availability of capacitors in the market, each flying capacitor with a capacitance of 3000 μF and nominal voltage of 2200 V is chosen. The proposed 4L-MLC is controlled with PD-PWM scheme. The PD-PWM requires three triangular carrier signals, which are generated with a frequency of 2000 Hz. The passive load is designed with a resistance of 3.5 Ω and an inductance of 1.8 mH.

The performance of the proposed 4L-MLC and voltage balancing approach with a step change in the modulation index is shown in Fig. 2.8. Initially, the modulation signals are generated with $m_a = 0.45$ and $f_o = 60$ Hz. The proposed 4L-MLC topology generates a line-to-line voltage waveform with 5-steps as shown in Fig. 2.8(a). The output voltage has a total harmonic distortion (THD) of 41.43% as shown in Table 2.6. The load draws balanced three-phase currents with a peak value of 430 A and these currents have a THD of 1.61% as shown in Fig. 2.8(b). The phase-a and -b flying capacitor voltages are shown in Fig. 2.8(c) and 2.8(d), respectively. Each flying capacitor voltage is regulated with an average value of 2200 V and they have a peak-to-peak

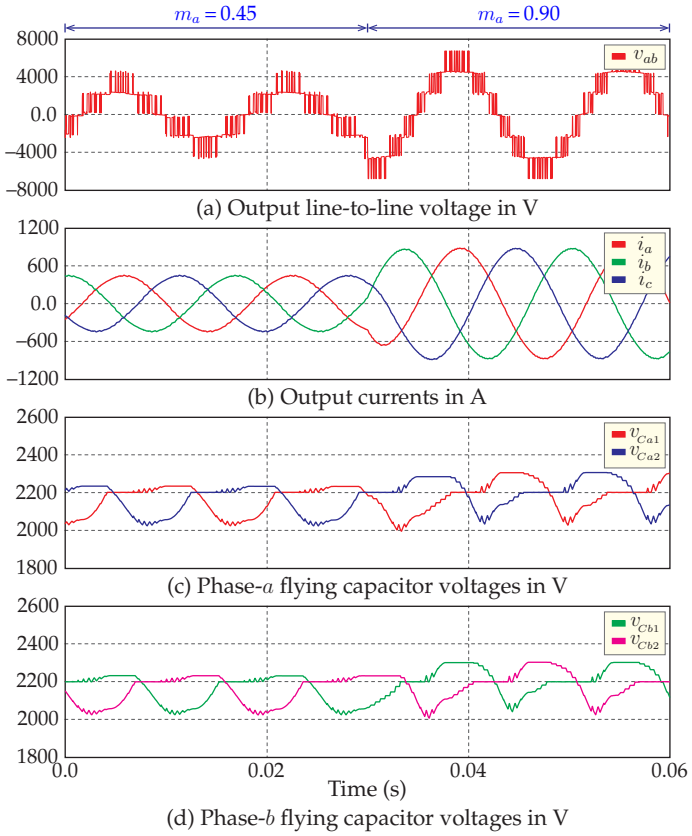


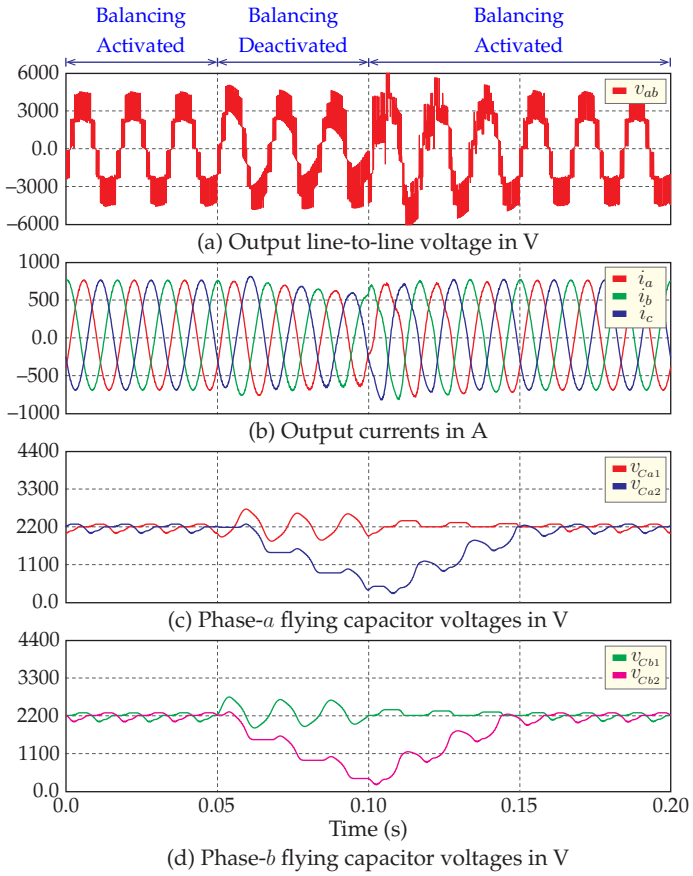
Figure 2.8. Step response with change in modulation index ($f_o = 60$ Hz and PF = 0.80 (lag)).

ripple of 201 V as shown in Table 2.6.

At $t = 0.03$ s, the modulation index is suddenly changed from 0.45 to 0.90 while maintaining $f_o = 60$ Hz. The output voltage has 7-steps and its THD is reduced to 23.66% as shown in Table 2.6. The load current magnitude is increased to 860 A due to the increase in voltage magnitude as shown in Fig. 2.8(b). The load current has a lesser ripple leading to a lower THD of 0.75%. Even though, there is an external disturbance but the flying capacitors of phase-a and -b are perfectly regulated at 2200 V with the help of the proposed voltage balancing approach. However, the flying capacitor voltage ripple is increased to 269 V due to the rise in current magnitude.

Table 2.6. Analysis with change in modulation index

m_a	$\%V_{THD}$	$\%I_{THD}$	$\Delta\, v_{cxj}$ (p-p)
0.45	41.43	1.61	201 V
0.90	23.66	0.75	269 V



(a) Output line-to-line voltage in V

(b) Output currents in A

(c) Phase-a flying capacitor voltages in V

(d) Phase-b flying capacitor voltages in V

Figure 2.9. Step response with and without balancing approach ($m_a = 0.75$, $f_o = 60$ Hz and PF = 0.80 (lag)).

2.3.3 Performance with and without Voltage Balancing

The performance of the proposed 4L-MLC topology is further investigated by activating and deactivating the voltage balancing approach for a short duration of time and corresponding results are shown in Fig. 2.9. In this study, the modulation signals are generated with $m_a = 0.75$ and $f_o = 60$ Hz. From

$t = 0$ s to 0.05 s, the voltage balancing is activated and the 4L-MLC generates a 5-steps voltage waveform with a step of 2200 V as shown in Fig. 2.9(a). The three-phase output currents are balanced and they have a peak value of 720 A as shown in Fig. 2.9(b). The phase-a and -b flying capacitor voltages are perfectly maintained at their nominal values of 2200 V as shown in Fig. 2.9(c) and 2.9(d), respectively.

At $t = 0.05$ s, the voltage balancing is deactivated. The converter output voltage waveform is highly distorted due to asymmetrical voltage steps. This leads to an increase in device voltage stress and causes their failure over a long time. The asymmetrical voltage stepped waveform forces distorted currents into the load as shown in Fig. 2.9(b). The flying capacitor voltages are diverged from their nominal values due to the absence of the voltage balancing approach. At $t = 0.1$ s, the voltage balancing is activated. The 4L-MLC operation becomes normal as it generates symmetrical stepped output voltage and balanced three-phase load currents. Also, the flying capacitor voltages are brought back to their nominal values of 2200 V with the help of the voltage balancing approach.

2.3.4 Performance with Step Change in Output Frequency

The performance of the proposed voltage balancing method is verified with a step change in output frequency as shown in Fig. 2.10. Initially, the modulation signals are generated with $m_a = 0.9$ and $f_o = 60$ Hz. The 4L-MLC generates an output voltage with a step of 2200 V and its THD is around 23.66% as shown in Table 2.7. The three-phase output currents are balanced and they have a lesser ripple leading to a THD of 0.75%. The phase-a and -b flying capacitor voltages are balanced around their nominal voltages of 2200 V as shown in Fig. 2.10(c) and 2.10(d), respectively. Each capacitor has a voltage ripple of 258 V as shown in Table 2.7.

At $t = 0.04$ s, the modulation signal frequency is changed from 60 Hz to 30 Hz. The change in frequency has no effect on the balancing of flying capacitors voltage, but their ripples are increased to 496 V as shown in Fig. 2.10(c)

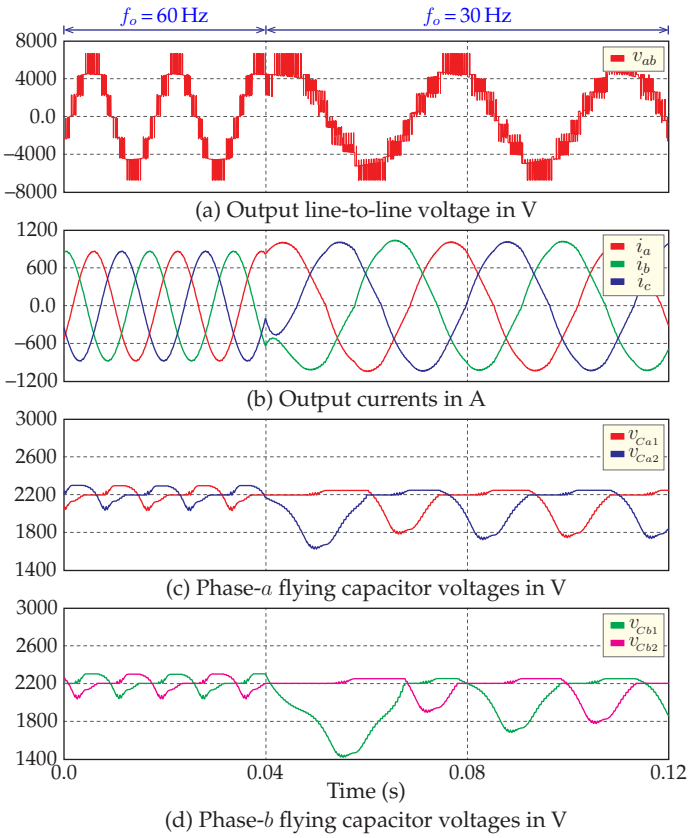


Figure 2.10. Step response with change in output frequency ($m_a = 0.9$ and PF = 0.80 (lag)).

Table 2.7. Analysis with change in fundamental frequency

f_o	$\%V_{THD}$	$\%I_{THD}$	$\Delta\, v_{cxj}$ (p-p)
60 Hz	23.66	0.75	258 V
30 Hz	23.32	2.11	496 V

and 2.10(d). The increase in voltage ripples causes higher distortion in output currents as shown in Fig. 2.10(b), and its THD is increased to 2.11% as shown in Table 2.7. These ripples have a little effect on the output voltage waveform quality and there is no much difference in output voltage THD as shown in Table 2.7.

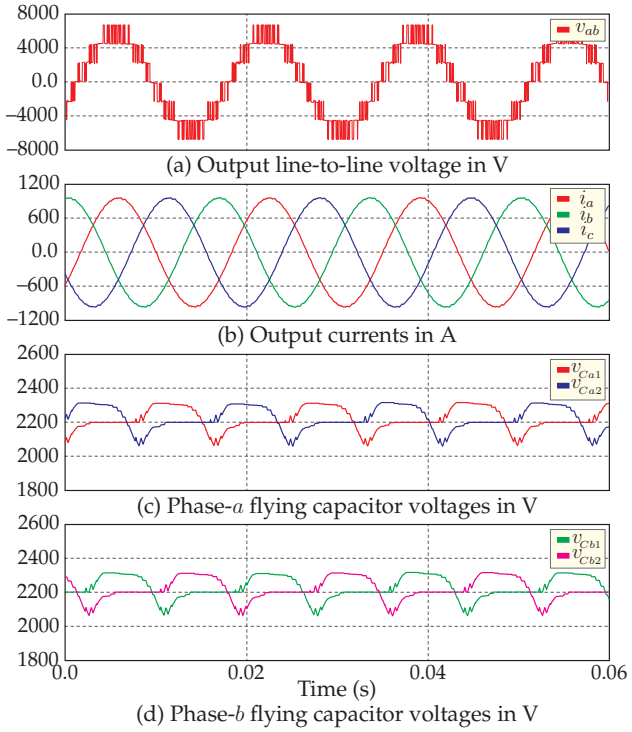


Figure 2.11. Steady-state response at $m_a = 0.99$, $f_o = 60$ Hz, and PF = 0.8 (lag).

2.3.5 Performance at Different Load Power Factors

The steady-state performance of the proposed 4L-MLC and voltage balancing approach at different load power factors is shown in Fig. 2.11 and 2.12. In this study, the modulation signals are generated with $m_a = 0.99$ and $f_o = 60$ Hz. The load power factor is adjusted by varying the load resistance and inductance values. At load power factor PF = 0.8 (lag), the 4L-MLC generates a 7-steps voltage waveform with a THD of 23.04% as shown in Fig. 2.11(a). The load draws balanced three-phase currents with a peak value of 950 A as shown in Fig. 2.11(b) and these currents have a THD of 0.81% as shown in Table 2.8. Each flying capacitor voltage in phase-a and -b is perfectly maintained at their rated value as shown in Fig. 2.11(c) and 2.11(d), respectively. Each flying capacitor has a peak-to-peak voltage ripple of 243 V as shown in Table 2.8.

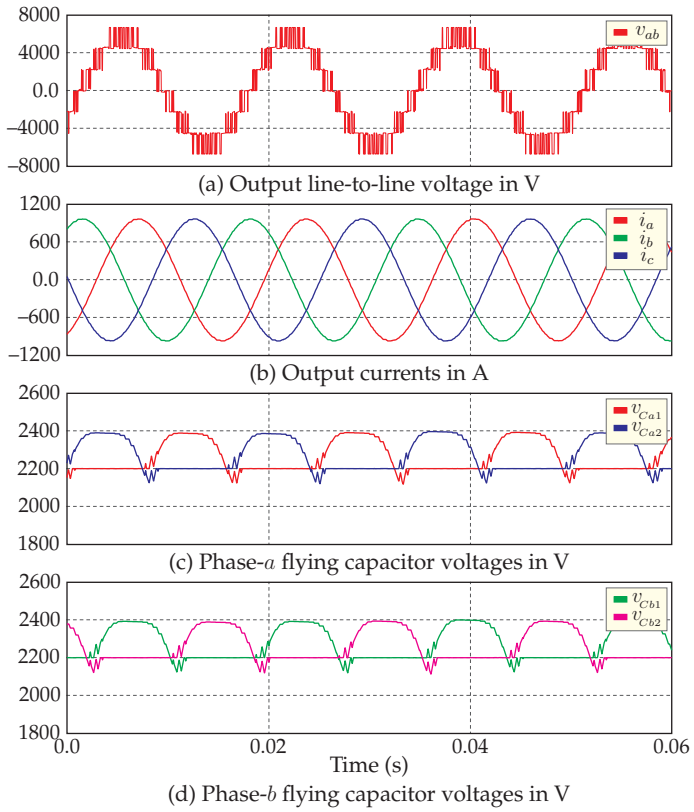


Figure 2.12. Steady-state response at $m_a = 0.99$, $f_o = 60$ Hz, and PF = 0.45 (lag).

Table 2.8. Analysis with change in load power factor

PF	$\%V_{THD}$	$\%I_{THD}$	$\Delta\, v_{cxj}$ (p-p)
0.80	23.04	0.81	243 V
0.45	22.92	0.53	256 V

Fig. 2.12 shows the simulation performance at load power factor 0.45, while operating the converter with the same modulation index and output frequency. The 4L-MLC generates a 7-steps voltage waveform with a THD of 22.92% as shown in Fig. 2.12(a). The load draws balanced three-phase currents with a peak value of 950 A as shown in Fig. 2.12(b) and the current THD reduced to 0.53% due to the increase in load inductance which acts as a filter. Each flying capacitor voltage in phase-a and -b is perfectly maintained at their rated value as shown in Fig. 2.12(c) and 2.12(d), respectively. The

flying capacitor voltage ripple increased to 256 V due to the increase in load reactive power demand.

2.4 Modified Carrier PWM Scheme

With the proposed voltage balancing method, the conventional PD-PWM scheme is effectively maintaining the flying capacitor voltages at their nominal values irrespective of the operating condition. However, the flying capacitor has a very large voltage ripple at low-frequency operation. These ripples cause a higher total harmonic distortion (THD) in the output current and increase the device voltage stress.

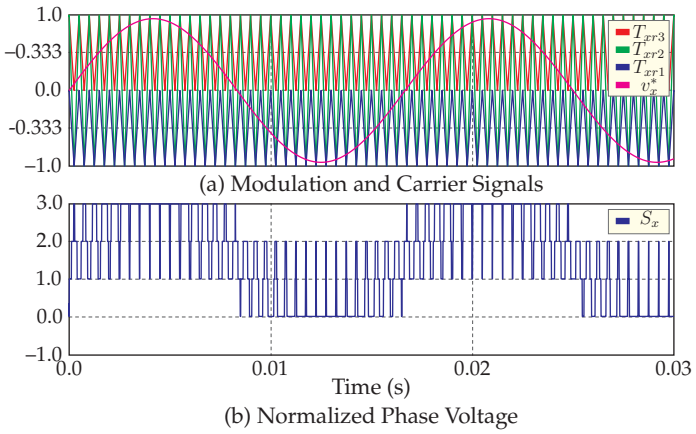


Figure 2.13. Representation of modulation and carrier signals in modified carrier PWM.

To minimize the flying capacitor voltage ripple, a modified carrier PWM scheme is proposed for a new 4L-MLC. The triangular carrier signals arrangement in the proposed modified carrier PWM is shown in Fig. 2.13(a). The proposed modified carrier PWM scheme also require three carrier signals to achieve the four-level operation with 4L-MLC. Among the three carriers, the upper and lower carrier signals are equally disposed in the linear operating range with the same magnitude and phase angle. On the other hand, the middle carrier signal is disposed in the same phase, but its magni-

tude is twice that of the upper/lower carrier signal as shown in Fig. 2.13(a). The modulation signal is compared with carrier signals and it results in a normalized phase voltage waveform as shown in Fig. 2.13(b). The normalized voltage waveform has multiple voltage levels jump and leading to an increase in the device switching frequency. The increase in device switching frequency effectively minimizes the flying capacitor voltage ripple in 4L-MLC. However, by applying the voltage balancing algorithm, the average switching frequency of the inverter is maintained at the carrier frequency.

2.4.1 Performance with Change in Modulation Index

The performance of the proposed 4L-MLC with modified carrier PWM under step change in the modulation index is shown in Fig. 2.14. Initially, the modulation signals are generated with $m_a = 0.45$ and $f_o = 60$ Hz. The proposed 4L-MLC topology generates a line-to-line voltage waveform with 5-steps as shown in Fig. 2.14(a). The output voltage has a total harmonic distortion (THD) of 47.68% as shown in Table 2.9. The output THD is increased by 15.08% compared with the conventional PD-PWM scheme. The load draws balanced three-phase currents with a peak value of 430 A and these currents have a THD of 1.22% as shown in Fig. 2.14(b). The output THD is decreased by 24.22% due to the reduction in capacitor voltage ripple. The phase-a and -b flying capacitor voltages are shown in Fig. 2.14(c) and 2.14(d), respectively. Each flying capacitor voltage is regulated with an average value of 2200 V and they have a peak-to-peak ripple of 49 V as shown in Table 2.9. With the modified carrier PWM, the ripples are decreased by 75.62%.

Table 2.9. Analysis with change in modulation index

m_a	$\%V_{THD}$	$\%I_{THD}$	Δv_{cxj} (p-p)
0.45	47.68	1.22	49 V
0.90	41.35	1.28	83 V

At $t = 0.03$ s, the modulation index is suddenly changed from 0.45 to 0.90 while maintaining $f_o = 60$ Hz. The output voltage has 7-steps and its THD

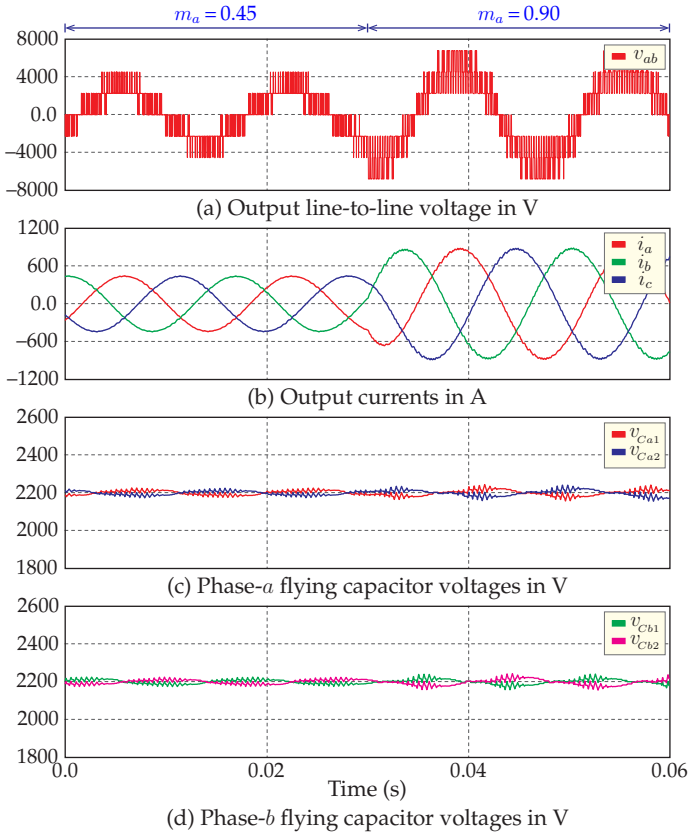


Figure 2.14. Step response with change in modulation index ($f_o = 60$ Hz and PF = 0.80 (lag)).

is increased to 41.35% as shown in Table 2.9. The load current magnitude is increased to 860 A due to the increase in voltage magnitude as shown in Fig. 2.14(b). The load current has a THD of 1.28%. The flying capacitor voltage ripple is increased to 83 V due to the rise in current magnitude.

2.4.2 Performance with Change in Output Frequency

The performance of 4L-MLC with modified carrier PWM scheme under a step change in output frequency as shown in Fig. 2.15. Initially, the modulation signals are generated with $m_a = 0.9$ and $f_o = 60$ Hz. The 4L-MLC generates an output voltage with a step of 2200 V and its THD is around 41.35%

as shown in Table 2.10. The output voltage is increased by 74.78% compared with PD-PWM. The three-phase output currents are balanced and they have lesser ripple leading to a THD of 1.28%. The phase-a and -b flying capacitor voltages are balanced around their nominal voltage of 2200 V as shown in Fig. 2.15(c) and 2.15(d), respectively. Each capacitor has a voltage ripple of 83 V as shown in Table 2.10. The voltage ripples are decreased by 67.83% compared with the PD-PWM scheme.

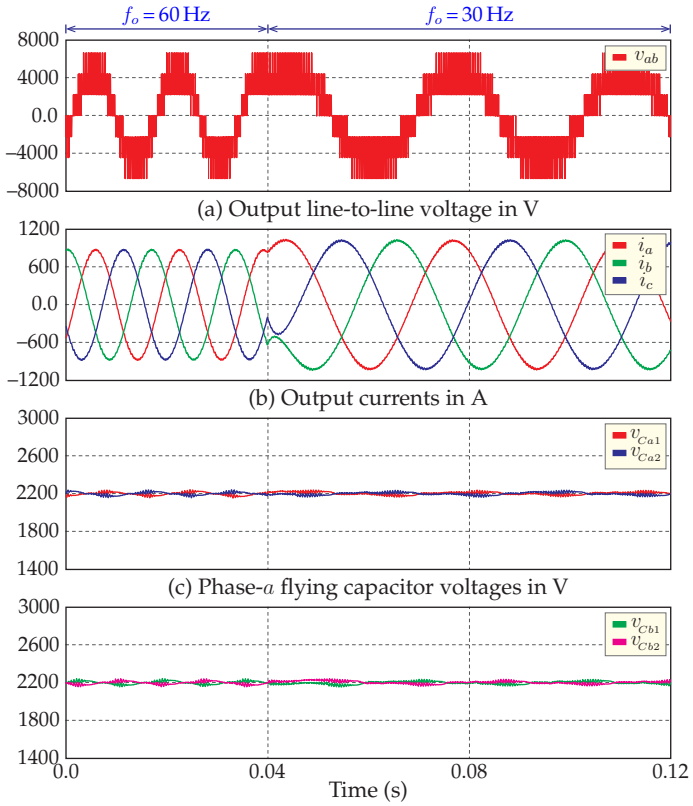


Figure 2.15. Step response with change in fundamental frequency ($m_a = 0.9$ and PF = 0.80 (lag)).

At $t = 0.04$ s, the modulation signal frequency is changed from 60 Hz to 30 Hz. The change in frequency has no effect on the balancing of flying capacitors voltage, but their ripples are decreased to 76 V as shown in Fig. 2.15(c) and 2.15(d). With the modified carrier PWM scheme, the capacitor voltage

ripples are decreased by 84.68% compared with the PD-PWM. These results show that the modified carrier PWM is capable of limiting the flying capacitor voltage ripple within 5% of their nominal during low-frequency operation. Thereby the output current distortion is reduced to 1.12% as shown in Table 2.10. These ripples have a little effect on the output voltage waveform quality and there is no much difference in output voltage THD as shown in Table 2.10.

Table 2.10. Analysis with change in output frequency

f_o	$\%V_{THD}$	$\%I_{THD}$	$\Delta\, v_{cxj}$ (p-p)
60 Hz	41.35	1.28	83 V
30 Hz	41.43	1.12	76 V

2.5 Summary

In this chapter, a new four-level multilevel converter (4L-MLC) is proposed for medium-voltage (MV) applications. The proposed topology is competitive in cost compared with existing four-level converters. Moreover, the proposed topology is attractive for MV applications due to the elimination of devices series connection, thereby the voltage equalization circuits are not needed. Also, it has a common DC-link and is suitable for back-to-back operation. In addition, a generalized carrier-based pulse width modulator along with a simple voltage balancing approach is proposed for 4l-MLC. The simulation results show that the proposed voltage balancing approach is highly effective in maintaining the flying capacitor voltages at their nominal values irrespective of the operating condition. However, the conventional carrier PWM scheme is unable to limit the flying capacitor voltage ripple within 5% of their nominal values under low-frequency operation. A modified carrier PWM scheme is proposed to minimize the capacitor voltage ripple in the 4L-MLC. The simulation results show the proposed approach is highly effective in limiting the capacitor voltage ripple within 5% of their nominal values under low-frequency operation.

CHAPTER 3

A NEW FOUR-LEVEL MULTILEVEL CONVERTER FED MEDIUM-VOLTAGE DRIVE

THE medium-voltage (MV) motor drives became popular due to the advent of multilevel converters. A number of MV drive products are available in the market today. These drives come with different power converter topologies and control schemes. Each drive offers some unique features but also has some limitations. Particularly, the variable speed operation with low torque ripple is one of the requirements for MV drives. The modern MV drives come with flying capacitor-based multilevel converters, and these converters have higher capacitor voltage ripples at low-speed and rated torque conditions. These ripples significantly affects the output currents, which in turn affect the motor torque and causes a higher torque ripple. In overall, the drive performance greatly depends on the converter topology and its control scheme.

In this chapter, a new four-level multilevel converter (4L-MLC) fed MV drive is proposed. The MV drive can handle an operating voltage up to 4.16 kV with the proposed 4L-MLC. The indirect field-oriented control (IFOC) is applied to control the speed/torque and flux in the proposed MV drive. The 4L-MLC has a very high flying capacitor voltage ripple at low-speed operation. To minimize the converter flying capacitor voltage ripple, a modified

carrier pulse width modulation scheme is employed with IFOC scheme. The simulation studies are presented to verify the performance of the proposed MV drive under start-up, transient, and low-speed conditions.

3.1 Fundamentals of 4L-MLC fed Motor Drive

In this section, the configuration of the proposed 4L-MLC fed motor drive system and its control schemes are discussed.

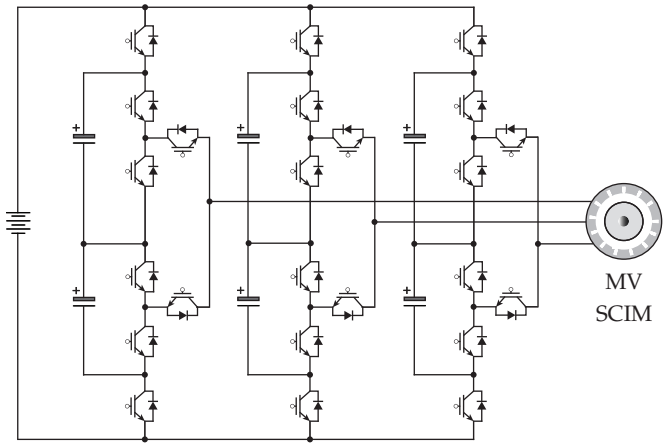


Figure 3.1. Proposed 4L-MLC fed MV drive.

3.1.1 System Configuration

In motor drive applications, the power conversion takes place in two stages. In the first stage, the AC grid supply is converted into DC supply using a rectifier. In the second stage, the DC supply is converted into variable-voltage, variable-frequency AC supply using an inverter. In the proposed drive system, there are two possibilities for the rectifier stage. The first possibility is to use a diode bridge converter. Another possibility is to use the proposed 4L-MLC in both rectifier and inverter stages. This kind of system is suitable for regenerative applications, and possible to control the grid power factor as well. In this work, the rectifier stage is replaced with a constant DC source,

whereas the converter AC terminals are connected to the medium-voltage (MV) squirrel-cage induction motor (SCIM) as shown in Fig. 3.1.

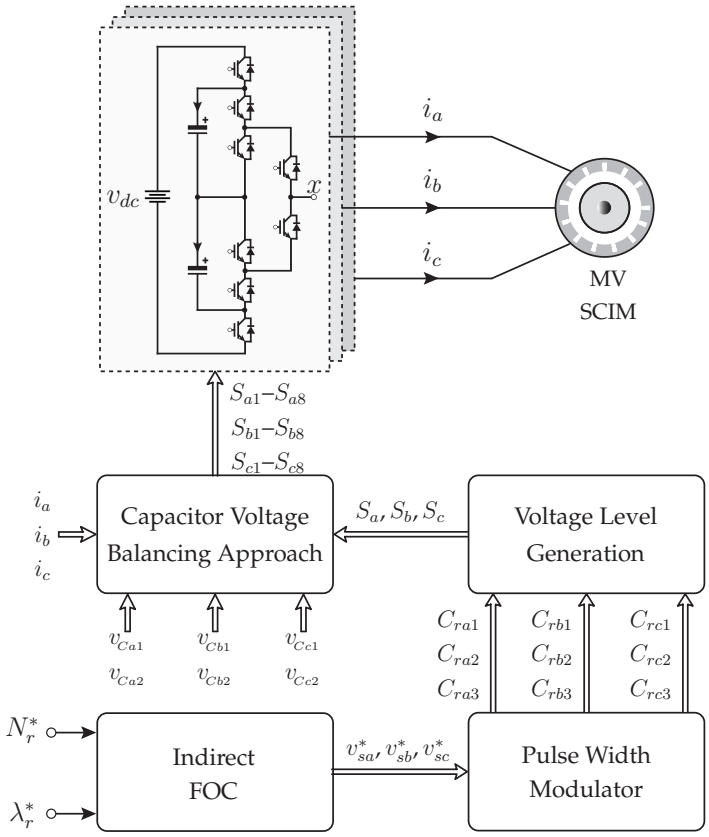


Figure 3.2. Control block diagram of the proposed 4L-MLC fed MV drive.

3.1.2 Drive Control Schemes

The 4L-MLC connected to an MV SCIM is shown in Fig. 3.1, in which the 4L-MLC is used to meet the drive requirements such as accurate control of speed/torque and flux. To achieve these objectives, several control methods such as direct field orientation control (DFOC), indirect field orientation control (IFOC), and direct torque control (DTC) methods are discussed in the literature [4]. These control methods are well established and used in commercial motor drive systems. In this work, the IFOC scheme is employed to

control the proposed 4L-MLC fed MV drive system as shown in Fig. 3.2.

3.2 Indirect Field Oriented Control

In this work, the DC-link voltage is maintained constant at the rated value of V_{dc} using a constant DC power source. The DC-link voltage is used to pre-charge the 4L-MLC flying capacitors to their nominal values of $V_{dc}/3$. These flying capacitors are controlled to generate variable AC voltage at the motor terminals depending on the motor speed/torque and flux demand.

The control block diagram of the 4L-MLC fed MV drive is shown in Fig. 3.2. This control scheme is implemented in the rotor flux reference frame, where the measured currents are transformed into rotor flux reference frame rotating at a speed of ω_s. The motor speed and rotor flux are controlled using the IFOC scheme. The actual speed/torque and the magnitude of flux and its position are obtained from the rotor/torque calculator. The IFOC controller generates reference modulation signals v^*_{sa}, v^*_{sb}, v^*_{sc}. These modulation signals are applied to the carrier pulse width modulator, which is implemented using a modified carrier PWM scheme. The resultant comparison of modulation and carrier signal is used together with the voltage balancing method to generate the device switching signals S_{x1}–S_{x8}.

3.2.1 Principle of Field Orientation

The field orientation is classified into stator flux, air-gap flux, and rotor flux orientations. Among them, the rotor flux orientation is simple and easy to implement for motor drives [4]. The SCIM electromagnetic torque is given as,

$$T_e = \frac{3\,P\,L_m}{2\,L_r}\left(\lambda_{dr}\,i_{qs} - \lambda_{qr}\,i_{ds}\right) \tag{3.2.1}$$

which is a function of d and q-axis rotor flux components λ_{dr} and λ_{qr}, respectively. The decoupled control of rotor flux λ_r and electromagnetic torque T_e can be achieved by aligning the rotor flux vector $\boldsymbol{\lambda}_\mathbf{r}$ along with the d-axis of

the dq-reference frame rotating at a speed of ω_s given by

$$\omega_s = 2\pi\, f_s \tag{3.2.2}$$

where f_s is the stator frequency of the motor drive. The process of rotor flux vector aligned with the d-axis is referred to as field orientation. As a result, the q-axis component of rotor flux λ_{qr} becomes zero. The d-axis component of rotor flux λ_{dr} is equal to λ_r. Finally, the simplified electromagnetic torque is given as,

$$T_e = K_{_T}\, \lambda_r\, i_{qs} \tag{3.2.3}$$

where "$K_{_T} = 3PL_m/2L_r$" is the torque constant, λ_r is the magnitude of rotor flux vector $\boldsymbol{\lambda}_\mathbf{r}$, and i_{qs} is the q-axis stator current component. With the field orientation, the electromagnetic torque has a linear relationship with the q-axis stator current component i_{qs}.

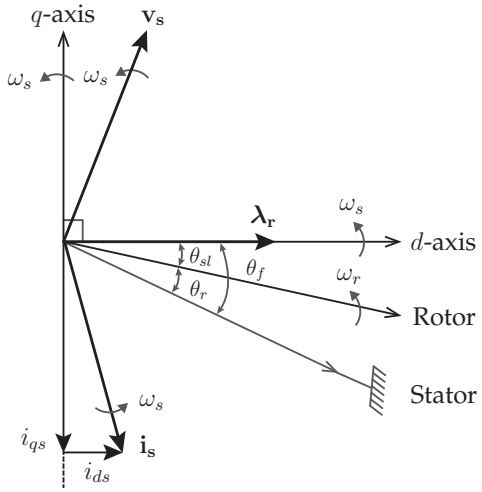


Figure 3.3. Space phasor diagram of field orientation.

The stator current vector $\mathbf{i_s}$ can be resolved into two orthogonal current components (d and q-axis current components) as shown in Fig. 3.3. The d-axis current component (i_{ds}) is the flux-producing component, while the q-axis current component (i_{qs}) is the torque-producing component. In field orientation, the rotor flux λ_r is maintained constant at its rated value. Therefore,

the i_{ds} become constant and equal to its rated value. The i_{qs} is independently controlled to meet the torque demand.

The determination of rotor flux vector position θ_f is one of the key issues in the field orientation. In IFOC scheme, the rotor flux vector position is obtained by

$$\theta_f = \theta_r + \theta_{sl} \tag{3.2.4}$$

where, θ_r and θ_{sl} are the measured rotor position angle and calculated slip angle, respectively.

3.2.2 Estimation of Rotor Flux Vector

The IFOC scheme requires the magnitude of rotor flux vector λ_r and its position θ_f, which are determined from the measured stator currents, rotor angular speed (ω_r), and calculated angular slip speed (ω_{sl}). The induction motor model in the arbitrary reference frame is employed to calculate the λ_r and θ_f values.

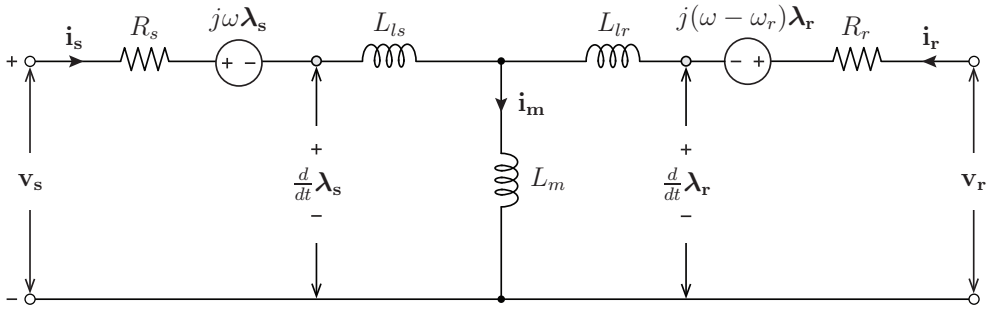


Figure 3.4. Space vector model of induction motor in the arbitrary reference frame.

From the equivalent circuit shown in Figure 3.4, the stator and rotor voltage vectors are defined as,

$$\begin{aligned} \mathbf{v_s} &= R_s\,\mathbf{i_s} + \frac{d\boldsymbol{\lambda}_\mathbf{s}}{dt} + j\omega\,\boldsymbol{\lambda}_\mathbf{s} \\ \mathbf{v_r} &= R_r\,\mathbf{i_r} + \frac{d\boldsymbol{\lambda}_\mathbf{r}}{dt} + j(\omega-\omega_r)\,\boldsymbol{\lambda}_\mathbf{r} \end{aligned} \tag{3.2.5}$$

where, $\mathbf{v_s}$ and $\mathbf{v_r}$ are the stator and rotor voltage vectors, $\mathbf{i_s}$ and $\mathbf{i_r}$ are the stator and rotor current vectors, $\boldsymbol{\lambda_s}$ and $\boldsymbol{\lambda_r}$ are the stator and rotor flux vectors, R_s and R_r are the stator and rotor winding resistances, ω is the rotating speed of arbitrary reference, and ω_r is the rotor angular speed.

The stator and rotor flux vectors are given by

$$\begin{aligned} \boldsymbol{\lambda_s} &= L_s\,\mathbf{i_s} + L_m\,\mathbf{i_r} \\ \boldsymbol{\lambda_r} &= L_r\,\mathbf{i_r} + L_m\,\mathbf{i_s} \end{aligned} \tag{3.2.6}$$

where, $L_s = L_{ls} + L_m$ is the stator self-inductance, $L_r = L_{lr} + L_m$ is the rotor self-inductance, L_{ls} and L_{lr} are the stator and rotor leakage inductances, and L_m is the magnetizing inductance.

The SCIM model in the dq-reference frame is obtained by replacing the ω with the ω_s, and $\mathbf{v_r} = 0$ in the equation (3.2.5), and it results in

$$\begin{aligned} \mathbf{v_s} &= R_s\,\mathbf{i_s} + \frac{d\boldsymbol{\lambda_s}}{dt} + j\omega_s\,\boldsymbol{\lambda_s} \\ 0 &= R_r\,\mathbf{i_r} + \frac{d\boldsymbol{\lambda_r}}{dt} + j\omega_{sl}\,\boldsymbol{\lambda_r} \end{aligned} \tag{3.2.7}$$

where, ω_s is the angular speed of a dq-reference frame and ω_{sl} is the angular slip speed ($\omega_{sl} = \omega_s - \omega_r$).

From equation (3.2.7), the angular slip speed (ω_{sl}) is given as

$$\frac{d\boldsymbol{\lambda_r}}{dt} = -R_r\,\mathbf{i_r} - j\omega_{sl}\,\boldsymbol{\lambda_r} \tag{3.2.8}$$

From equation (3.2.6), the rotor current is given as,

$$\mathbf{i_r} = \frac{1}{L_r}(\boldsymbol{\lambda_r} - L_m\,\mathbf{i_s}) \tag{3.2.9}$$

which is substituted in the equation (3.2.8) and results in

$$\frac{d\boldsymbol{\lambda_r}}{dt} = -\frac{R_r}{L_r}\,(\boldsymbol{\lambda_r} - L_m\,\mathbf{i_s}) - j\omega_{sl}\,\boldsymbol{\lambda_r} \tag{3.2.10}$$

from which

$$\boldsymbol{\lambda_r}\,(1 + \tau_r\,(p + j\,\omega_{sl})) = L_m\,\mathbf{i_s} \tag{3.2.11}$$

where, p is the derivative operator ($p = \frac{d}{dt}$) and τ_r is the rotor time constant ($\tau_r = \frac{L_r}{R_r}$).

Considering the field orientation ($\lambda_{qr} = 0$ and $\lambda_{dr} = \lambda_r$), the equation (3.2.11) is decomposed into two orthogonal components in dq-reference frame as,

$$\begin{aligned} \lambda_r \left(1 + p\,\tau_r\right) &= L_m\, i_{ds} \\ \omega_{sl}\,\tau_r\,\lambda_r &= L_m\, i_{qs} \end{aligned} \tag{3.2.12}$$

From equation (3.2.12), the magnitude of rotor flux vector and the angular slip speed are given by

$$\begin{aligned} \lambda_r &= \frac{L_m}{1 + p\,\tau_r}\, i_{ds} \\ \omega_{sl} &= \frac{L_m}{\tau_r\,\lambda_r}\, i_{qs} \end{aligned} \tag{3.2.13}$$

From the measured angular rotor speed (ω_r) and calculated angular slip speed (ω_{sl}), the position of rotor flux vector (θ_f) is given by

$$\theta_f = \int \left(\omega_r + \omega_{sl}\right) dt \tag{3.2.14}$$

The digital control implementation of the rotor flux magnitude and its position estimator is shown in Fig. 3.5. The three-phase stator currents in the abc-frame are transformed into the dq-reference frame. Rest of the blocks are simple constant blocks and derived from the equation (3.2.13) and (3.2.14). The output of the rotor flux estimator is the rotor flux magnitude λ_r and angular slip speed ω_{sl}. The measured rotor mechanical speed is multiplied with the pole pairs (P) to obtain the rotor electrical angular speed (ω_r). The angular slip speed is added to the rotor electrical angular speed, and results in the rotor flux vector angular speed in the dq-reference frame. The angular position of the rotor flux vector (θ_f) is obtained by integrating its angular speed as shown in Fig. 3.5.

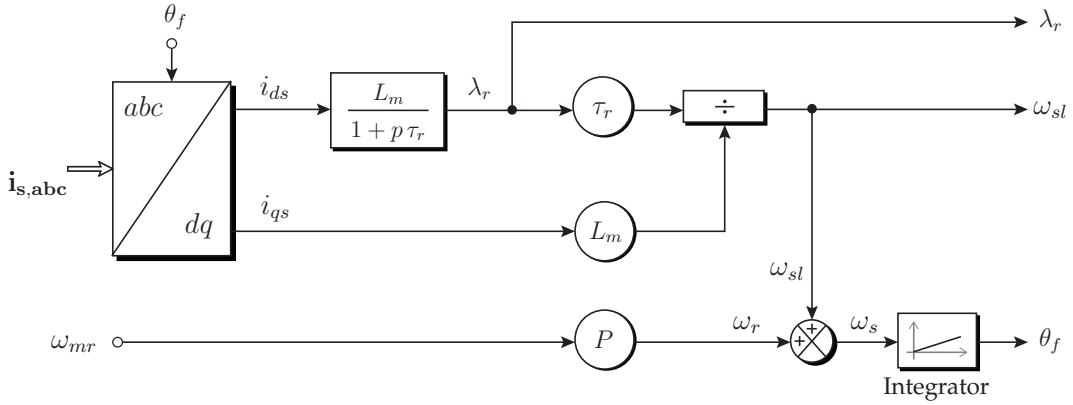


Figure 3.5. Estimation of rotor flux magnitude and position (λ_r and θ_f).

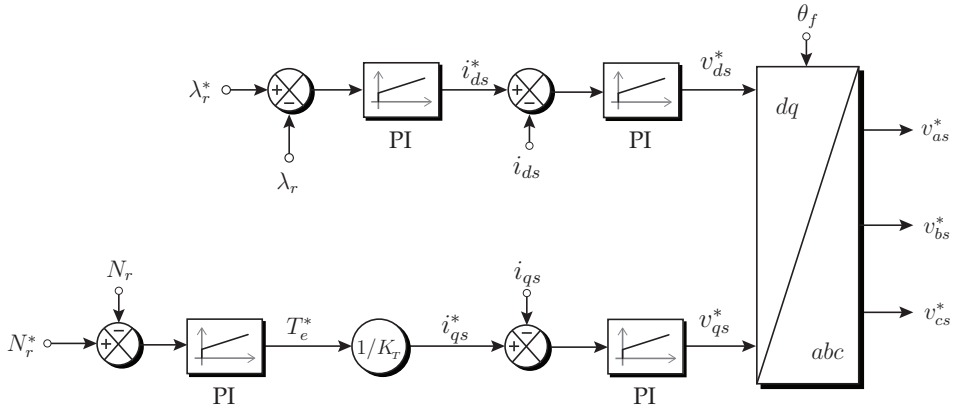


Figure 3.6. Control block diagram of IFOC.

3.2.3 Block Diagram of IFOC Scheme

The control block diagram of the IFOC scheme for SCIM is shown in Fig. 3.6. The IFOC consists of outer rotor flux and speed control loops, and inner current control loops. The motor rotor flux is maintained constant at their rated value by using rotor flux control. The reference rotor flux λ_r^* is compared with the estimated rotor flux λ_r. Its difference is minimized using a PI-regulator and results in a reference d-axis stator current component i_{ds}^*. The speed control loop minimizes the error between the reference and actual speed. The speed controller output is a reference electromagnetic torque T_e^*, which is

multiplied with the torque constant K_T to obtain the reference q-axis stator current component i_{qs}^* as shown in Fig. 3.6.

The feedback dq stator current components are obtained by transforming the measured three-phase stator currents i_{as}, i_{bs} and i_{cs} in the abc-frame to the rotor flux dq-reference frame. The feedback signals i_{ds} and i_{qs} are compared with their references, and corresponding errors are given to the PI-regulators. The PI-regulators generate the reference stator voltages v_{ds}^* and v_{qs}^* in the dq-reference frame. The dq-reference voltages are transformed back to the abc-frame. The reference stator voltages v_{as}^*, v_{bs}^*, and v_{cs}^* are used with the pulse width modulator to generate the gating signals for the switching devices.

Table 3.1. Three-phase SCIM Specifications

Motor Rating	**SI Unit**	**Motor Parameter**	**SI Unit**
Output Power (P_s)	1475 hp	Stator Resistance (R_s)	0.0726 Ω
Line-to-Line Voltage (V_s)	4000 V	Rotor Resistance (R_r)	0.1182 Ω
Stator Current (I_s)	159 A (rms)	Stator Leakage Inductance (L_{ls})	3.9 mH
Speed (N_r)	1189 RPM	Rotor Leakage Inductance (L_{lr})	3.9 mH
Torque (T_e)	8835 N-m	Magnetizing Inductance (L_m)	173.4 mH
Stator Flux Linkage (λ_s)	9.0 Wb (peak)	Moment of Inertia (J)	10 $kg-m^2$
Rotor Flux Linkage (λ_r)	8.35 Wb (peak)	Number of Pole Pairs (P)	3

3.3 Simulation Results

Fig. 3.2 shows the system configuration under study, where the motor is designed with the parameters given in Table 3.1. The net DC-link voltage of the 4L-MLC is realized by using a constant DC source of 6600 V. The flying capacitors of the 4L-MLC are designed with a capacitance of 3000 μF each and their nominal voltage is 2200 V. The proposed 4L-MLC is controlled with a modified carrier PWM scheme. The modified carrier PWM requires three triangular carrier signals, which are generated with a frequency of 5000 Hz.

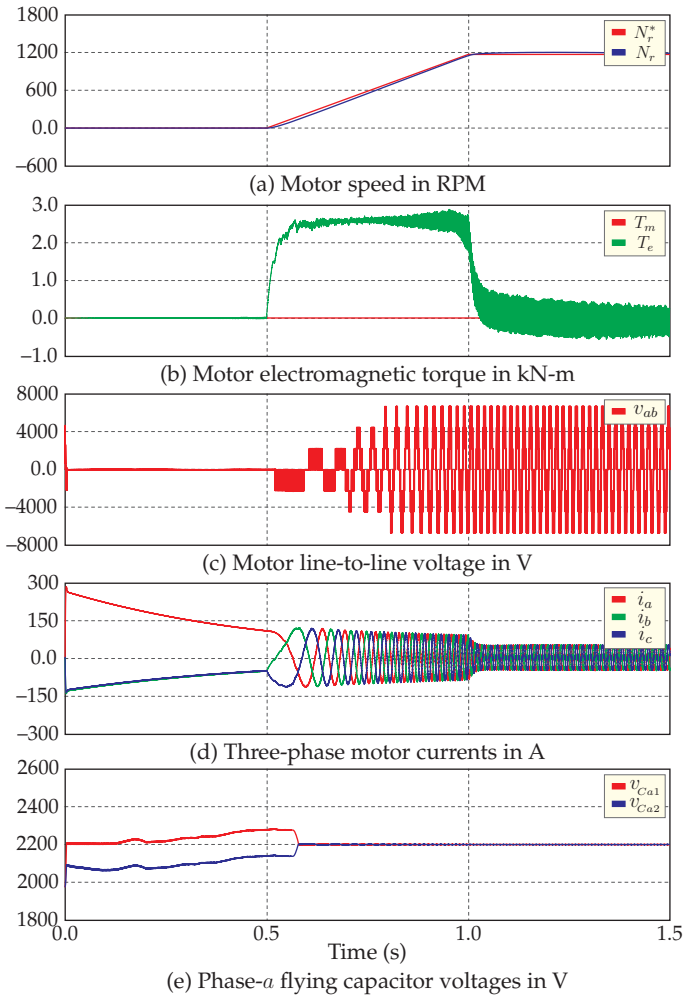
3.3.1 Start-up Operation

The start-up performance of the proposed 4L-MLC fed MV drive is shown in Fig. 3.7. From $t = 0$ s to 0.5 s, the reference speed and load torque (T_m) demand are set to zero. The converter is operated to establish the rotor flux of 8.35 Wb in the motor. The actual motor speed and electromagnetic torque follow their reference values as shown in Fig. 3.7(a) and 3.7(b), respectively. During this period, the motor voltage and currents are DC in nature as shown in Fig. 3.7(c) and 3.7(d), respectively. The phase-a flying capacitors are continuously charging due to the DC currents as shown in Fig. 3.7(e).

At $t = 0.5$ s, the motor reference speed is increased linearly and reaches their rated speed of 1189 RPM within 0.5 s. The speed and flux controller errors produce a finite value of the reference dq-axis currents, and these currents produce a rated flux and a finite electromagnetic torque in the motor as shown in Fig. 3.7(b). The motor draws finite currents and voltage corresponding to the produced electromagnetic torque. The flying capacitor voltages are perfectly regulated at their nominal values of 2200 V. When the reference and actual speeds reach the rated speed as shown in Fig. 3.7(a), whereas the motor developed torque becomes zero due to zero load torque (T_m) demand as shown in Fig. 3.7(b). The motor only draws voltage and no-load current component corresponding to the rotor flux. The flying capacitor voltages have very small ripple and regulated at their nominal values as shown in Fig. 3.7(e).

3.3.2 Transient Operation

In this study, the drive is operating at the rated speed of 1189 RPM as shown in Fig. 3.8(a). At $t = 0.5$ s, a step-change is applied in the load torque (T_m) demand from 0 kN-m to 8 kN-m as shown in Fig. 3.8(b). This sudden disturbance affects the speed controller performance and due to its slower response, it takes a longer time to reach its reference speed. The torque controller loop has a faster response, and the actual torque developed by the



(a) Motor speed in RPM

(b) Motor electromagnetic torque in kN-m

(c) Motor line-to-line voltage in V

(d) Three-phase motor currents in A

(e) Phase-a flying capacitor voltages in V

Figure 3.7. Startup performance of the proposed MV drive.

drive quickly follows its reference. The motor torque has a very small ripple due to the tight regulation of the flying capacitor voltages. This process leads to a smooth rotation of the drive and significantly improves its performance.

During this process, the converter generates a voltage at the motor terminals corresponding to the motor speed (voltage/frequency ratio) as shown in Fig. 3.8(c). These voltages have 7 steps and their frequency are close to 59.45 Hz ($\approx$ 60 Hz). From $t = 0$ s to 0.5 s, the motor develops 0 kN-m torque, and it draws only a no-load current component corresponding to the mo-

tor flux. From $t = 0.5$ s, the motor develops a 8 kN-M torque, and it draws a current component corresponding to the motor flux and developed electromagnetic torque as shown in Fig. 3.8(d). During this process, the converter flying capacitor voltages are regulated at their nominal values of 2200 V irrespective of the operating condition as shown in Fig. 3.8(e). The capacitor voltage ripples (peak-to-peak) are well below 5% of their nominal values.

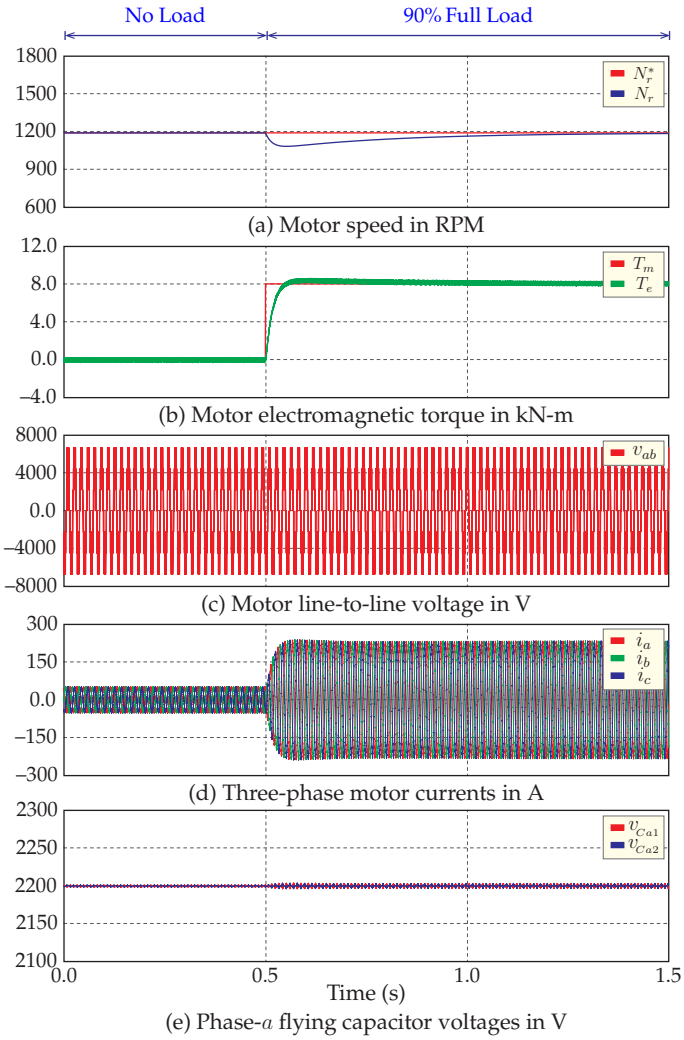
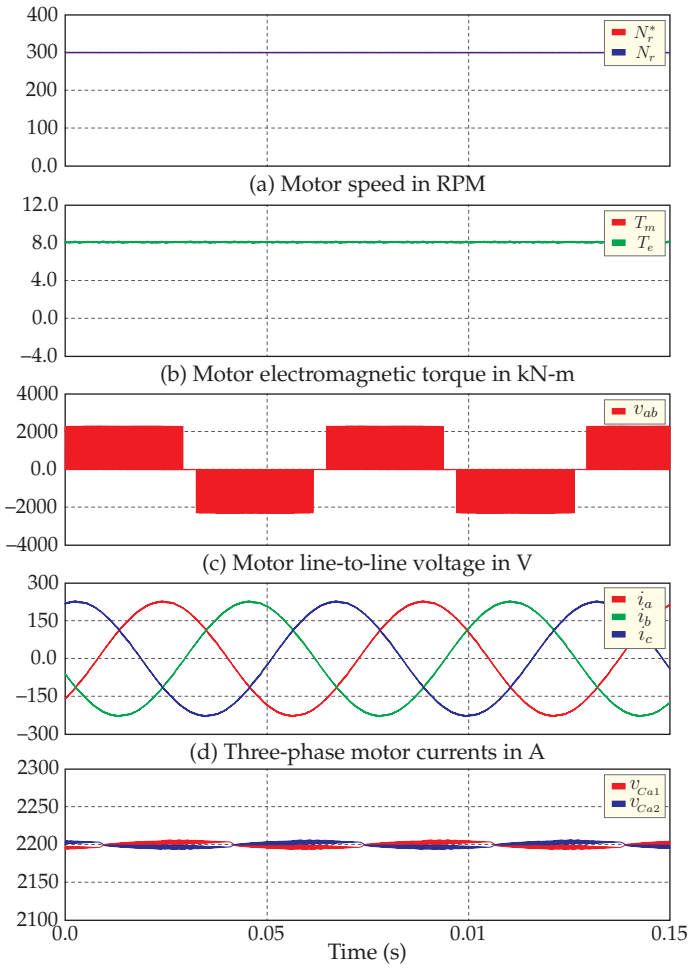


Figure 3.8. Transient performance of the proposed MV drive.

3.3.3 Low-Speed Operation

The proposed 4L-MLC fed MV drive is verified under the low-speed operating condition and corresponding results are presented in Fig. 3.9. In this study, the drive reference speed is set to 300 RPM, whereas the load torque demand is set to 8 kN-m as shown in Fig. 3.9(a) and 3.9(b), respectively. During this operation, the motor rotor flux is maintained constant at its rated value of 8.35 Wb.



(a) Motor speed in RPM

(b) Motor electromagnetic torque in kN-m

(c) Motor line-to-line voltage in V

(d) Three-phase motor currents in A

(e) Phase-a flying capacitor voltages in V

Figure 3.9. Low-speed (25% of synchronous speed) operation of the proposed MV drive.

The speed and torque controllers perfectly maintain the actual speed and electromagnetic torque of the motor at their reference values. The 4L-MLC generates a voltage at the motor terminals with a frequency of 15 Hz as shown in Fig. 3.9(c). These voltages have 3 steps corresponding to a low-speed operation. The motor draws a current of 250 A (peak) corresponding to the torque developed by the motor as shown in Fig. 3.9(d). The converter flying capacitor voltages are regulated at their nominal values with less than 5% ripples as shown in Fig. 3.9(e).

3.4 Summary

In this chapter, a new four-level multilevel converter (4L-MLC) fed medium-voltage (MV) drive is proposed. The indirect field-oriented control (IFOC) is applied to control the motor speed and torque. The IFOC scheme is implemented in the rotor flux reference frame. The modified carrier pulse width modulation (PWM) scheme is proposed along with the IFOC scheme to minimize the flying capacitor voltage ripple, thereby the drive has a very low speed and torque ripple. The modeling and implementation of IFOC in the synchronous dq-reference frame are presented. The simulation studies are presented to validate the proposed MV drive performance under start-up, transient, and low-speed operating conditions. The results show the proposed MV drive achieved very good performance in terms of lesser speed and torque ripple with the proposed control and PWM method. At the same time, the 4L-MLC flying capacitor voltages have smaller ripple (less than 5% of their nominal values) even under the low-speed operating condition. Hence, the converter flying capacitors can be designed with a smaller capacitance value, thereby the system cost becomes low.

CHAPTER 4

CONCLUSIONS

THE medium-voltage drives found a wide range of applications with the development of multilevel converters. However, the existing drive technologies have some limitations due to the cost and complexity involved in the multilevel converter topology. Moreover, the modern multilevel converters have flying capacitors, and these capacitors have a very high ripple at low-speed operation, causes higher speed and torque ripples in the drive. These issues lead to a poor performance of the MV drive system.

In this thesis, a new four-level multilevel converter (4L-MLC) fed medium-voltage motor drive is proposed. This work mainly includes the study on four-level multilevel converter topologies, voltage balancing methods, generalized carrier pulse width modulator design, and pulse width modulation schemes to handle the low-speed operation of the medium-voltage motor drive, and motor drive closed-loop control schemes. This chapter highlights the contributions and conclusions, as well the future work.

4.1 Contributions and Conclusions

The contributions and conclusions of this thesis are summarized as follows:

1) **A new four-level multilevel converter (4L-MLC) for medium-voltage applications**

A new 4L-MLC without series connection of devices is proposed for MV applications. Hence, the proposed topology does not require voltage equalization circuits. It also requires a lesser number of semiconductor devices and flying capacitors, and they do not need any clamping diodes. Hence, the proposed topology is competitive in cost compared with the existing converter topologies. Also, the proposed topology is suitable for back-to-back operation due to the presence of a common DC-link. The proposed topology has redundancy switching states, which can be used to achieve the voltage balancing objective. Hence, it does not require a complex control system.

2) **A new voltage balancing method for 4L-MLC**

A new voltage balancing method is proposed for 4L-MLC. The proposed method uses redundancy switching states to achieve the balancing of flying capacitors voltage. This method does not cause unwanted device switchings, unlike existing methods. Moreover, its balancing capability is extended to low power factors and low fundamental frequencies as well. The proposed method is designed such that it can be implemented with both multi-carrier PWM and SVM schemes.

3) **A new generalized carrier-based pulse width modulator for 4L-MLC**

The carrier arrangement directly affects the converter output voltage and current harmonic distortions, and flying capacitor voltage ripple. To investigate the performance of different carrier arrangements, a new pulse width modulator is proposed to control the 4L-MLC. With the proposed structure, it is easy to integrate the proposed voltage balancing method and study the performance of various multi-carrier arrangements for 4L-MLC.

4) **A modified carrier-based pulse width modulation scheme for the low-speed operation of MV drive**

The quality of output AC voltages/currents directly depends on flying capacitor voltage ripple, which in turn causes motor speed and torque ripple leading to a poor load performance. A modified multi-carrier PWM scheme is proposed to keep the flying capacitor voltage ripple within limits throughout the MV drive operation. By doing so, the converter generates voltage and current waveforms with a less harmonic distortion, which in turn leads to a smaller ripple in the motor speed and torque. The field-oriented control (FOC) in the rotor flux reference frame is applied to achieve the closed-loop control of motor speed/torque and flux in the proposed 4L-MLC fed MV drive system.

4.2 Future Work

In the present work, the classical PI-controllers are used to control the motor speed/torque and flux. These controllers significantly affect the dynamic response of the system. Furthermore, the modified carrier PWM scheme is able to minimize the capacitor voltage ripple at the cost of an aincrease in the average device switching frequency. Considering these issues, the following future works are suggested.

1. Investigate the control methods with a fast dynamic response for MV drives;
2. Investigate the pulse width modulation schemes with low device switching frequency to handle the low-speed operation of MV drive;
3. Develop a flying capacitor pre-charging method to 4L-MLC;
4. Develop a laboratory prototype to verify the feasibility of the proposed converter and methodologies;
5. Prepare the manuscripts for scholarly publications.

BIBLIOGRAPHY

[1] H. Stemmler, "High-power industrial drives," *Proc. IEEE*, vol. 82, no. 8, pp. 1266–1286, Aug 1994.

[2] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. . M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov 2009.

[3] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE Ind. Appl. Mag.*, vol. 18, no. 4, pp. 26–39, Jul 2012.

[4] B. Wu and M. Narimani, *High-power converters and AC drives*, 2nd ed. Wiley-IEEE Press, Jan 2017.

[5] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: Challenges and existing technology," *IEEE Power Electron. Maz.*, vol. 3, no. 2, pp. 29–41, Jun 2016.

[6] Z. Quan, L. Ge, Z. Wei, Y. W. Li, and L. Quan, "A survey of powertrain technologies for energy-efficient heavy-duty machinery," *Proc. IEEE*, vol. 109, no. 3, pp. 279–308, Mar 2021.

[7] "Ieee recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, 2014.

[8] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan 1999.

[9] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug 2005.

[10] K. P. Phillips, "Current-source converter for ac motor drives," *IEEE Trans. Ind. Appl.*, vol. 8, no. 6, pp. 679–683, Nov 1972.

[11] J. Rodriguez, B. Wu, S. Bernet, N. Zargari, J. Rebolledo, J. Pontt, and P. Steimer, "Design and evaluation criteria for high power drives," in *2008 IEEE Industry Applications Society Annual Meeting*, pp. 1–9, 2008.

[12] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Simple ac/dc converters to meet iec 1000-3-2," in *APEC 2000 - Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, vol. 1, pp. 487–493, 2000.

[13] M. Verma, D. Phares, and B. Dick, "Medium voltage adjustable speed drives: Power factor and motor control–a beautiful combination," in *2019 IEEE-IAS/PCA Cement Industry Conference (IAS/PCA)*, pp. 1–11, 2019.

[14] J. Rodriguez, J. Pontt, C. Silva, R. Musalem, P. Newman, R. Vargas, and S. Fuentes, "Resonances and overvoltages in a medium-voltage fan motor drive with long cables in an underground mine," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 856–863, May-Jun 2006.

[15] A. S. Maklakov, A. A. Radionov, and V. R. Gasiyarov, "Power factor correction and minimization thd in industrial grid via reversible medium voltage ac drives based on 3l-npc afe rectifiers," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, pp. 2551–2556, 2016.

[16] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage pwm voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, Sept 2000.

[17] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output filters for ac adjustable speed drives," in *APEC 2007 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 236–242, 2007.

[18] D. Rendusara, E. Cengelci, P. Enjeti, V. Stefanovic, and J. Gray, "Analysis of common mode voltage-"neutral shift" in medium voltage pwm adjustable speed drive (mv-asd) systems," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1124-1133, Nov 2000.

[19] M. Mechlinski, S. SchrÃ¶der, J. Shen, and R. W. De Doncker, "Grounding concept and common-mode filter design methodology for transformerless mv drives to prevent bearing current issues," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5393–5404, Nov-Dec 2017.

[20] S. Wei, N. Zargari, B. Wu, and S. Rizzo, "Comparison and mitigation of common mode voltage in power converter topologies," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, vol. 3, pp. 1852–1857, 2004.

[21] T. K. Jappe, S. A. Mussa, M. L. Heldwein, D. R. Caballero, and A. Castillo, "Space vector modulation scheme to minimize common-mode voltage gener-

ated by a three-phase hybrid multilevel inverter," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, pp. 1–9, 2011.

[22] T. Laczynski and A. Mertens, "Predictive stator current control for medium voltage drives with ¡emphasis emphasistype="italic"¿lc ¡/emphasis¿ filters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2427–2435, Nov 2009.

[23] T. Geyer, P. Karamanakos, and R. Kennel, "On the benefit of long-horizon direct model predictive control for drives with lc filters," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3520–3527, 2014.

[24] J. A. Sayago, T. Bruckner, and S. Bernet, "How to select the system voltage of mv drives-a comparison of semiconductor expenses," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3381–3390, Sept 2008.

[25] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212–4228, 2015.

[26] A. Nagel, S. Bernet, T. Bruckner, P. Steimer, and O. Apeldoorn, "Characterization of igcts for series connected operation," in *Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129)*, vol. 3, pp. 1923–1929, 2000.

[27] K. Vechalapu, S. Hazra, U. Raheja, A. Negi, and S. Bhattacharya, "High-speed medium voltage (mv) drive applications enabled by series connection of 1.7 kv sic mosfet devices," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 808–815, 2017.

[28] S. Rizzo and N. Zargari, "Medium voltage drives: what does the future hold?" in *The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.*, vol. 1, pp. 82–89, 2004.

[29] J. Rodriguez, J. Pontt, N. Becker, and A. Weinstein, "Regenerative drives in the megawatt range for high-performance downhill belt conveyors," *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 203–210, Jan-Feb 2002.

[30] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[31] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.

[32] E. Watanabe, M. Aredes, L. Willcox de Souza, and M. Bellar, "Series connection of power switches for very high-power applications and zero-voltage switching," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 44–50, Jan 2000.

[33] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters: State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.

[34] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[35] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631-1656, Dec 2017.

[36] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Pèrez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul 2010.

[37] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun 2008.

[38] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[39] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul 2010.

[40] V. Yaramasu and B. Wu, "Model predictive decoupled active and reactive power control for high-power grid-connected four-level diode-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3407–3416, Jul 2014.

[41] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source pwm inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar 2000.

[42] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level npc converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2262–2271, Jul 2010.

[43] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active npc switches," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 2, pp. 1135–1140, 2001.

[44] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Initial capacitor charging in grid-connected flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3245–3249, Jul 2014.

[45] D. Janik, T. Kosan, P. Kamenicky, and Z. Peroutka, "Universal precharging method for dc-link and flying capacitors of four-level flying capacitor converter," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, pp. 6322–6327, 2013.

[46] B. P. McGrath and D. G. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three-phase flying capacitor converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1425–1433, Jul 2009.

[47] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "New active capacitor voltage balancing method for flying capacitor multicell converter based on logic-form-equations," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3467–3478, May 2017.

[48] B. P. McGrath and D. G. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1554–1561, Jun 2009.

[49] M. V. Bressan, C. Rech, and A. L. Batschauer, "Impact of capacitor design methodology on fc inverters," in *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, pp. 1–6, 2019.

[50] A. M. Y. M. Ghias, J. Pou, G. J. Capella, P. Acuna, and V. G. Agelidis, "On improving phase-shifted pwm for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5384–5388, Aug 2016.

[51] J. Ebrahimi and H. Karshenas, "A new modulation scheme for a four-level single flying capacitor converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 1860–1870, Jun 2021.

[52] M. Wu, Y. W. Li, H. Tian, Y. Li, and K. Wang, "Modified carrier-overlapped pwm with balanced capacitors and eliminated dead-time spikes for four-level nnpc converters under low frequency," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, pp. 1–1, 2021.

[53] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (nnpc) converter for medium-voltage (mv) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec 2014.

[54] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A novel and simple single-phase modulator for the nested neutral-point clamped (nnpc) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4069–4078, Aug 2015.

[55] H. Tian and Y. W. Li, "Carrier based three-level pwm for improving flying capacitor balancing of nested neutral-point-clamped (nnpc) converter," in *2017*

IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2590–2597, Mar 2017.

[56] L. Tan, B. Wu, M. Narimani, D. Xu, and G. Joós, "Multicarrier-based pwm strategies with complete voltage balance control for nnpc inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2863–2872, Apr 2018.

[57] L. Tan, B. Wu, M. Narimani, D. Xu, J. Liu, Z. Cheng, and N. R. Zargari, "A space virtual-vector modulation with voltage balance control for nested neutral-point clamped converter under low output frequency conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3458–3466, May 2017.

[58] K. Wang, Z. Zheng, and Y. Li, "Topology and control of a four-level anpc inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2342–2352, Mar 2020.

[59] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A four-level hybrid-clamped converter with natural capacitor voltage balancing ability," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1152–1162, Mar 2014.

[60] J. Pan, Y. Yang, H. Cai, and L. Xu, "Capacitor voltage fluctuation minimization for 4-level hybrid clamped converter using improved common mode voltage injection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7560–7573, Jul 2020.

[61] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Voltage balancing control of a four-level hybrid-clamped converter based on zero-sequence voltage injection using phase-shifted pwm," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5389–5399, Aug 2016.

[62] F. Faraji, A. Hajirayat, and M. Narimani, "Fault tolerant t-type nested neutral point clamped (t-nnpc) converter," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, pp. 1–6, 2017.

[63] W. Wu and D. Wang, "An optimal voltage-level based model predictive control approach for four-level t-type nested neutral point clamped converter with reduced calculation burden," *IEEE Access*, vol. 7, pp. 87 458–87 468, 2019.

[64] L. Ji, C. Zheng, Q. Wang, and Q. Chen, "A simplified virtual space vector modulation strategy for four-level t-type nnpc converter," in *2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp. 2344–2349, 2019.

[65] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[66] A. Dekka, V. Yaramasu, R. L. Fuentes, and D. Ronanki, "Chapter 5 - modular multilevel converters," in *Multilevel Inverters*, E. Kabalci, Ed. Academic Press, 2021, pp. 147–179. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128216682000040

[67] A. Nami, J. Liang, F. Dijkhuizen, and G. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan 2015.

[68] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular Multilevel Converters: Analysis, Control, and Applications*. Wiley-IEEE Press, Feb 2018.

[69] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan 2015.

[70] J.-J. Jung, H.-J. Lee, and S.-K. Sul, "Control strategy for improved dynamic performance of variable-speed drives with modular multilevel converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 371–380, Jun 2015.

[71] L. He, K. Zhang, J. Xiong, S. Fan, and Y. Xue, "Low-frequency ripple suppression for medium-voltage drives using modular multilevel converter with full-bridge submodules," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 657–667, Jun 2016.

[72] A. Dekka, B. Wu, V. Yaramasu, R. L. Fuentes, and N. R. Zargari, "Model predictive control of high-power modular multilevel converters–an overview," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 168–183, Mar 2019.

[73] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Trans. Ind. Electron.*, vol. 39, no. 5, pp. 410–420, Oct 1992.

[74] D. Holmes and B. McGrath, "Opportunities for harmonic cancellation with carrier-based pwm for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 574–582, Mar-Apr 2001.

[75] B. P. McGrath and D. G. Holmes, "Multicarrier pwm strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug 2002.

[76] R. Naderi and A. Rahmati, "Phase-shifted carrier pwm technique for general cascaded inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257–1269, May 2008.

[77] K. Wang, Z. Zheng, and Y. Li, "A novel carrier-overlapped pwm method for four-level neutral-point clamped converters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 7–12, Jan 2019.

[78] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A generalized carrier-overlapped pwm method for neutral-point-clamped multilevel converters," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9095–9106, Sept 2020.

[79] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted pwm control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, Jan 2007.

[80] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Comparison of phase-shifted and level-shifted pwm in the modular multilevel converter," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pp. 3764–3770, May 2014.

[81] A. Marquez, J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, E. Freire, and S. Kouro, "Variable-angle phase-shifted pwm for multilevel three-cell cascaded h-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3619–3628, May 2017.

[82] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier pwm for cascaded h-bridge converters and modular multilevel converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 589–605, Jun 2016.

[83] P. Sochor and H. Akagi, "Theoretical and experimental comparison between phase-shifted pwm and level-shifted pwm in a modular multilevel sdbc inverter for utility-scale photovoltaic applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4695–4707, Sept-Oct 2017.

[84] Z. Shu, J. Tang, Y. Guo, and J. Lian, "An efficient svpwm algorithm with low computational overhead for three-phase inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1797–1805, Sept 2007.

[85] A. Gupta and A. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sept 2007.

[86] R. M. Tallam, D. Leggate, D. W. Kirschnik, and R. A. Lukaszewski, "Reducing common-mode current: A modified space vector pulsewidth modulation scheme," *IEEE Ind. Appl. Mag.*, vol. 20, no. 6, pp. 24–32, 2014.

[87] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan 2008.

[88] L. Franquelo, M. Prats, R. Portillo, J. Galvan, M. Perales, J. Carrasco, E. Diez, and J. Jimenez, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr 2006.

[89] M. Renge and H. Suryawanshi, "Three-dimensional space-vector modulation to reduce common-mode voltage for multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2324–2331, Jul 2010.

[90] N.-Y. Dai, M.-C. Wong, Y.-H. Chen, and Y.-D. Han, "A 3-d generalized direct pwm algorithm for multilevel converters," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 85–88, Sept 2005.

[91] A. Gupta and A. Khambadkone, "A space vector pwm scheme for multilevel inverters based on two-level space vector pwm," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct 2006.

[92] Y. Deng, K. H. Teo, C. Duan, T. Habetler, and R. Harley, "A fast and generalized space vector modulation scheme for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5204–5217, Oct 2014.

[93] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan 2016.