A Design Methodology For Low Power CMOS Current Source

by

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Abstract

A current reference circuit is a basic building block in analog, digital and mixed-signal design systems. This work focuses on one type of integrated CMOS current reference circuit. This source only uses one type of MOSFET transistor and is suitable to produce very low currents in the order of nano Amperes. Despite being used in several works in the literature, there is no clear methodology to produce an optimal design for this source. With the absence of a design methodology, process variability becomes critical in affecting the performance of the current source. This variability issue is prominent in nanometer scaling of the technology. This work addresses that problem by developing a methodology to achieve a design with low area and low sensitivity to transistor mismatch.

Presented are the sensitivity and mismatch analysis, methodology, design example and results in addition to performance figures for a lesser sensitive circuit as compared with its traditional counterpart. Future scope of research has also been included in this thesis.

Dedication

-To my Late Grandparents

Acknowledgements

I am thankful to the following that helped me engineer this interesting work.

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7. Thank you very much Yusaf Magsi for always supporting and motivating me.

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-Anuj Sharma(2016)

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Chapter 1

Introduction

1.1 Motivation and Objective

Analog, digital, and mixed-signal systems require a fundamental building block known as current reference circuit that provides biasing to the integrated circuits [1]. Integrated circuits incorporate current references extensively. For example, a current reference circuit [2] is used to bias operational amplifiers. Another application of current reference circuit is in biasing voltage reference circuits required in the quantization step of analog to digital converters [3]. A reference of such a kind has a well-defined dependence on temperature, little or no dependence (ideally) on the supply voltage as shown in Figure 1.1.

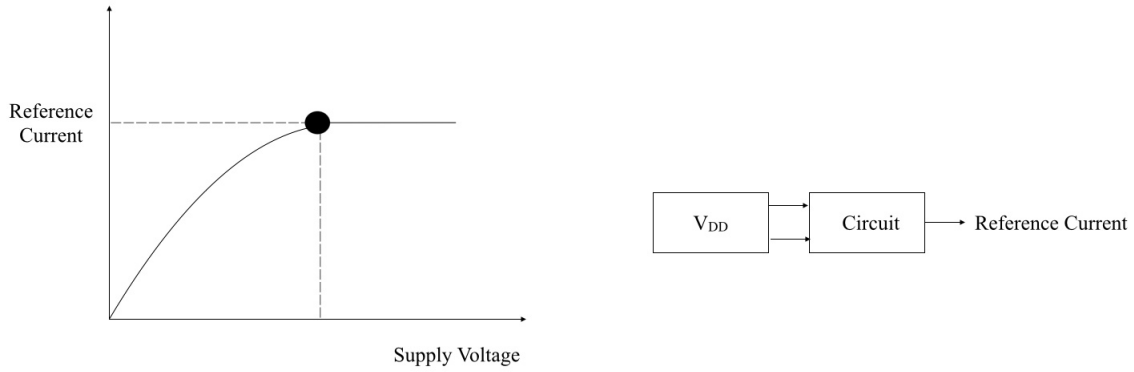

Figure 1.1: Current Reference Overview

Some current reference circuits require resistors or two types of transistors having different threshold voltages to generate the output current. The current source [4] studied and analysed in this thesis only requires standard CMOS transistors and is suitable for low voltage and low power applications.

Process parameter variations and mismatch are unavoidable, and they have an effect in the generated output current. A good design should not be very sensitive to mismatch and process variations.

The objectives of this work are to study the effects of process parameter variations and device mismatch in the current reference circuit proposed in [4] and to develop a design methodology to minimize their effects.

1.2 Thesis Outline

In order to realize the objectives, background information has been furnished in Chapter 2. Chapter 3, reviews previous works assisting the construction of an understanding of the unsolved problem.

An extensive sensitivity and mismatch analysis is documented in Chapter 4. The solution to the unaccounted problem comes by the development of a proposed design methodology presented in Chapter 5 with a design example. The thesis ends with the discussion on the future scope of research in Chapter 6.

Chapter 2

Background

This chapter covers the fundamental knowledge required to understand and design the transistor based current source circuit. The chapter begins with an explanation of the Advanced Compact MOSFET Model (ACM) [5] that is used in this thesis.
As the design decision relies on the layout, therefore layout considerations are discussed. The chapter ends with definitions of figures of merit including sensitivity, line sensitivity and power supply rejection ratio (PSRR).

2.1 ACM Model

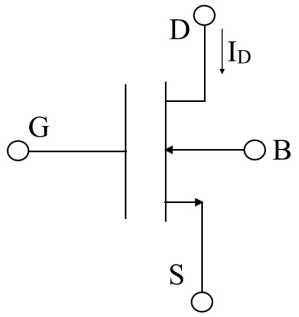

Figure 2.1: A NMOS with Four Terminals

This section describes a continuously differentiable model that is consistent through all the operational region of transistor [5] based on physical parameters. The transistor schematic is shown in Figure 2.1. V_G, V_S and V_D are the gate, source and drain voltages respectively. All of

them are referred to bulk (B). The following equations are valid for a long channel N-MOSFET. The drain current I_D flowing through the MOSFET is quantified as:

$$I_D = I_{SQ} S (i_f - i_r), \tag{2.1}$$

where i_f, i_r are forward inversion level coefficient and reverse inversion level coefficient respectively, S is the aspect ratio given as $S{=}\frac{W}{L}$, where W is the width of the transistor and L is the length of the transistor. I_{SQ} is a technology dependent sheet normalisation current given by following equation:

$$I_{SQ} = \frac{n \mu_n C_{ox} V_T^2}{2}, \tag{2.2}$$

where n is subthreshold slope factor, μ_n is electron mobility, C_{ox} is the oxide capacitance per unit area and V_T is thermal voltage given as $\frac{kT}{q}$ with k being Boltzmann constant, T is temperature and q is electronic charge.

The voltages at the transistor terminals are related to the inversion coefficients through the following equations:

$$\mathcal{F}(i_f) \simeq \frac{V_p - V_S}{V_T}. \tag{2.3}$$

$$\mathcal{F}(i_r) \simeq \frac{V_p - V_D}{V_T}, \tag{2.4}$$

where V_p is the pinch-off voltage given by:

$$V_p = \frac{V_G - V_{th}}{n}, \tag{2.5}$$

where V_{th} is threshold voltage of transistor. $\mathcal{F}(i_{(f,r)})$ is defined as:

$$\mathcal{F}(i_{(f,r)}) = -2 + \sqrt{1 + i_{(f,r)}} + \ln(\sqrt{1 + i_{(f,r)}} - 1). \tag{2.6}$$

Subtracting Equation (2.3) from Equation (2.4) leads to the following equation:

$$\mathcal{F}(i_f) - \mathcal{F}(i_r) = \frac{V_p - V_S - V_p + V_D}{V_T} = \frac{V_{DS}}{V_T}. \tag{2.7}$$

Solving Equation (2.7) using Equation (2.6), the following expression is obtained:

$$\frac{V_{DS}}{V_T} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1}\right). \tag{2.8}$$

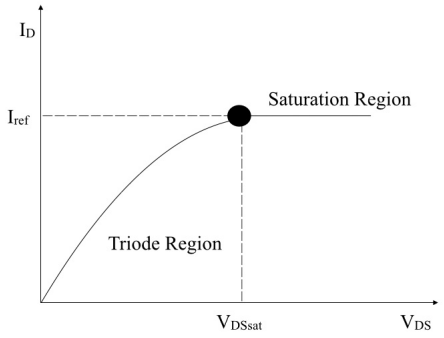

Figure 2.2: Output Characteristic of a Long-Channel N-MOSFET in Saturation

Defining $\xi = \frac{\sqrt{1+i_r}-1}{\sqrt{1+i_f}-1}$ and solving Equation (2.8) for drain-source voltage V_{DS}:

$$V_{DS} = V_T \left[\ln\left(\frac{1}{\xi}\right) + (1-\xi)\left(\sqrt{1+i_f} - 1\right)\right]. \tag{2.9}$$

Equation (2.9) defines the boundary between triode and saturation region in terms of inversion level. ξ is chosen arbitrarily small as 0.01 to calculate the minimum drain-source saturation voltage $V_{DS_{sat}}$ required to keep the operation of MOSFET in active region for a given inversion level. $V_{DS_{sat}}$ for ξ=0.01 is obtained as:

$$V_{DS_{sat}} = V_T(\sqrt{1+i_f} + 3.6). \tag{2.10}$$

If the transistor is working in saturation region then i_f becomes much higher than i_r, hence i_r can be neglected. Therefore the current I_D is expressed as:

$$I_D \simeq S I_{SQ} i_f. \tag{2.11}$$

The value of inversion coefficient determines the region of operation of MOSFET [5]:

1. i_f <1

   A lesser than 1 inversion level coefficient (i_f) indicates weak inversion level.

2. $1 \leq i_f \leq 100$

   A range of inversion level coefficient (i_f) from 1 to 100 indicates moderates inversion level.

3. $i_f > 100$

   As soon as inversion level coefficient (i_f) is greater than 100, strong inversion level condition is obtained.

Consistency of ACM model with standard MOSFET model is shown in next two subsections by deriving the equations for both models in weak and strong inversion.

2.1.1 Weak inversion

In weak inversion the inversion coefficient i_f is small. The assumption of source voltage V_S=0 helps in neglecting the body effect. The use of Taylor series approximation results in the following expression:

$$\mathcal{F}(i_f) \simeq -1 + \ln\left(\frac{i_f}{2}\right). \tag{2.12}$$

From Equation (2.3) and (2.5), the following equation results:

$$\frac{V_G - V_{th}}{nV_T} \simeq -1 + \ln\left(\frac{i_f}{2}\right). \tag{2.13}$$

Solving Equation (2.13) for i_f

$$i_f \simeq 2\exp(1)\exp\left(\frac{V_G - V_{th}}{nV_T}\right). \tag{2.14}$$

Now putting the Equation (2.14) of i_f in the Equation (2.11) of drain current results in the following equation:

$$I_D = S\exp(1)n\mu_n C_{ox}V_T^2\exp\left(\frac{V_G - V_{th}}{nV_T}\right). \tag{2.15}$$

Thus a clear manifestation of exponential growth of drain current with the gate voltage in weak inversion.

The weak inversion current equation for standard MOSFET model is represented as [6]:

$$I_{D_{standard}} = S\mu_n C_{ox}(n-1)V_T^2\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right). \tag{2.16}$$

2.1.2 Strong inversion

The inversion coefficient i_f is greater than 100 in strong inversion. Thus $\mathcal{F}(i_f)$ simplifies to:

$$\mathcal{F}(i_f) \simeq \sqrt{i_f}. \tag{2.17}$$

Relating Equation (2.17) and Equation (2.3) and (2.5) the following expression for i_f is achieved.

$$i_f = \left(\frac{V_G - V_{th}}{nV_T} - \frac{V_S}{V_T}\right)^2. \tag{2.18}$$

Assuming V_S=0, so from Equation (2.18) i_f becomes:

$$i_f = \left(\frac{V_G - V_{th}}{nV_T}\right)^2. \tag{2.19}$$

Thus drain current becomes

$$I_D = SI_{SQ}\left(\frac{V_G - V_{th}}{nV_T}\right)^2. \tag{2.20}$$

Using the expression of I_{SQ} from Equation (2.2), the drain current I_D is given as:

$$I_D = S\left(\frac{\mu_n C_{ox}}{2}\right)\frac{1}{n}\left(V_G - V_{th}\right)^2. \tag{2.21}$$

It is critical to note that V_G=V_{GS} since V_S=0. This current equation is different from standard MOSFET model equation by subthreshold slope factor n. The current equation for standard MOSFET model is given as [6]:

$$I_{D_{standard}} = S\left(\frac{\mu_n C_{ox}}{2}\right)\left(V_G - V_{th}\right)^2. \tag{2.22}$$

It is important to note that standard MOSFET model and square-law model is one and same.

2.2 Simple Current Source

2.2.1 Basic Current Reference circuit

The generation of reference current in its very basic form is achieved by connecting a resistor R_1 from supply voltage V_{DD} to the gate of transistor M_1 as shown in Figure 2.3.

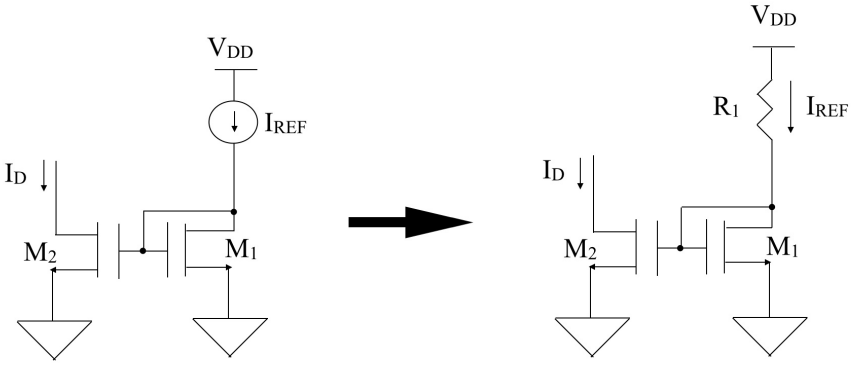

Figure 2.3: Current Reference Generation

The drain current of M_1 is supplied by V_{DD} through resistor R_1 and this current through resistor R_1 is I_{REF} the reference current given as:

$$I_{REF} = \frac{V_{DD} - V_{G1}}{R_1}, \tag{2.23}$$

where V_{DD} is supply voltage, R_1 is the input resistor and V_{G1} is gate voltage of transistor M_1. As source of transistor M_1 is grounded, the function of inversion level of this transistor is expressed as:

$$\mathcal{F}(i_{f1}) = \frac{V_{G1} - V_{th1}}{nV_T}. \tag{2.24}$$

The equation for gate voltage of transistor M_1 solved using Equation (2.24) is quantified as:

$$V_{G1} = nV_T\mathcal{F}(i_{f1}) + V_{th1}. \tag{2.25}$$

From Equations (2.23),(2.25), the resistance R_1 is expressed as:

$$R_1 = \frac{V_{DD} - \left[V_{th1} + nV_T\mathcal{F}(i_{f1})\right]}{I_{REF}}. \tag{2.26}$$

Given the supply voltage, and the reference current I_{REF} to be generated and desired inversion level coefficient i_{f1}. Put all the values in Equation (2.26) to find the value of resistor R_1. The transistors are sized using Equation (2.11).

For current in both branches to be equal, M_1 shall match M_2. Reference current I_{REF} will vary with supply voltage due to the generation of current through resistor R_1. This is a major drawback of this circuit.

2.2.2 Widlar Current Source

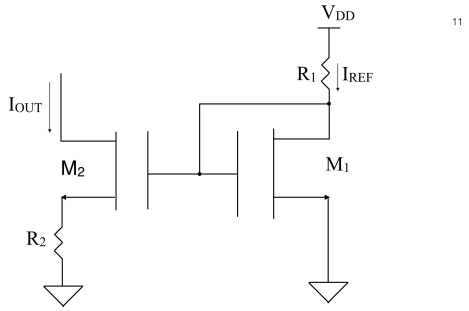

Figure 2.4: Widlar Current Source

The explanation of Widlar current source in this section uses MOSFET transistors, however the original work [7] is based on bipolar transistors. The inclusion of output resistor R_2 in the Widlar current source [6] of Figure 2.4, makes current output I_{OUT} less dependent upon input current I_{IN} and supply voltage V_{DD}.

The transistor M_1 is working in saturation region (The input reference current should not be very low) as its gate is shorted to the drain thus making it a diode connected transistor.

The function of inversion level of transistor M_2 as explained in the Section 2.1 is given as:

$$\mathcal{F}(i_{f2}) = \frac{V_{G2} - V_{th2}}{nV_T} - \frac{V_{S2}}{V_T}. \tag{2.27}$$

Using Equation (2.24) and Equation (2.27) results in the following equation:

$$\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2}) = \frac{V_{S2}}{V_T}. \tag{2.28}$$

Substituting source voltage V_{S2}=$R_2 I_{OUT}$ in Equation (2.28) and solving for R_2 results in the following expression:

$$R_2 = \frac{V_T\Big(\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2})\Big)}{I_{OUT}}, \tag{2.29}$$

where I_{OUT} is the output current, $\mathcal{F}(i_{f1})$ and $\mathcal{F}(i_{f2})$ are function of inversion level of transistor M_1 and M_2 respectively.

The design starts by calculating input resistor R_1 from Equation (2.26). The output resistor is calculated by choosing value of output current and inversion coefficients i_{f1}, i_{f2}. The transistors are sized using Equation (2.11).

The disadvantage of such a circuit is that reference current is not fully supply independent as any variation in supply voltage will cause variation in reference current. The solution to this problem is presented in the Section 2.2.3.

2.2.3 Self-Biased Widlar Current Source

Self-biased structure [6] or bootstrapping as shown in Figure 2.5, reduces the power supply sensitivity. Input current is not generated by the input resistor, rather it is made dependent upon output current. Power supply sensitivity is greatly reduced if the feedback loop has a stable operating point.

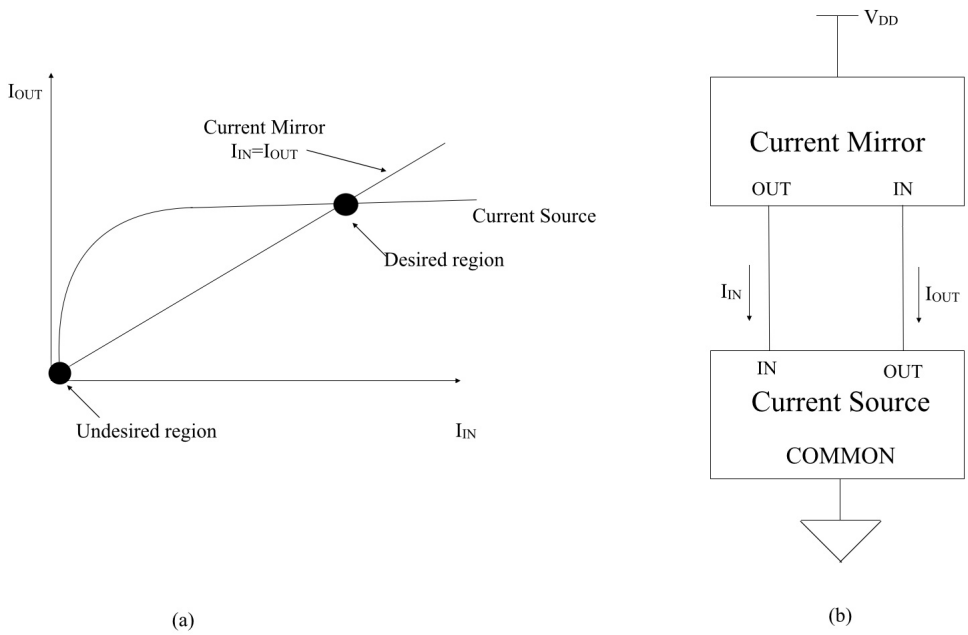

Figure 2.5: Self-Biased Reference (a)Determination of Operating Region and (b)Block Diagram

As can be seen in part (a) of Figure 2.5 from the viewpoint of current mirror, output current I_{OUT} is directly related to input current I_{IN} (A change in input current changes the output current by same amount) but from the viewpoint of current source, output current I_{OUT} is weakly dependent on input current I_{IN} (Output current does not change with the change in the input current).

The gain of PMOS current mirror is assumed to be unity and hence increase in input current is observed by the current mirror whenever output current increases. On the other hand, output current of the current source is increased by the amount depending upon the gain of the current source. The operating region is at the intersection of these two characteristics. In the desired region of operation the gain of the loop is very minute as change in input current has little impact on output current.

In stable operating point that is in desired region, gain is very small as output current I_{OUT} is less dependent on input current I_{IN}. On the other side, gain at unstable operating point which is undesired region is made greater than unity so that point of intersection at two characteristics is away from origin. In practice, current in unstable operating point is in the range of pico-ampere making it a stable operating point. Leakage currents and other effects reduces gain of current

mirror at such low levels therefore making the gain less than unity causing the circuit to operate in zero current state. So, a start-up circuit is required to make sure circuit do not operate in zero current state when power supply is non-zero.

As shown in Figure 2.6, the input resistor R_1 of Figure 2.4 is replaced by a PMOS current mirror making the source a self biased structure giving an advantage of supply insensitive reference current generation.

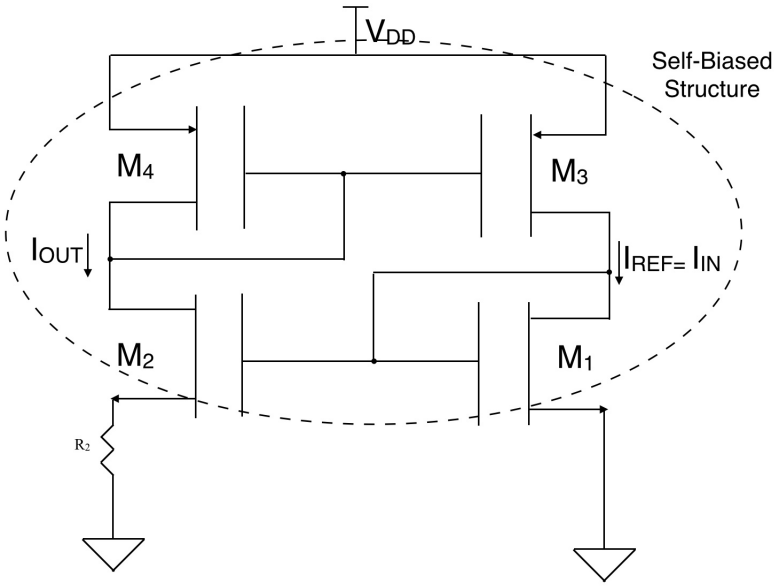

Figure 2.6: Self Biased Widlar Current Source

From Equation (2.28), the ratio of source voltage of transistor M_2 to thermal voltage V_T ($\frac{V_{S2}}{V_T}$) is represented as:

$$\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2}) = \frac{V_{S2}}{V_T}. \tag{2.30}$$

Resistance R_2 is given as:

$$R_2 = \frac{V_T\Big(\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2})\Big)}{I_{OUT}}. \tag{2.31}$$

The design starts by choosing a value of drain current in each branch and inversion coefficients i_{f1}, i_{f2}. From the chosen values output resistor R_2 is calculated using Equation(2.31). The transistors are sized using Equation (2.11). A unity gain PMOS mirror is designed.

This source is supply independent due to the presence of PMOS current mirror. Still it posses

a problem of large area for small reference current generation as resistor takes up large silicon area during fabrication [4]. A resistorless current reference design was presented in [8].

2.3 Layout Considerations

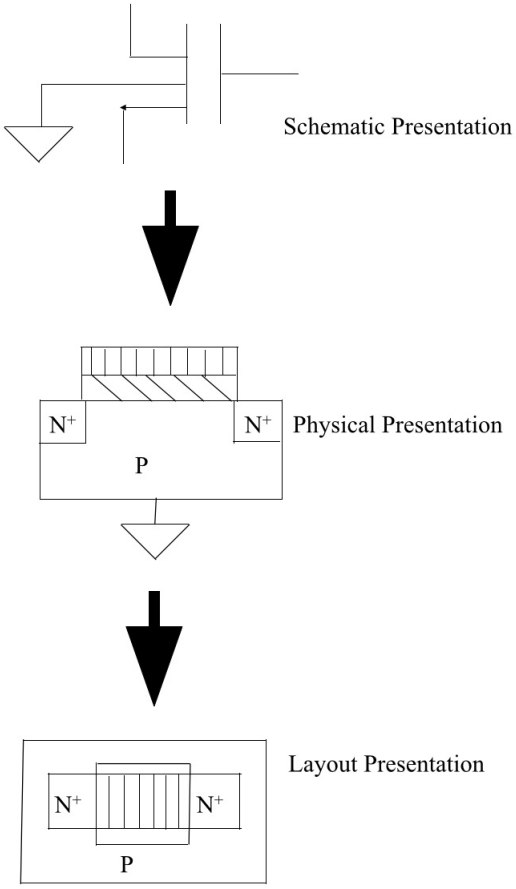

Figure 2.7: Representation of Schematic to Layout Procedure

As shown in Figure 2.7 to fabricate a circuit, schematic is presented through layout. To minimize the effects of mismatch several layout techniques are considered. Various factors considered to counter the effect of random process variations are:

1. Mirror symmetry [6] where all transistors are mirror images of each other. This saves area but introduces sensitivity to alignment shifts in an IC.

2. To overcome sensitivity to alignment shifts a translational symmetry [6] is considered. In

this symmetry all transistors are copies of each other without rotation.

3. Another consideration is to split each transistor into two pieces. Such a symmetry is known as translational and mirror symmetry [6].
   Sensitivity to process gradient perpendicular to the line of symmetry is a disadvantage of translational symmetry, translational and mirror symmetry.

4. Common centroid symmetry [6] is implemented to overcome the disadvantage of linear process gradient.

5. Temperature gradient [9] is important for layout consideration.

6. Ion implantation [2] occurs alternatively at different angles during fabrication for ensuring the creation of source and drain terminals. So implementation of dummy transistors surrounding the design transistor is critical in order to achieve same threshold voltages as ion implantation occurs from any angle.

These six factors are considered before finalising the design of a circuit.

2.4 Figures of Merit

2.4.1 Sensitivity

The simplest definition of sensitivity is the amount of change in a circuit characteristic occurring due to change in circuit component parameter value(s) [6]. For example aspect ratios, threshold voltages, current mirror gain varies. Device parameter variations from wafer to wafer, chip to chip and device to device results from manufacturing variations. That means current in one sample may deviate more or less from the desired value than in other sample. Random component mismatches occur due to local variations occurring at the time of fabrication.
Sensitivity is given by the following equation:

$$S_x^y = \lim_{\Delta x \to 0} \left[\frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} \right] = \frac{x}{y} \frac{\partial y}{\partial x}. \tag{2.32}$$

In the above mathematical formula of sensitivity, S is the sensitivity while x is changing parameter and y is the characteristic we wish to evaluate with the variation of x. In other words, it

is the percentage change that independent variable x cause to dependent variable y. This ratio is evaluated for minute variations by keeping the limit of change in $\Delta x \to 0$. For an example, sensitivity value 2 with 1% change in x means that dependent variable y is changing by 2% due to 1% change in x.

Chapter 3

Literature Review

Many current reference designs exist depending upon requirements of temperature compensation, use of resistors, low power. References [10]–[15] are some examples. The articles reviewed in this chapter deal with the history and sensitivity aspects of the considered current reference circuit [4].

3.1 Oguey *et al.*, 1997

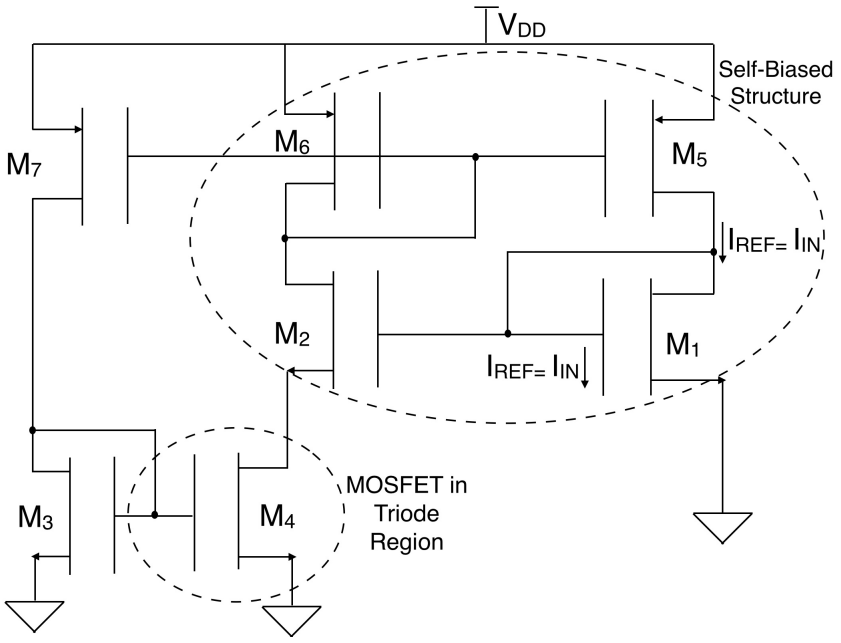

Figure 3.1: Oguey Current Source

The current source [4] presented here replaced a resistor with a MOSFET M_4 working in triode region as shown in Figure 3.1 for micropower applications for the first time. The authors proposed the analysis of NMOS transistors in weak and strong inversion with circuit designed using traditional MOSFET model. All P-MOSFET's are designed to work in strong inversion.

Transistors M_1 and M_2 are working in weak inversion and the voltage at the source of transistor M_2 is given as:

$$V_{S2} = V_T \ln\left(\frac{S_2 S_5}{S_1 S_6}\right), \tag{3.1}$$

where S_1, S_2, S_5, S_6 are aspect ratios of transistors M_1, M_2, M_5, M_6 respectively.

M_4 is working in triode region and M_3 works in saturation region with both of them biased in strong inversion.

The current flowing into the branch of M_3 is given as:

$$I_{D3} = I_{OUT} = \frac{1}{2}\mu_n C_{ox} S_3 (V_{G3} - V_{th})^2. \tag{3.2}$$

As gate and threshold voltages of M_3 and M_4 are same, the current flowing through transistor M_4 using Equation (3.2) is given as:

$$I_{D4} = S_4 \mu_n C_{ox} V_T \ln(K)\left(\sqrt{\frac{2I_{D3}}{\mu_n C_{ox} S_3}} - \frac{nV_T \ln(K)}{2}\right), \tag{3.3}$$

where K is $\frac{S_2 S_5}{S_1 S_6}$ and V_T is thermal voltage. The Equation (3.3) results due to current mirror relation between M_3 and M_4. All MOSFET current source is the key contribution of this paper.

3.2 Serra-Graells *et al.*, 2003

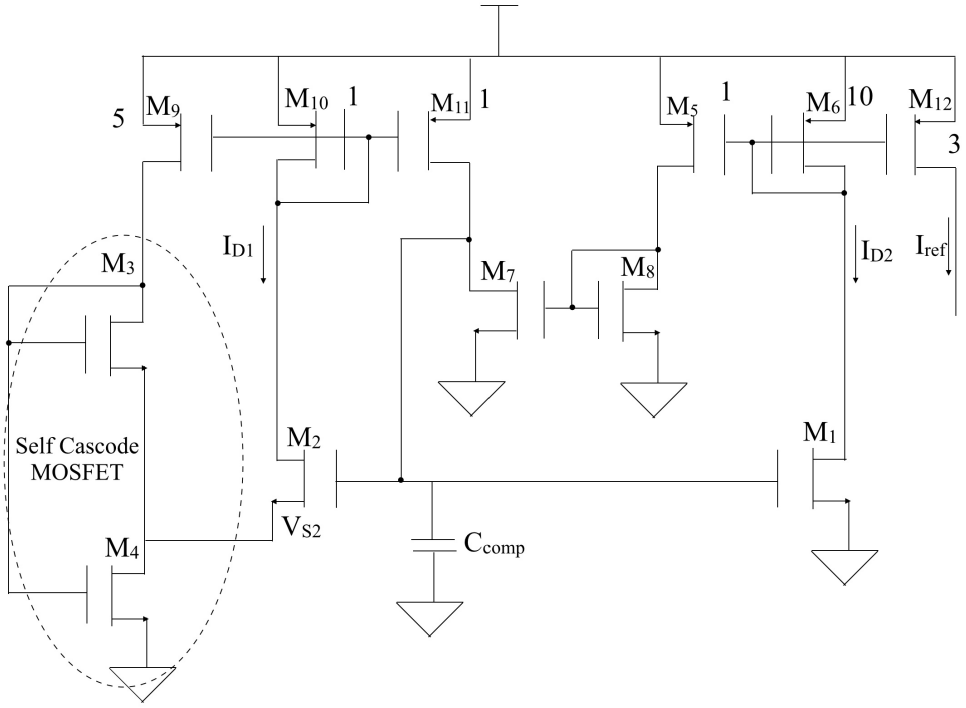

Figure 3.2: Current Reference Circuit of Serra-Graells *et al.*

The paper [16] presents a new MOSFET-only current reference circuit as shown in Figure 3.2. Source of M_2 generates a proportional to absolute temperature (PTAT) voltage. Except for M_1-M_2 that is working in weak inversion saturation region and M_4 that is in strong inversion triode region, all other MOSFET's are working in strong inversion saturation region. The researchers replaced resistor with a self cascode MOSFET of M_3-M_4.

The generated source voltage V_{S2} ensures PTAT behaviour (due to the thermal behaviour of V_T) at the source of M_2 given by the expression:

$$V_{S2} = V_T \ln\left(\frac{S_1 S_6}{S_2 S_{10}}\right), \tag{3.4}$$

where S_1, S_2, S_6, S_{10} are aspect ratio's of transistor M_1, M_2, M_6, M_{10} and $\frac{S_1 S_6}{S_2 S_{10}}$ is K.

Variation in V_{S2} is dependent on the value of K. Less change of V_{S2} achieved with higher value of K and the reverse is also true, therefore it is the major contributor of inaccuracy. Therefore a higher value of K shall be chosen at the design stage. Sensitivity of the reference voltage with

respect to K is analysed in this current reference circuit.

This work is significant because it presents the analysis to achieve a target precision in the PTAT reference voltage (V_{S2}). However, the accuracy of the output current is not considered in the design methodology. Measured current is approximately 10% higher than the designed value. Constraint in this work is that the analysis is done only for M_3 and M_4 working in strong inversion.

3.3 Galeano *et al.*, 2005

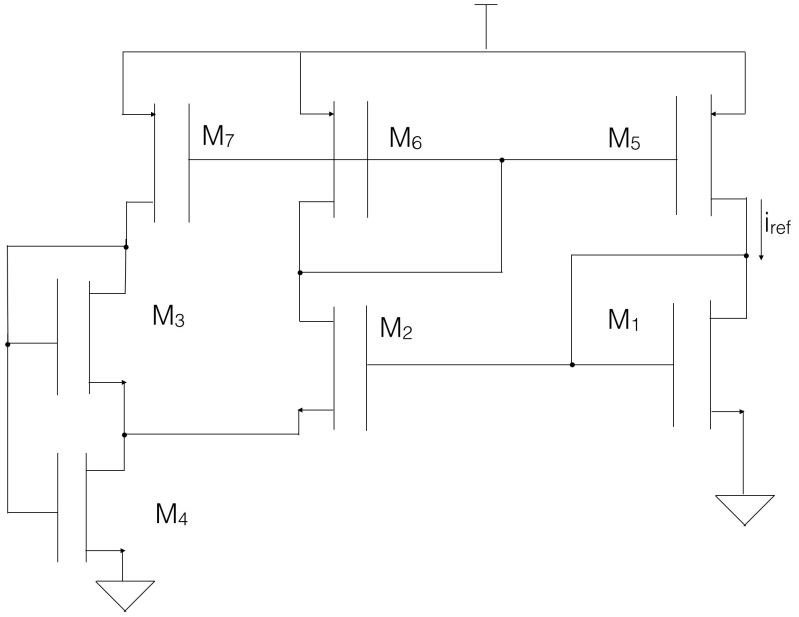

Figure 3.3: Asymmetric Current Reference Circuit of Galeano *et al.*

Galeano *et al.* [1] presented the design of a self biased current reference circuit with the design methodology based on the concept of inversion level for ultra-low power applications. Two topologies are presented in this paper. Figure 3.3 shows the asymmetric version of the circuit as source of transistor M_1 is grounded. PTAT voltage is derived by biasing MOSFET's M_1 and M_2 in weak inversion and achieved output current is proportional to the specific current of MOSFET. The transistors M_3, M_4 are working in moderate inversion to reduce sensitivity of reference current with respect to reference voltage (V_{S2}). Unity gain PMOS current mirrors are

employed in this design.

The sensitivity of reference current i_{ref} to the reference voltage V_{S2} is given as:

$$\frac{\partial i_{ref}/i_{ref}}{\partial V_{S2}} = \frac{2}{V_T}\left[\sqrt{(1+i_{f4})} - \sqrt{1+\frac{i_{f4}}{1+\frac{2S3}{S4}}}\right]^{-1}. \tag{3.5}$$

The design procedure starts by assuming same current in all branches in the reference circuit. According to Equation (3.5), sensitivity depends on $\frac{S3}{S4}$ and i_{f4}. It is shown in [1] that Equation (3.5) decreases with i_{f4}. Therefore i_{f4} should be greater than 3. i_{f1} is arbitrarily selected to put M_1 in weak inversion, i_{f2}=$\frac{i_{f1}}{K}$, i_{f3} is set to 3 and the inversion level i_{f4} is calculated from the following expression:

$$\ln(K) = \sqrt{1+i_{f4}} - 2 + \ln(\sqrt{1+i_{f4}} - 1). \tag{3.6}$$

This method guarantees that i_{f4} is greater than 3, ensuring a reasonable sensitivity. One disadvantage of this approach is the arbitrary selection of inversion level coefficients. This work does not talk about sensitivity analysis for all possible mismatch.

3.4 Rossi *et al.*, 2007

This paper [17] presents MOSFET only PTAT voltage generator driven by a constant inversion level MOSFET current source. The analysis in this section is concentrated on the current generator. The schematic is the same shown in Figure 3.3. All the branches have same current. Except M_4 all transistors are working in saturation leading to the following equation:

$$S_1 i_{f1} = S_2 i_{f2} = S_3 i_{f4} = S_4(i_{f4} - i_{r4}). \tag{3.7}$$

Since gate voltage of transistors M_1 and M_2 are same in Figure 3.1, therefore voltage at the source of M_2 is given as:

$$V_{S2} = V_T[\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2})]. \tag{3.8}$$

$$\mathcal{F}(i_{f4}) = \frac{V_{P4}}{V_T}. \tag{3.9}$$

$$\mathcal{F}(i_{r4}) = \frac{V_{P4} - V_{D4}}{V_T}. \tag{3.10}$$

Since V_{G3}=V_{G4} and V_{S3}=V_{D4} it follows that $\mathcal{F}(i_{f3})$=$\mathcal{F}(i_{r4})$ and this implies:

$$i_{f3} = i_{r4}. \tag{3.11}$$

Also from Equation (2.6):

$$\mathcal{F}(i_{f4}) - \mathcal{F}(i_{r4}) = \frac{V_{D4}}{V_T}. \tag{3.12}$$

Combining Equation (3.8), (3.11) and (3.12) noting that V_{D4}=V_{S2} results in the following relation:

$$\mathcal{F}(i_{f4}) - \mathcal{F}(i_{r4}) = \mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2}). \tag{3.13}$$

Equation (3.7) and Equation (3.13) completely determine all the inversion levels, given the aspect ratios of the transistors, therefore inversion coefficients are constant independent of temperature and the branch currents are proportional to the sheet normalization current I_{SQ}. Hence, the source becomes MOS-only constant inversion level current source. It is important to note that Equation (3.13) is valid even if M_1 or M_2 are not in weak inversion.

3.5 Luong *et al.*, 2014

The literature review in context of this thesis [18] discusses the current source as shown in Figure 3.3 designed for providing bias current to the voltage reference circuit.

This work does not analyze the trade off between constant inversion level current sensitivity with respect to circuit parameters and area and does not discusses the effect of variation of parameters on the current reference circuit. There is a mismatch between simulated and measured values that motivates the work done in this thesis. The current source was designed for 0.6 nA in each branch but measured values ranged from 0.33 nA to 0.53 nA in five samples.

Chapter 4

Sensitivity and Mismatch Analysis

This chapter presents an in depth sensitivity analysis of the current reference circuit presented in [4]. All parameter fluctuations in the equations are considered.
The first section concentrates on developing a model to analyze the effect of random mismatches in current reference circuit. Section 4.1 presents the equations for all sensitivities. The most important sensitivities are then plotted over a wide range in the design space and finally existing designs from the literature are analyzed using the proposed model.

4.1 Notation and Equation Formulation

All derivations presented in this chapter follow Figure 4.1. k_1, k_2 are gains of PMOS mirror and $R=\frac{I_{SQ3}S3}{I_{SQ4}S4}$.

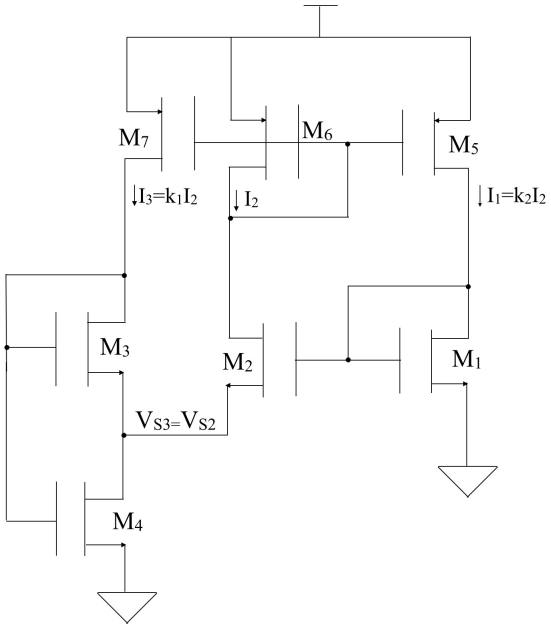

Figure 4.1: Current Source Circuit

For this current source circuit to work following equation [14], [19] must be satisfied:

$$\frac{1}{k_2} I_{D1} = I_{D2} = \frac{1}{k_1} I_{D3} = \frac{1}{(k_1+1)} I_{D4}. \tag{4.1}$$

The analysis in this chapter relies on the following definitions:

$$K = \frac{i_{f1}}{i_{f2}} = k_2 \frac{I_{SQ2} S2}{I_{SQ1} S1}. \tag{4.2}$$

$$M = \frac{i_{f3}}{i_{f2}} = k_1 \frac{I_{SQ2} S2}{I_{SQ3} S3}. \tag{4.3}$$

$$D = \frac{i_{f4}}{i_{f3}} = 1 + R\left(\frac{1+k_1}{k_1}\right). \tag{4.4}$$

Combining Equation (3.13), (4.2), (4.3) and (4.4) leads to the following error function that only depends on i_{f2}, K, M, D, n_1, n_2, n_3, n_4, ΔV_{th12} and ΔV_{th34} :

$$G(i_{f2}) = \frac{n_4}{n_3}\mathcal{F}(MDi_{f2}) - \mathcal{F}(Mi_{f2}) + \mathcal{F}(i_{f2}) - \frac{n_1}{n_2}\mathcal{F}(Ki_{f2}) - \frac{\Delta V_{th12}}{n_2 V_T} + \frac{\Delta V_{th34}}{n_3 V_T} = 0. \tag{4.5}$$

The derivative of error function ($G'(i_{f2})$) with respect to i_{f2} is given as:

$$\frac{\partial G}{\partial i_{f2}} = \mathrm{G}'(i_{f2}) = \frac{n_4}{n_3}\frac{\partial \mathcal{F}(MDi_{f2})}{\partial i_{f2}} - \frac{\partial \mathcal{F}(Mi_{f2})}{\partial i_{f2}} + \frac{\partial \mathcal{F}(i_{f2})}{\partial i_{f2}} - \frac{n_1}{n_2}\frac{\partial \mathcal{F}(Ki_{f2})}{\partial i_{f2}}. \tag{4.6}$$

For calculation of sensitivity with respect to K, M, k_1 and R threshold voltages, slope factors are considered to be perfectly matched. The sensitivity with respect to threshold voltage mismatch is calculated by assuming that rest all parameters are perfectly matched. Similar is true for slope factor mismatch where we consider that parameters K, M, k_1, R are perfectly matched with no difference between the threshold voltages.

4.2 Mismatch Analysis

This section takes into consideration all the possible mismatch due to terms in the equations that can occur in this current reference circuit. The sensitivities are derived by taking into account one mismatch at a time.

All sensitivities are measured in %/% except sensitivity with respect to ΔV_{th} which has %/mV as its unit. $\mathcal{F}'$ is defined as:

$$\mathcal{F}' = \frac{\partial \mathcal{F}(i_f)}{\partial i_f}. \tag{4.7}$$

4.2.1 Sensitivity with respect to K

The following equation studies the effect of change in K on the inversion level of i_{f2}.

Differentiating Equation (4.5) with respect to K yields:

$$\frac{\partial \mathrm{G}}{\partial K} = -i_{f2}\frac{n_1}{n_2}\mathcal{F}'(Ki_{f2}). \tag{4.8}$$

The sensitivity of i_{f2} with respect to K is simplified as:

$$S_K^{i_{f2}} = \frac{\partial i_{f2}}{\partial K} \times \frac{K}{i_{f2}} = -\frac{\partial \mathrm{G}}{\partial K} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{K}{i_{f2}} = \frac{n_1}{n_2}\mathcal{F}'(Ki_{f2}) \times \frac{K}{\mathrm{G}'(i_{f2})}. \tag{4.9}$$

4.2.2 Sensitivity with respect to M

To determine the sensitivity of i_{f2} to M, differentiating Equation (4.5) with respect to M yields:

$$\frac{\partial \mathrm{G}}{\partial M} = \frac{n_4}{n_3}Di_{f2}\mathcal{F}'(MDi_{f2}) - i_{f2}\mathcal{F}'(Mi_{f2}). \tag{4.10}$$

A simplified expression for the effect on i_{f2} for a smaller variation in M is quantified as:

$$S_M^{i_{f2}} = \frac{\partial i_{f2}}{\partial M} \times \frac{M}{i_{f2}} = -\left(\frac{n_4}{n_3}D\mathcal{F}'(MDi_{f2}) - \mathcal{F}'(Mi_{f2})\right) \times \frac{M}{\mathrm{G}'(i_{f2})}. \tag{4.11}$$

4.2.3 Sensitivity with respect to k_1

Differentiating Equation (4.5) with respect to k_1 yields:

$$\frac{\partial \mathrm{G}}{\partial k_1} = i_{f2}\bigg(-\mathcal{F}'(Mi_{f2})\frac{I_{SQ2}S2}{I_{SQ3}S3} + \frac{n_4}{n_3}\mathcal{F}'(MDi_{f2})\bigg(\frac{I_{SQ2}S2}{I_{SQ3}S3}D - M\frac{R}{k_1}\bigg)\bigg). \tag{4.12}$$

The sensitivity of i_{f2} with respect to k_1 is simplified as:

$$S_{k_1}^{i_{f2}} = \frac{\partial i_{f2}}{\partial k_1} \times \frac{k_1}{i_{f2}} = -\frac{\partial \mathrm{G}}{\partial k_1} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{k_1}{i_{f2}}. \tag{4.13}$$

4.2.4 Sensitivity with respect to R

To study the effect of variation in R on i_{f2}, differentiating Equation (4.5) with respect to R:

$$\frac{\partial \mathrm{G}}{\partial R} = \frac{n_4}{n_3}\bigg(1 + \frac{1}{k_1}\bigg)Mi_{f2}\mathcal{F}'(MDi_{f2}). \tag{4.14}$$

The sensitivity of i_{f2} with respect to R is expressed as:

$$S_R^{i_{f2}} = \frac{\partial i_{f2}}{\partial R} \times \frac{R}{i_{f2}} = -\frac{n_4}{n_3}\bigg(1 + \frac{1}{k_1}\bigg)M\mathcal{F}'(MDi_{f2}) \times \frac{R}{\mathrm{G}'(i_{f2})}. \tag{4.15}$$

4.2.5 Sensitivity with respect to sheet normalisation current

Sensitivity of i_{f2} with respect to sheet normalisation current (I_{SQ}) in M_1 and M_2 is considered as:

$$S_{\frac{I_{SQ2}}{I_{SQ1}}}^{i_{f2}} = S_{k_2}^{i_{f2}} = S_{\frac{S2}{S1}}^{i_{f2}} = S_K^{i_{f2}}. \tag{4.16}$$

Also, similar analysis in M_2 and M_3 is considered as:

$$S_{\frac{I_{SQ2}}{I_{SQ3}}}^{i_{f2}} = S_{k_1}^{i_{f2}} = S_{\frac{S2}{S3}}^{i_{f2}} = S_M^{i_{f2}}. \tag{4.17}$$

Another similar analysis in M_3 and M_4 is considered as:

$$S_{\frac{I_{SQ3}}{I_{SQ4}}}^{i_{f2}} = S_{\frac{S3}{S4}}^{i_{f2}} = S_R^{i_{f2}}. \tag{4.18}$$

4.2.6 Sensitivity with respect to threshold voltage mismatch between transistor M_1 and M_2

The derivative of Equation (4.5) with respect to ΔV_{th12} is quantified as :

$$\frac{\partial G}{\partial(\Delta V_{th12})} = -\frac{1}{n_2 V_T}. \tag{4.19}$$

The following equation studies the effect of change in V_{th12} on the inversion level of i_{f2}.
The sensitivity equation for ΔV_{th12} is given as:

$$S^{i_{f2}}_{(\Delta V_{th12})} = \frac{\partial i_{f2}}{\partial(\Delta V_{th12})} \times \frac{1}{i_{f2}} \times 100 = \frac{1}{n_2 V_T} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}} \times 100. \tag{4.20}$$

4.2.7 Sensitivity with respect to threshold voltage mismatch between Transistor M_3 and M_4

Following an analysis similar to Section 4.2.6 but the derivative of Equation (4.5) with respect to ΔV_{th34} is quantified as:

$$\frac{\partial G}{\partial(\Delta V_{th34})} = \frac{1}{n_3 V_T}. \tag{4.21}$$

The following equation studies the effect of change in V_{th} on the inversion level of i_{f2}. The sensitivity equation for ΔV_{th34} is given as:

$$S^{i_{f2}}_{(\Delta V_{th34})} = \frac{\partial i_{f2}}{\partial(\Delta V_{th34})} \times \frac{1}{i_{f2}} \times 100 = -\frac{1}{n_3 V_T} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}} \times 100. \tag{4.22}$$

Since slope factor of M_1, M_2, M_3 and M_4 are same and thermal voltage is same for all the transistors therefore only one sensitivity due threshold voltage mismatch is calculated.

4.2.8 Sensitivity with respect to slope factor mismatch between M_1 and M_2

The derivative of Equation (4.5) is quantified as:

$$\frac{\partial G}{\partial \frac{n_1}{n_2}} = -\mathcal{F}(K i_{f2}). \tag{4.23}$$

The following equation studies the effect of change in $\frac{n_1}{n_2}$ on the inversion level of i_{f2}.
The sensitivity equation for $\frac{n_1}{n_2}$ is given as:

$$S^{i_{f2}}_{\frac{n_1}{n_2}} = \frac{\partial i_{f2}}{\partial \frac{n_1}{n_2}} \times \frac{1}{i_{f2}} = -\frac{\partial G}{\partial \frac{n_1}{n_2}} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}} = \mathcal{F}(K i_{f2}) \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}}. \tag{4.24}$$

4.2.9 Sensitivity with respect to slope factor Mismatch of Transistor M_3 and M_4

The derivative of Equation (4.5) with respect to $\frac{n_1}{n_2}$ is quantified as:

$$\frac{\partial G}{\partial \frac{n_4}{n_3}} = \mathcal{F}(MDi_{f2}). \tag{4.25}$$

The following equation studies the effect of change in $\frac{n4}{n3}$ on the inversion level of i_{f2}. The sensitivity equation for changes in $\frac{n_4}{n_3}$ is quantified as::

$$S^{i_{f2}}_{\frac{n_4}{n_3}} = \frac{\partial i_{f2}}{\partial \frac{n_4}{n_3}} \times \frac{1}{i_{f2}} = -\frac{\partial G}{\partial \frac{n_4}{n_3}} \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}} = -\mathcal{F}(MDi_{f2}) \times \frac{1}{\mathrm{G}'(i_{f2})} \times \frac{1}{i_{f2}}. \tag{4.26}$$

4.3 Area Figure of Merit (AFM)

The Area Figure of Merit (AFM) is intended to compare the area requirements of a design:

$$AFM \propto W_u \times L_u \times N_u, \tag{4.27}$$

where $W_u \times L_u$ is the gate area of a unit transistor and N_u is the total number of unit transistors in the design. Assuming W_u is constant equal to the minimum allowable for a given matching requirement, AFM is proportional to length (L_u) of unit transistor times the number of unit transistors (N_u):

$$AFM \propto L_u \times N_u. \tag{4.28}$$

The AFM is valid by assuming one unit transistor is used for transistor M_1. This is a reasonable choice if the current source is expected to produce a very low current in order of few nA or less. It is important to note that AFM only consider the area of N-MOSFET's. L_u is given in terms of width (W_u), inversion level (i_{f1}) of transistor M_1, current I_{D1} flowing into transistor M_1 and sheet normalisation current I_{SQ} as:

$$L_u = \frac{I_{SQ} W_u i_{f1}}{I_{D1}} \propto i_{f1} = K i_{f2}. \tag{4.29}$$

N_u is calculated from the design parameters as follows:

$$M_1 = 1. \tag{4.30}$$

$$M_2 = \frac{K}{k_2}. \tag{4.31}$$

$$M_3 = \frac{k_2}{k_1} \times \frac{M}{K}. \tag{4.32}$$

$$M_4 = \frac{k_2}{(k_1+1)} \times (D-1) \times \frac{M}{K}. \tag{4.33}$$

$$N_u = M_1 + M_2 + M_3 + M_4. \tag{4.34}$$

M_1 and M_2 require higher width over length ratio [16] as they are in weak inversion and hence they will be implemented as parallel association of unit transistors. On the contrary M_3 and M_4 are implemented as series association of unit transistors as they are working in moderate or in strong inversion.

4.4 Exploration of Design Space

This section interpret sensitivities graphically. Since 4D plots are not possible, individual plots for variation in K, M, D are shown for sensitivity. Following is the broad range for different parameters in order to consider all possible values that can affect sensitivity:

1. $D \ \epsilon$ (2,12)
2. $K \ \epsilon$ (8,30)
3. $M \ \epsilon$ (40,600)

This paragraph explains the script A.1 that plot sensitivity graphs presented in this section. For a given combination of K, M and D, Equation (4.5) is solved to obtain i_{f2} using bisection method and then graphs are plotted for all possible sensitivities presented in section 4.1. For example, Figure 4.2 shows the lowest sensitivities for each value of K when D and M are allowed to take any value in the considered range. Sensitivity plots do not include sensitivity respect to k_1, M because they are always lower than $S_R^{i_{f2}}$ and $S_K^{i_{f2}}$. Sensitivity with respect to k_1 and k_2 are not included in the graphs presented in this section because both of them are always less than sensitivity with respect to R and K.

4.4.1 Effects of K

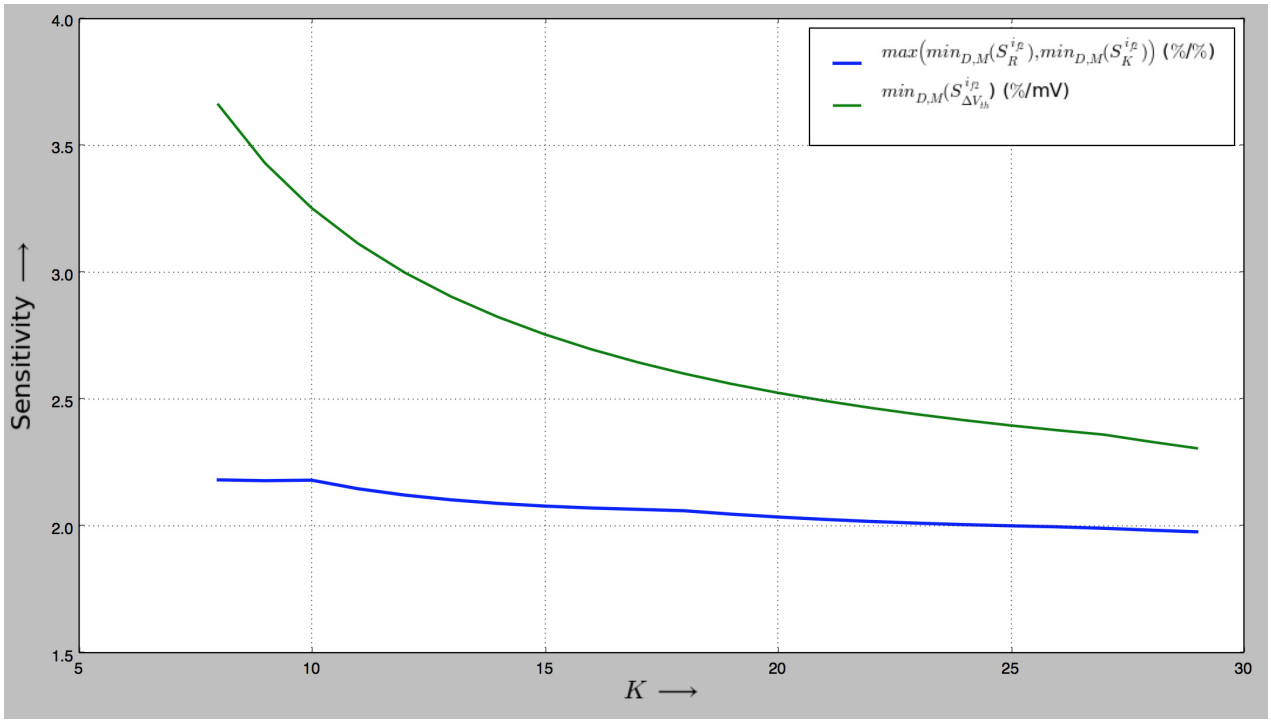

Figure 4.2: Effect of K on Sensitivities

The graph presented in this section show the best possible sensitivities for a given combination of D and M for each value of K. Figure 4.2 shows $max\left(min_{D,M}(S_R^{if2}), min_{D,M}(S_K^{if2})\right)$ and $min_{D,M}(S_{\Delta V_{th}}^{if2})$ versus K. The value of K does not affect much $max\left(min_{D,M}(S_R^{if2}), min_{D,M}(S_K^{if2})\right)$, but it has significant effect on $min_{D,M}(S_{\Delta V_{th}}^{if2})$. As expected, the greater K, the better.

4.4.2 Effects of M

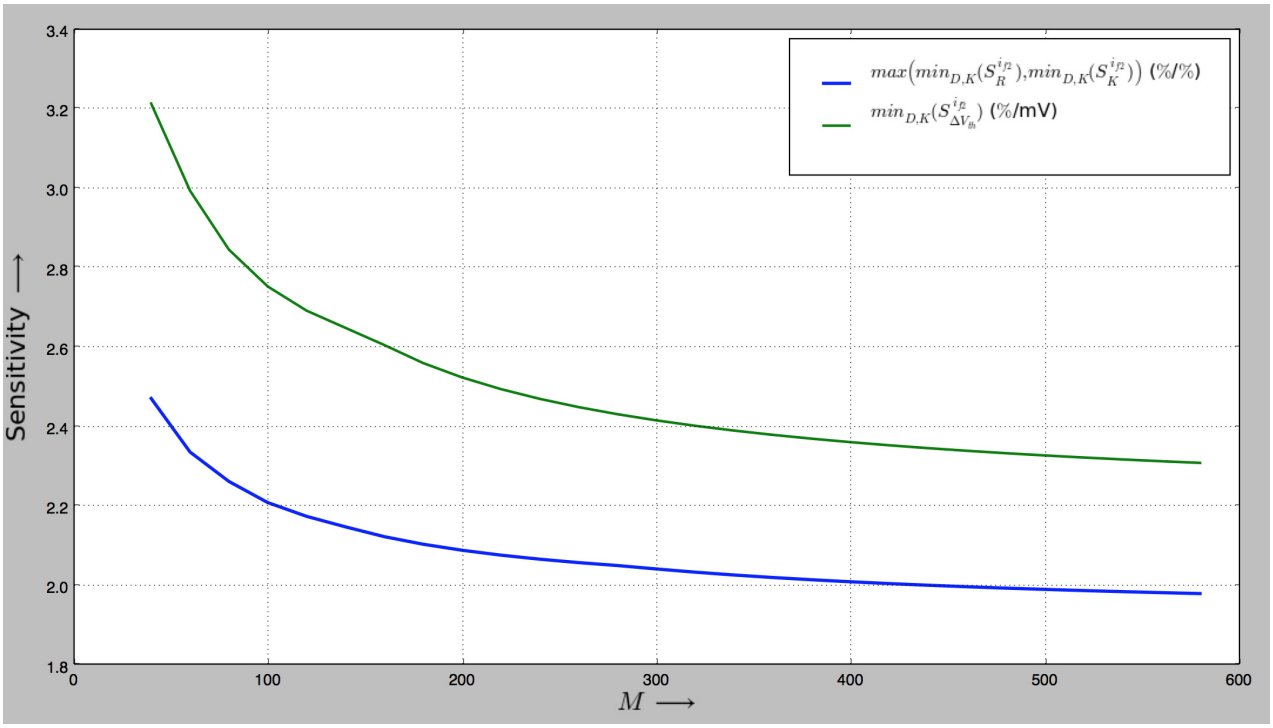

Figure 4.3: Effect of M on Sensitivities

The graph presented in this section show the best possible sensitivities for a given combination of D and K for each value of M. Figure 4.3 shows $max\left(min_{D,K}(S_R^{if2}), min_{D,K}(S_K^{if2})\right)$ and $min_{D,K}(S_{\Delta V_{th}}^{if2})$ versus M. The value of M has significant effect on $max\left(min_{D,K}(S_R^{if2}), min_{D,K}(S_K^{if2})\right)$ and $min_{D,K}(S_{\Delta V_{th}}^{if2})$. Therefore as M increases, sensitivity decreases.

4.4.3 Effects of D

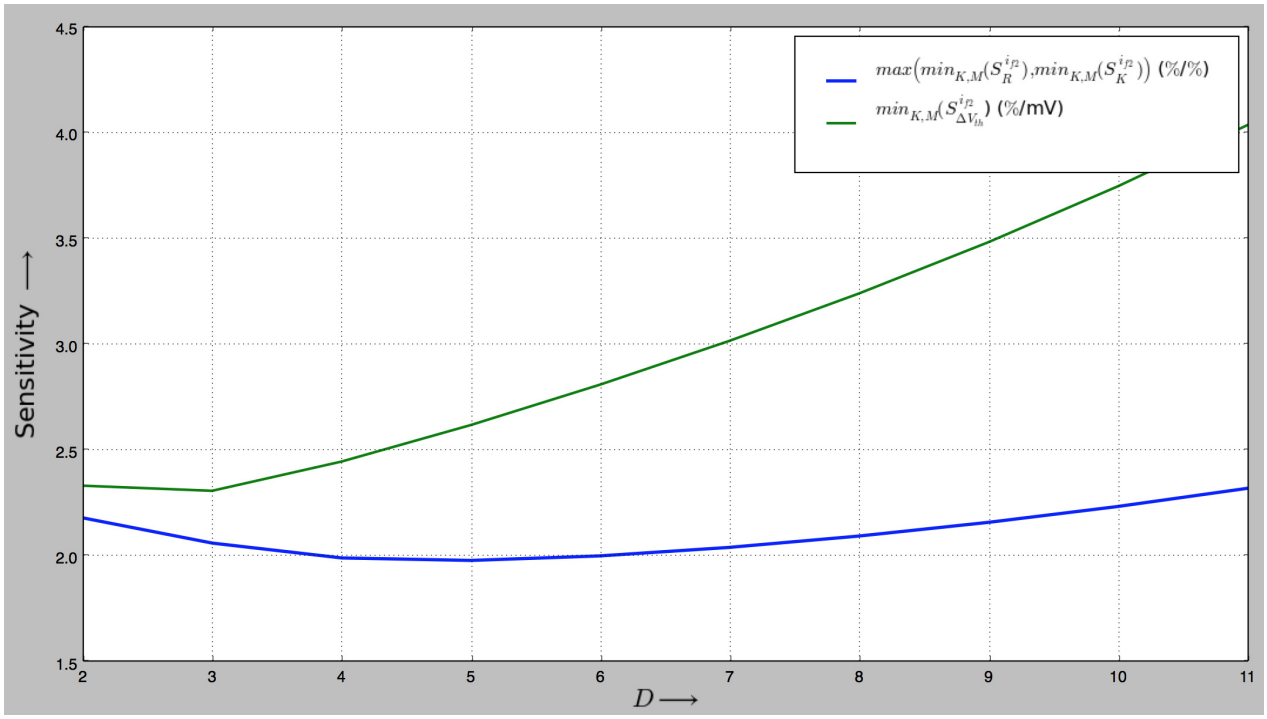

Figure 4.4: Effect of D on Sensitivities

The graphs presented here show the best possible sensitivities for a given combination of M and K for each value of D. A plot of Sensitivities versus D in Figure 4.4, plots maximum of minimum sensitivity respect to R and K. The other plotted sensitivity is with respect to ΔV_{th}. This suggest an initial rise in D, the sensitivities decreases but a rise in both the sensitivities are observed afterwards as indicated by Figure 4.4, of Sensitivity versus D plot. For a given sensitivity this plot suggest optimum D.

4.5 Random Mismatches

This section follows [20]. The standard deviation of the difference between the threshold voltages of two identical transistors is given as:

$$\sigma(\Delta V_{th}) = \frac{A_{VT}}{\sqrt{WL}}, \tag{4.35}$$

where

$$A_{VT}(mV\mu m) \simeq t_{ox}(nm), \tag{4.36}$$

is threshold mismatching coefficient. t_{ox} is oxide thickness. So it can be said that increase in gate area (WL) can help in reducing threshold voltage mismatch.

The current factor difference $\Delta\beta$ (β=$\mu C'_{ox}\frac{W}{L}$) between pairs of matched transistors is modelled as:

$$\frac{\Delta\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}}. \tag{4.37}$$

Typical values of A_β (change in the value is insignificant with technology scaling) ranges from 1% μm to 3% μm.

Assuming the transistors to be identical in terms of same source and gate voltages having uncorrelated V_{th}, β, the normalised standard deviation of current mirror is quantified as:

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left(\frac{A_\beta}{\sqrt{WL}}\right)^2 + \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_{th})}. \tag{4.38}$$

The largest mismatch occurs in weak inversion:

$$\frac{\sigma(\Delta I_D)}{I_D} \simeq \frac{\sigma(\Delta V_{th})}{nV_T}. \tag{4.39}$$

The minimum mismatch occurs in strong inversion.

4.6 Analysis of Previous Designs

All the calculations presented in this section use the parameters extracted from the original work with different unit transistors for each research article [1], [16], [18]. All of them have different drain currents. Table (4.1) lists design parameters for three key references. Table (4.2) lists the inversion level coefficient for transistors M_1, M_2, M_3 and M_4 for the three works done in literature. i_{f1} and i_{f2} for [16] is an educated guess based on the assumption that M_1 and M_2 are working in weak inversion and the reported gate area.

Table (4.3) list sensitivity evaluation for different parameters for three key references. The AFM for Serra-Graells *et al.* is worse than the other two because of higher k_1 and k_2 however that result in better sensitivity.

Parameters	Galeano *et al.* [1]	Luong *et al.* [18]	Serra-Graells *et al.* [16]
M	225	320	848
D	3.4	3.2	1.6
K	9	8	10
k_1	1	1	5
k_2	1	1	10
R	1.2	1.1	0.5

Table 4.1: Parameter Comparison of Literature Review

Inversion level	Galeano *et al.* [1]	Luong *et al.* [18]	Serra-Graells *et al.* [16]
i_{f1}	0.144	0.086	0.9
i_{f2}	0.016	0.01	0.09
i_{f3}	3	3.2	76.34
i_{f4}	10.2	10.24	122.15

Table 4.2: Inversion Level of N-MOSFET

Sensitivity	Galeano *et al.* [1]	Luong *et al.* [18]	Serra-Graells *et al.* [16]
$S_R^{i_{f2}}$ (%/%)	2.36	2.38	2.43
$S_{k_1}^{i_{f2}}$ (%/%)	0.15	0.17	0.83
$S_K^{i_{f2}}$ (%/%)	1.57	1.64	1.33
$S_M^{i_{f2}}$ (%/%)	1.05	1.03	1.23
$S_{\frac{n1}{n2}}^{i_{f2}}$ (%/%)	5.39	6.75	1.5
$S_{\frac{n4}{n3}}^{i_{f2}}$ (%/%)	7.85	8.29	28.99
$S_{\Delta V_{th}}^{i_{f2}}$ (%/mV)	4.49	4.74	3.17
AFM	8.41	7.48	213.266

Table 4.3: Sensitivity Result Comparison of Literature Review

In Table 4.4, σ_R is standard deviation of variation in R calculated as:

$$\sigma_R = max(\sigma(S3), \sigma(S4)) = max\left(\frac{A_\beta}{\sqrt{(WL)_3}}, \frac{A_\beta}{\sqrt{(WL)_4}}\right). \tag{4.40}$$

Standard deviation of changes in k_1 is symbolised as σ_{k_1} given by Equation (4.38). Taking a clue from Equation (4.2).

The standard deviation of product of two independent or uncorrelated variable is given as [21]:

$$\sigma_{XY} = \sqrt{\sigma^2{}_X[E(Y)]^2 + \sigma^2{}_Y[E(X)]^2 + \sigma^2{}_X\sigma^2{}_Y}. \tag{4.41}$$

As all standard deviations are normalized therefore E(X)=E(Y)=1. Hence Equation (4.41) is reduced to:

$$\sigma_{XY} = \sqrt{\sigma^2{}_X + \sigma^2{}_Y + \sigma^2{}_X\sigma^2{}_Y}. \tag{4.42}$$

As K is given by Equation (4.2) σ_K which is a normalised standard deviation of variation in K is calculated as:

$$\sigma_K = \sqrt{\sigma^2_{k_2}\sigma^2_{12} + \sigma^2_{k_2} + \sigma^2_{12}}, \tag{4.43}$$

where is σ_{12}=$max(\sigma(I_{SQ1}S_1), \sigma(I_{SQ2}S_2))$.

Similarly σ_M is quantified as:

$$\sigma_M = \sqrt{\sigma^2{}_{k_1}\sigma^2_{23} + \sigma^2_{k_1} + \sigma^2_{23}}. \tag{4.44}$$

where σ_{23}=$max(\sigma(I_{SQ2}S_2), \sigma(I_{SQ3}S_3))$.

The standard deviation of the difference between the threshold voltages of M_1-M_2 is given as:

$$\sigma_{\Delta V_{th12}} = max\left(\frac{A_{Vt}}{\sqrt{(WL)_1}}, \frac{A_{Vt}}{\sqrt{(WL)_2}}\right). \tag{4.45}$$

A similar expression for standard deviation of the difference between the threshold voltages of M_3-M_4, $\sigma_{V_{th34}}$ can be given as:

$$\sigma_{\Delta V_{th34}} = max\left(\frac{A_{Vt}}{\sqrt{(WL)_3}}, \frac{A_{Vt}}{\sqrt{(WL)_4}}\right). \tag{4.46}$$

The mismatch of $\frac{n_1}{n_2}$ and $\frac{n_4}{n_3}$ is expected to be low because each transistor in the pair has the same gate voltage. Since we do not have any way to analyse this, the corresponding sensitivity should be kept not too high. Mismatch of k_1, K and M for [16] cannot be estimated due to missing data about PMOS mirror. Area of PMOS mirror are main contributor for higher σ_K and σ_M.

Table 4.5 presents the standard deviation in i_{f2} due to each source of mismatch. The results in this table suggest that K, M and V_{th12} introduces greatest mismatch. All the three parameters shall be improved by carefully designing PMOS current mirror. The sensitivity and standard

Circuit Parameter Standard Deviation	Galeano *et al.* [1]	Luong *et al.* [18]	Serra-Graells *et al.* [16]
σ_R (%)	0.05	0.14	0.58
σ_{k_1} (%)	9.7	7.85	n/a
σ_K (%)	9.72	7.94	n/a
σ_M (%)	10.14	7.87	n/a
$\sigma_{\Delta V_{th12}}$ (mV)	2.5	1.52	1.42
$\sigma_{\Delta V_{th34}}$ (mV)	1.42	0.24	0.8

Table 4.4: Circuit Parameter Standard Deviation

$\frac{\sigma(i_{f2})}{i_{f2}}$ %	Galeano *et al.* [1]	Luong *et al.* [18]	Serra-Graells *et al.* [16]
$S_R^{i_{f2}} \times \sigma_R$	0.12	0.34	1.42
$S_{k_1}^{i_{f2}} \times \sigma_{k_1}$	1.46	1.53	n/a
$S_K^{i_{f2}} \times \sigma_K$	15.27	13.03	n/a
$S_M^{i_{f2}} \times \sigma_M$	10.65	8.11	n/a
$S_{\Delta V_{th12}}^{i_{f2}} \times \sigma_{\Delta V_{th12}}$	11.23	7.21	4.51
$S_{\Delta V_{th34}}^{i_{f2}} \times \sigma_{\Delta V_{th34}}$	6.38	1.14	2.54

Table 4.5: Multiplication of Sensitivity and Standard Deviation of each parameter ($\frac{\sigma(i_{f2})}{i_{f2}}$ %)

deviation for ΔV_{th} are worst in case of [1], whereas in [18] sensitivity and standard deviation for ΔV_{th} is less for $M3$, $M4$ compared with other designs but ΔV_{th} sensitivity and standard deviation for $M1$, $M2$ in [18] are higher than [16] and less than [1].

Chapter 5

Proposed Design Methodology

This chapter explain proposed design methodology with design example. Results of the design example is compared with [18]. Circuit simulation is also presented to verify proposed design method.

5.1 Design Objective

The objective of the design is to re-design current source in [18] with identical or better performance and less area. The current source is designed for a total current consumption of 1.8 nA in AMS 0.35 μm technology with less than 70 unit transistors while consuming not more than 1518 μm^2 of total gate area. Another specification is achieving less than 13.03% of maximum $\frac{\sigma(i_{f2})}{i_{f2}}$.

5.2 Design Procedure

The following steps shall be followed for an efficient current reference design. The design is divided into three sections.

5.2.1 Sensitivity and Area Selection

Following five steps guide helps in selecting a good compromise between sensitivity and area.

1. Plan a good layout design of the current source. Select k_1, k_2, M and K based on the layout plan.

2. Sweep D to obtain promising sensitivity values and area with a reasonable compromise between sensitivities and AFM.

3. Iterate step 1 and 2 until a satisfactory result is obtained.

4. Use integer number of unit transistors.

5. Recalculate i_{f1}, i_{f2}, i_{f3}, i_{f4} and all the sensitivities.

5.2.2 Design of NMOS Section

NMOS shall be designed by following the three steps procedure:

1. Calculate unit transistor size for a given inversion level, I_{SQ} and drain current I_D.

2. From:

   (a) $S_R^{i_{f2}} \times \sigma_R$

   (b) $S_K^{i_{f2}} \times \sigma_{K_{NMOS}}$

   (c) $S_M^{i_{f2}} \times \sigma_{M_{NMOS}}$

   (d) $S_{\Delta V_{th12}}^{i_{f2}} \times \sigma_{\Delta V_{th12}}$

   (e) $S_{\Delta V_{th34}}^{i_{f2}} \times \sigma_{\Delta V_{th34}}$

   Find the maximum symbolized as σ_{MAX}.

3. Try reducing σ_{MAX} by increasing NMOS transistor gate area.

5.2.3 PMOS Mirror Design

PMOS current mirror plays vital role in mismatch analysis therefore careful design of PMOS current mirror is important. This can be done by deriving minimum PMOS gate area from the following:

1. $S_{M_{NMOS}}^{i_{f2}} \times \sigma_{k1} \leqslant \sigma_{MAX}$.
   The maximum mismatch shall be greater than $S_{M_{NMOS}}^{i_{f2}} \times \sigma_{k1}$.

2. $S_{k_1}^{i_{f2}} \times \sigma_{k_1} \leqslant \sigma_{MAX}$
   Using step 2 minimum gate area for PMOS M_7 in Figure 5.1 is obtained.

3. $S_{K_{NMOS}}^{i_{f2}} \times \sigma_{k_2} \leqslant \sigma_{MAX}$

   This step derive the minimum gate area for M_5 and M_6 of Figure 5.1. The steps followed in designing PMOS mirror will help reducing the mismatch in k_1 and k_2 depending upon the expected $\frac{\sigma_{i_{f2}}}{i_{f2}}$.

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5.3 Design Example

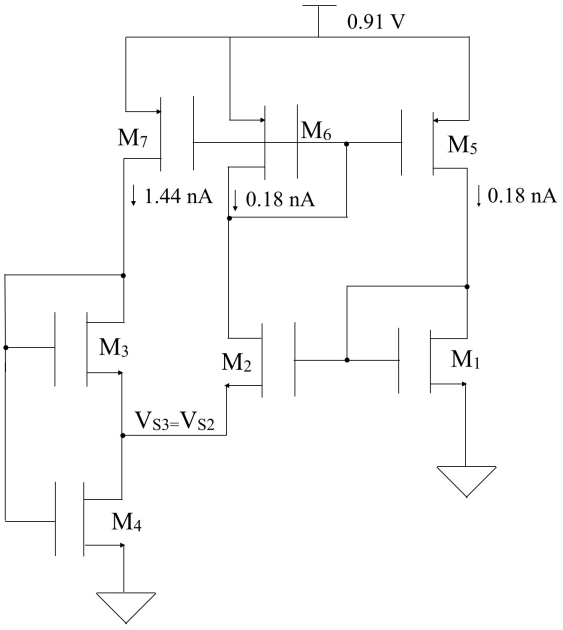

Figure 5.1: Current Source Circuit

5.3.1 Sensitivity and Area Selection

M3 M2 M2 M2 M2 M2 M2 M3

M3 M2 M1 M1 M1 M1 M2 M3

M3 M2 M2 M2 M2 M2 M2 M3

Figure 5.2: Layout Plan

1. Figure 5.2 depicts a common centroid layout. In the plan 4 M_1 transistors in series-parallel combination are surrounded by 14 M_2 transistors connected in parallel. For a well matched layout consideration, $K=\frac{S_{M2}}{S_{M1}}=\frac{i_{f1}}{i_{f2}}=14$. Thus M_2 surrounds M_1 from all the directions. 6 M_3 transistors in series surround 6 M_2 transistors vertically. As shown in Figure 5.3, transistor M_1 is connected in a series-parallel combination making it a single unit transistor to reduce σ_K presented by Equation (4.43) and $\sigma_{V_{th12}}$ presented by Equation (4.45). M_2 is connected as a parallel association of unit transistors due to weak inversion level as it require higher aspect ratio. However M_3 and M_4 are in moderate inversion therefore they are connected as series association of unit transistors due to the requirement of low aspect ratio. $\frac{S_2}{S_3}$ is selected as 84 but k_1=1 makes it very small leading to higher sensitivity values. To accomplish a better trade-off between sensitivity and area, selected k_1, k_2, M and K are shown in Table 5.1. k_1 is selected as 8 so that PMOS mirror units have branches in parallel. A higher value of k_1 results in reduced sensitivity. k_2 is kept as 1 since higher k_2 causes increment in AFM. The value of K is selected as 14 for common centroid layout and to lower sensitivities. Assuming same sheet normalisation current, $\frac{S_2}{S_3}$, k_1 and using Equation (4.3) higher M as 672 is achieved, therefore helping in reduction of sensitivities. The branch of M_1 and M_2 generates 0.18 nA of current while 1.44 nA (8 $\times$ 0.18 nA) of current is fed to the branch of M_3. Therefore total current is 1.8 nA.

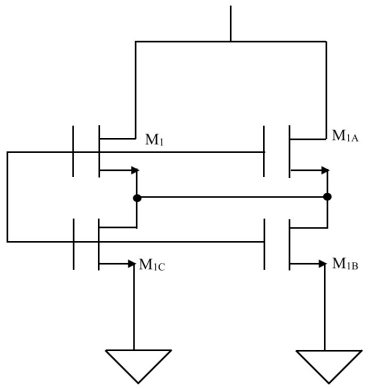

Figure 5.3: Series-Parallel Combination for M_1

2. A sweep of D was performed. Higher D increases all sensitivities but reduces area. Therefore

a trade-off between area and sensitivity must be done. So D is selected as 5.125 for a promising sensitivity and area trade-off.

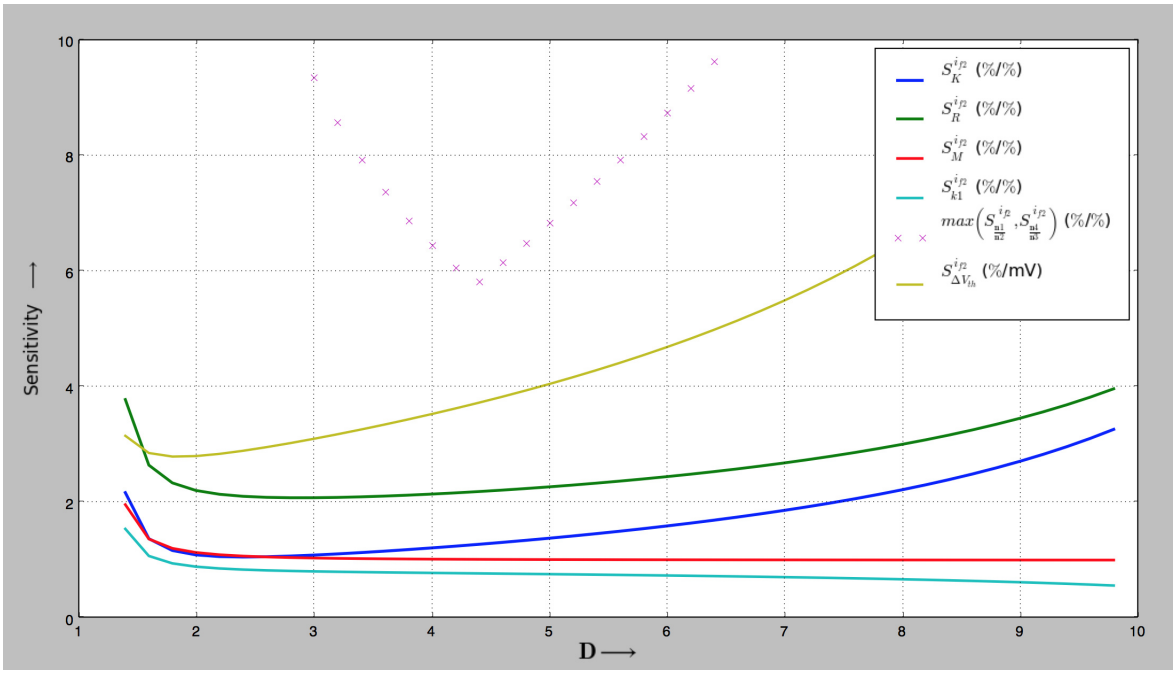

Figure 5.4: Sensitivity Graph of this Work

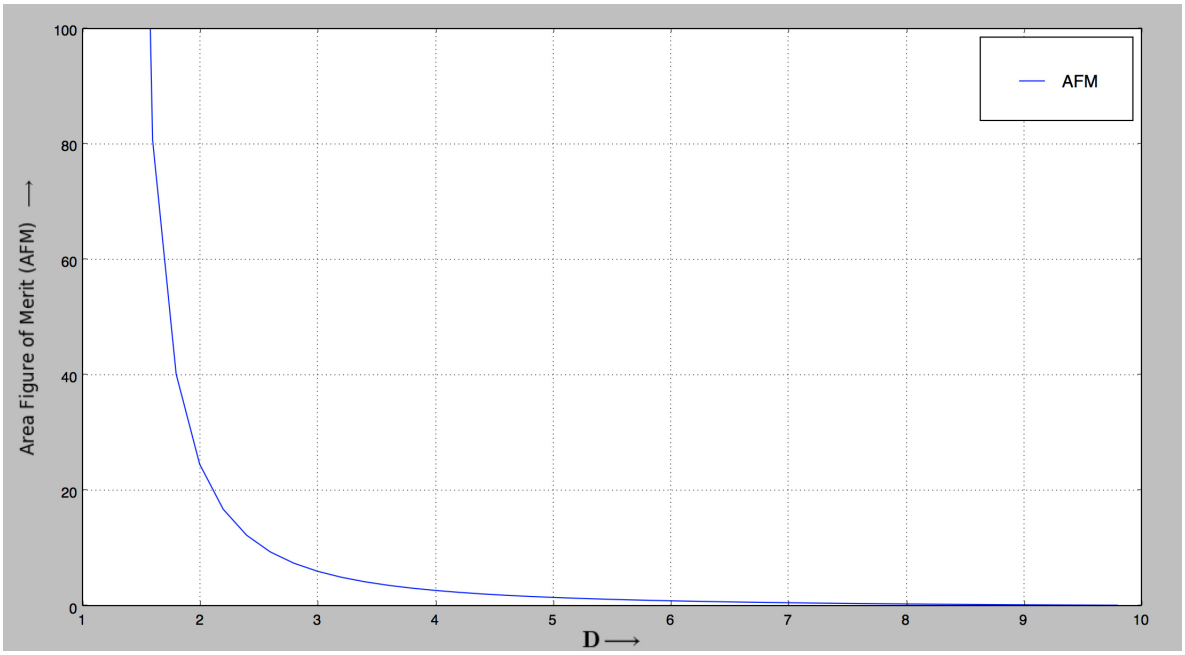

Figure 5.5: Effect of D on Area Figure of Merit (AFM)

Figure 5.4 and 5.5 follows A.2.

3. Layout plan in step 1 is proposed after few iterations.

4. Units in M_1 and M_2 are now calculated to 4 and 14 respectively while 6 and 21.85 unit transistors are used by M_3 and M_4 respectively. However M_4 is rounded up to 22 causing a little change in sensitivity and area but goes better with layout as shown in Figure 5.6.

M4 M4 M4 M4 M4 M4 M4 M4
M4 M3 M2 M2 M2 M2 M2 M2 M3 M4
M4 M3 M2 M1 M1 M1 M1 M2 M3 M4
M4 M3 M2 M2 M2 M2 M2 M2 M3 M4
M4 M4 M4 M4 M4 M4 M4 M4

Figure 5.6: Layout Plan including M_4

5. Inversion level coefficients and all sensitivity values are verified as shown in Tables 5.2, 5.3. According to Table 5.2 M_3 has a very low inversion level that is close to weak inversion. Table 5.1 show the value of parameters compared to [18].

Parameters	This Work	Luong *et al.* [18]
k_1	8	1
k_2	1	1
M	672	320
K	14	8

Table 5.1: Parameters used in this Work

Inversion Level Coefficients	This work	Luong *et al.* [18]
i_{f1}	0.034	0.086
i_{f2}	0.0024	0.01
i_{f3}	1.62	3.2
i_{f4}	8.30	10.24

Table 5.2: Inversion Level Coefficients of N-MOSFET's

Sensitivity Parameter	This Work	Luong *et al.* [18]
S_R^{if2}	2.29	2.38
$S_{k_1}^{if2}$	0.75	0.17
S_K^{if2}	1.40	1.64
S_M^{if2}	0.99	1.03
$S_{\frac{n1}{n2}}^{if2}$	4.59	6.75
$S_{\frac{n4}{n3}}^{if2}$	6.99	8.29
$S_{\Delta V_{th}}^{if2}$ (%/mV)	4.09	4.74
AFM	1.55	7.48

Table 5.3: Sensitivity and AFM Values of Design Example

5.3.2 Design of NMOS Section

Circuit Parameter Standard Deviation	This Work	Luong *et al.* [18]
σ_R %	0.3	0.14
$\sigma_{K_{NMOS}}$ %	0.37	0.43
$\sigma_{M_{NMOS}}$ %	0.30	0.15
$\sigma_{\Delta V_{th12}}$ mV	0.94	1.08
$\sigma_{\Delta V_{th34}}$ mV	0.77	0.34

Table 5.4: Standard Deviation of Circuit Parameters

1. The design of NMOS section starts by calculating unit transistor size for inversion levels, I_{SQ} and drain current I_D. For 0.18 nA of drain current in transistor M_1 and 86.76 nA of I_{SQ}, $\frac{1}{16.38}$ $(\frac{\mu m}{\mu m})$ is size of transistor M_1. This is taken as the dimension of unit transistor. Hence all the transistors are multiple of this unit transistor.

2. From all the available data number of unit transistors is calculated to be 46.

3. From Table 5.5 maximum standard deviation (σ_{MAX}) is 3.81 %.

5.3.3 PMOS Mirror Design

$\frac{\sigma_{i_{f2}}}{i_{f2}}$ %	This Work	Luong *et al.* [18]
$S_R^{i_{f2}} \times \sigma_R$	0.68	0.34
$S_K^{i_{f2}} \times \sigma_{K_{NMOS}}$	0.52	0.72
$S_M^{i_{f2}} \times \sigma_{M_{NMOS}}$	0.3	0.16
$S_{\Delta V_{th12}}^{i_{f2}} \times \sigma_{\Delta V_{th12}}$	3.81	5.12
$S_{\Delta V_{th34}}^{i_{f2}} \times \sigma_{\Delta V_{th34}}$	3.15	1.62

Table 5.5: Multiplication of Circuit Parameters with Sensitivity $\frac{\sigma(i_{f2})}{i_{f2}}$ %

1. From Table 5.5 the maximum standard deviation (σ_{MAX}) is 3.81 %, therefore mismatch in the current source shall not be greater than 3.81 %. Mathematically, $S_M^{i_{f2}} \times \sigma_{k1} \leqslant 3.81$ %.

2. Following step 2 of PMOS mirror design in Section 5.2.3. Solving for gate area of M_7 in Figure 5.1 using Equation (4.38) and σ_{MAX} from Table 5.5 results in 20 μm^2 of minimum gate area for M_7.

3. A similar analysis for M_5 and M_6 shown in Figure 5.1 results in minimum gate area of 66.08 μm^2 for less than or equal to 3.81 % of σ_{MAX} .

$$\mathsf{M_5\ M_6\ M_7\ M_6\ M_5}$$
$$\mathsf{M_5\ M_6\ M_7\ M_6\ M_5}$$

Figure 5.7: Layout Plan for PMOS Mirror

However gate area for PMOS mirror M_5, M_6 and M_7 in Figure 5.1 is selected as 80, 80 and 40 μm^2 respectively to achieve a mismatch of less than 3.81 %. This will ensure that greatest mismatch is not introduced by PMOS mirror. The unit transistor size for PMOS mirror is $\frac{1}{20}\left(\frac{\mu m}{\mu m}\right)$. For good matching, width is selected to be 1 μm and for increasing the output resistance of PMOS mirror, the length is selected to be 20 μm. Figure 5.7 show centroid layout plan for PMOS Mirror.

The results shown in Table 5.3 suggest a huge reduction in area and a similar sensitivity performance as in [18]. Both the works analysed weak and moderate inversion levels of NMOS transistors. $\left(\frac{\sigma_{i_{f2}}}{i_{f2}}\right)_{MAX}$ in the design example is less as compared to [18]. Table 5.6 provides worst $\frac{\sigma_{i_{f2}}}{i_{f2}}$, NMOS gate area, PMOS gate area and total current for all the designs. This table gives an idea that the design example has less worst standard deviation due to better PMOS mirror design compared to all the designs. Aspect ratio of NMOS and PMOS for [18] are $\frac{1}{24.9}$ and $\frac{2}{1}$ and that of this work are $\frac{1}{16.38}$ and $\frac{1}{20}$ respectively in $\frac{\mu m}{\mu m}$. Area figure of merit (AFM) is not the same as aspect ratio. Aspect ratio of a transistor is represented by width over length but AFM is a factor given in terms of number of unit transistors, minimum allowed width and length of unit transistor which is proportional to $K \times i_{f2}$. The Table 5.6 compares the design discussed in the literature review with this work suggesting a trade-off between area and total current. Therefore circuit with large current consumes less area and vice-versa. Since Serra-Graells *et al.* [16] do not have enough information, so meaningful comparison cannot be drawn in Table 5.6.

Design	Worst $\frac{\sigma_{i_{f2}}}{i_{f2}}$ %	NMOS Area (μm^2)	PMOS Area (μm^2)	Total Current (nA)
Galeano *et al.* [1]	15.27	8920	192	1.2
Luong *et al.* [18]	13.03	1494	24	1.8
This Work	3.81	753.48	200	1.8

Table 5.6: Design Characteristic Comparison

Transistor	Unit Transistor $\left(\frac{\mu m}{\mu m}\right)$	Number of units	Configuration
M_1	$\frac{1}{16.38}$	4	Series-Parallel
M_2	$\frac{1}{16.38}$	14	Parallel
M_3	$\frac{1}{16.38}$	6	Series
M_4	$\frac{1}{16.38}$	22	Series
M_5	$\frac{1}{20}$	4	Series
M_6	$\frac{1}{20}$	4	Series
M_7	$\frac{1}{20}$	2	Parallel

Table 5.7: Design Summary

Table 5.7 outline the details of size, number of units and configuration of all the transistors.

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5.4 Design Verification

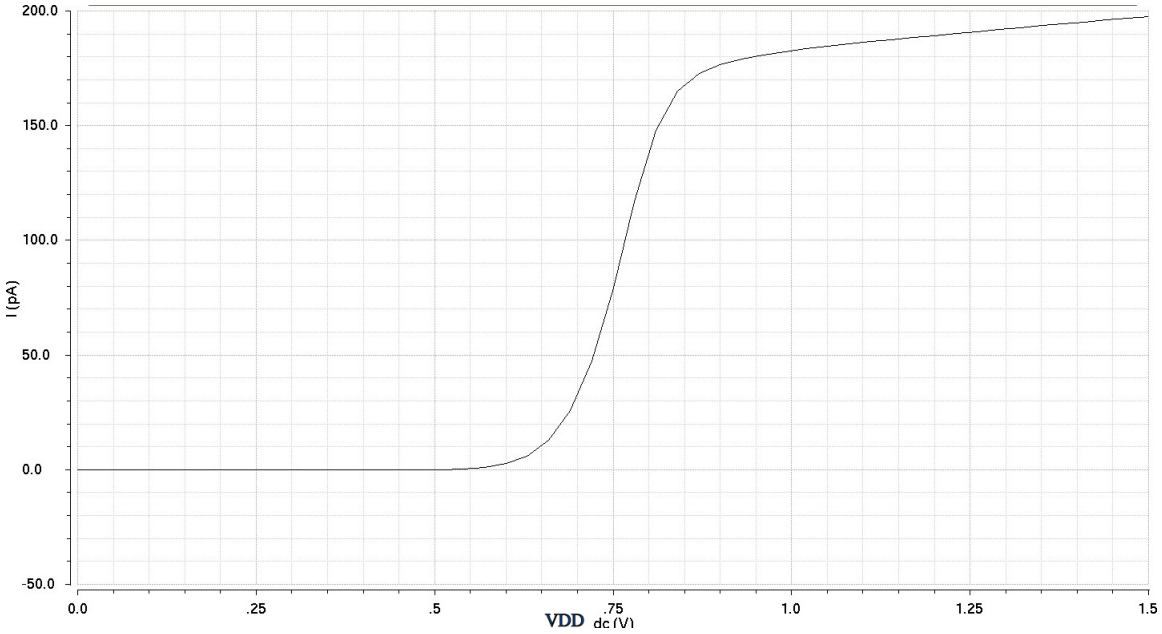

Figure 5.8: Output Current as a Function of Supply Voltage

Figure 5.8 shows the simulation for the circuit with the parameters discussed in the previous section. The current source is designed for the current flowing in the drain of M_1 to 0.18 nA. Channel length modulation causes deviation of current as shown in Figure 5.8 and can be improved by employing cascode current mirror and cascode transistors to equalize V_{DS} in M_1 and M_2 [18].

Sensitivity Parameter	Theoretical Value	Simulated Value
S_R^{if2}	2.29	2.42
$S_{k_1}^{if2}$	0.75	0.62
S_K^{if2}	1.40	1.31
S_M^{if2}	0.99	0.89
$S_{\Delta V_{th}}^{if2}$ (%/mV)	4.09	4.2

Table 5.8: Theoretical Vs Simulated Sensitivity Comparison

However Table 5.8 compares theoretical and simulated sensitivity that clearly verify the developed theory. To estimate sensitivities, simulations with ΔV_{th} set to 1 mV and other parameters incremented by 1 % were performed.

Chapter 6

Conclusion and Future Research Work

6.1 Conclusion

Effects of process parameter variations and device mismatch in the current reference circuit proposed in [4] was studied and a novel design methodology for reducing these effects and area of the current source is developed. This developed method is verified by simulations.
The following conclusions are drawn:

1. The sensitivities are mainly dependent on three variables namely K, M and D. Rise in K and M causes reduction of sensitivities with respect to different parameters but increases area. On the other hand, higher sensitivity with reduced area is achieved with a higher value of D.

2. PMOS current mirror gains k_1 and k_2 also impact sensitivity and area. Efficient PMOS current mirror design is important to reduce mismatch.

3. Slope factor sensitivity may cause inaccuracies in this type of current reference circuits. Slope factor mismatch can not be accounted due to lack of method and should be further studied.

4. The results presented in this thesis show that it is possible to achieve current sources with accurate inversion levels. The presented example has a standard deviation of 3.81%. By relaxing area and current consumption conditions even lower standard deviations are possible.

6.2 Future Research

1. The experimental verification of the designed circuit is an important future research consideration to validate the results obtained in theory and simulation. A test chip implementing the current source design should also include a circuit to experimentally extract the ACM parameters and thus allow the extraction of the actual inversion levels in current source.

2. Since Slope factor mismatch sensitivity can be quite large in this type of current source, a way to estimate the uncertainty in slope factor should be considered by the researchers interested in taking this work ahead.

3. Sensitivity of inversion level of M_2 respect to threshold voltage ($S^{i_{f2}}_{\Delta V_{th}}$ (%/mV)) is still very high. Therefore, reducing it further keeping low area and all possible sensitivities within acceptable limit is a good future research consideration.

4. Although standard deviation less than 3.81% can be achieved with large area and high current consumption. Developing a method that gives lower standard deviation for low current consumption with low area can be considered for future research.

5. This study can be expanded to study and analyse the effects of process parameter variations and device mismatch in the symmetric version of current reference circuit proposed in [1]. A method to reduce all possible sensitivities can also be developed for symmetric current reference circuit.

Appendix A

Python Code

A.1 Python Script to Plot Sensitivities respect to K, M, D

```
#!/usr/bin/python

from __future__ import print_function
import numpy as np
from scipy.optimize import bisect
import matplotlib.pyplot as plt
def fifr(i):
    """
    F(i_f(r)) from ACM model
    """
    sqi1 = np.sqrt(1. + i)
    return sqi1 - 2. + np.log(sqi1 - 1.)
def dfifr(i):
    """
    dF(i_f)/di_f from ACM model
    """
    sqi1 = np.sqrt(1. + i)
    return .5/(sqi1 - 1.)
def F(if2):
    """
    Zero function
    """
    return fifr(if2) + fifr(M * D * if2) \
        - fifr(M * if2) - fifr(K * if2)
def Fp(if2):
    """
    Derivative of F()
    """
    return dfifr(if2) + M * D * dfifr(M * D * if2) \
```

```
        - M * dfifr(M * if2) - K * dfifr(K * if2)
# (Not needed)
def dFdM(if2):
    return if2 * (D * dfifr(M * D * if2) - dfifr(M * if2))
def dFdD(if2):
    return M * if2 * dfifr(M * D * if2)
def dFdK(if2):
    return - if2 * dfifr(K * if2)
# k1, k2 not needed but assumed to be 1 for area estimation
k1 = 1.
k2 = 1.
# (K, M, D) -> (i, j, k)
K = 0.
M = 0.
D = 0.
Kv = np.arange(8., 30., 1.)
Mv = np.arange(40., 600., 20.)
Dv = np.arange(2., 12., 1.)
nk = len(Kv)
nm = len(Mv)
nd = len(Dv)
if2T = np.ones((nk,nm,nd)) * np.nan
sensT = np.ones_like(if2T) * np.nan
sensVthT = np.ones_like(if2T) * np.nan
afmT = np.ones_like(if2T) * np.nan
for i in range(nk):
    K = Kv[i]
    for j in range(nm):
        M = Mv[j]
        for k in range (nd):
            D = Dv[k]
            # Calculate zero of F(if2)
            try:
                if2 = bisect(f = F, a = 1e-5, b = 200.)
                # Sensitivities
                dfi = Fp(if2) * if2
                sensK = abs(K * dFdK(if2) / dfi)
                sensS34 = abs((D-1) * dFdD(if2) / dfi)
                # Area figure of merit
                n2 = K/k2
                n3 = k2/k1 * M/K
                n4 = k2/(k1+1) * (D-1)*M/K
                afmT[i,j,k] = (1 + n2 + n3 + n4) * K * if2
                # Save results
                if2T[i,j,k] = if2
                sensVthT[i,j,k] = 1./dfi
                sensT[i,j,k] = max(sensK, sensS34)
            except:
```

```
                pass
                #if2T[i,j,k] = 0.
                # sensT[i,j,k] = 100.
# Sensitivity respect to Delta_Vth (assumes n=1.3)
sensVthT *= 100./1.3/26.
print("Best sensitivity:", np.nanmin(sensT))
idx = np.unravel_index(np.nanargmin(sensT),(nk,nm,nd))
K = Kv[idx[0]]
M = Mv[idx[1]]
D = Dv[idx[2]]
print("if2 =", if2T[idx])
print("sens. Delta_Vth:", sensVthT[idx], "%/mV")
print("Area figure of merit: ", afmT[idx])
print("K =", K, "M =", M, "D =", D)
# Area
nNMOS = K/k2  + 1. + M/k1 + (D-1)*M/(k1+1)
nPMOS = k1 + k2 + 1
print("Number of NMOS = ", nNMOS)
print("Number of PMOS = ", nPMOS)
# Plot sensitivity respect to K
skmin = np.zeros_like(Kv)
skmax = np.zeros_like(Kv)
sVthmin = np.zeros_like(Kv)
afmSv = np.zeros_like(Kv)
afmVv = np.zeros_like(Kv)
for i in range(nk):
    skmin[i] = np.nanmin(sensT[i,:,:])
    skmax[i] = np.nanmax(sensT[i,:,:])
    sVthmin[i] = np.nanmin(sensVthT[i,:,:])
    i1 = np.unravel_index(np.nanargmin(sensT[i,:,:]), (nm,nd))
    afmSv[i] = afmT[i,i1[0],i1[1]]
    i1 = np.unravel_index(np.nanargmin(sensVthT[i,:,:]), (nm,nd))
    afmVv[i] = afmT[i,i1[0],i1[1]]
plt.cla()
plt.plot(Kv,skmin,label=r'$max$$\left(min_{D,M}(S_{R}^{i_{f2}}),min_{D,M}(S_{K}^{i_{f2}})\right)$ ($\%$/$\%$)'

,linewidth=2.5)
#plt.plot(Kv,skmax)
plt.plot(Kv,sVthmin,label=r'$min_{D,M}(S_{\Delta {V_{th}}}^{i_{f2}}$) ($\%$/mV)',linewidth=2) # Unit: %/V
plt.xlabel(r'$K$ $\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'$Sensitivity$ $\longrightarrow$', {'fontsize': 20})
plt.grid()
plt.legend(borderpad=1)
# AFM
plt.figure()
plt.xlabel(r'$K$$\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'Area Figure of Merit (AFM) $\longrightarrow$', {'fontsize': 20})
plt.plot(Kv,afmSv,label=r'AFM $\left(\mathrm{max} \left(S_{R}^{i_{f2}},S_{K}^{i_{f2}}\right)\right)$',linewidth=2.5)
```

```
plt.plot(Kv,afmVv,label=r'AFM $\left(S_{\Delta {V_{th}}}^{i_{f2}}\right)$',linewidth=2)
plt.grid()
plt.legend(borderpad=1.5)
# Plot sensitivity respect to M
smmin = np.zeros_like(Mv)
smmax = np.zeros_like(Mv)
sVthmin = np.zeros_like(Mv)
afmSv = np.zeros_like(Mv)
afmVv = np.zeros_like(Mv)
for j in range(nm):
    smmin[j] = np.nanmin(sensT[:,j,:])
    smmax[j] = np.nanmax(sensT[:,j,:])
    sVthmin[j] = np.nanmin(sensVthT[:,j,:])
    i1 = np.unravel_index(np.nanargmin(sensT[:,j,:]), (nk,nd))
    afmSv[j] = afmT[i1[0],j,i1[1]]
    i1 = np.unravel_index(np.nanargmin(sensVthT[:,j,:]), (nk,nd))
    afmVv[j] = afmT[i1[0],j,i1[1]]
plt.figure()
plt.xlabel(r'$M$ $\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'$Sensitivity $$\longrightarrow$', {'fontsize': 20})
plt.plot(Mv,smmin,label=r'$max$$\left(min_{D,K}(S_{R}^{i_{f2}}),min_{D,K}(S_{K}^{i_{f2}})\right)$ ($\%$/$\%$)'
,linewidth=2.5)
#plt.plot(Mv,smmax)
plt.plot(Mv,sVthmin,label=r'$min_{D,K}(S_{\Delta {V_{th}}}^{i_{f2}})$ ($\%$/mV)',linewidth=2) # Unit: %/V
plt.grid()
plt.legend(borderpad=1.5)
# AFM
plt.figure()
plt.xlabel(r'M $\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'Area Figure of Merit (AFM) $\longrightarrow$', {'fontsize': 20})
plt.plot(Mv,afmSv,label=r'AFM $\left(\mathrm{max} \left(S_{R}^{i_{f2}},S_{K}^{i_{f2}}\right)\right)$',linewidth=2.5)
plt.plot(Mv,afmVv,label=r'AFM $\left(S_{\Delta {V_{th}}}^{i_{f2}}\right)$',linewidth=2)
plt.grid()
plt.legend(borderpad=1.5)
# Plot sensitivity respect to D
sdmin = np.zeros_like(Dv)
sdmax = np.zeros_like(Dv)
sVthmin = np.zeros_like(Dv)
afmSv = np.zeros_like(Dv)
afmVv = np.zeros_like(Dv)
for k in range(nd):
    sdmin[k] = np.nanmin(sensT[:,:,k])
    sdmax[k] = np.nanmax(sensT[:,:,k])
    sVthmin[k] = np.nanmin(sensVthT[:,:,k])
    i1 = np.unravel_index(np.nanargmin(sensT[:,:,k]), (nk,nm))
    afmSv[k] = afmT[i1[0],i1[1],k]
    i1 = np.unravel_index(np.nanargmin(sensVthT[:,:,k]), (nk,nm))
    afmVv[k] = afmT[i1[0],i1[1],k]
```

```
plt.figure()
plt.xlabel(r'$D$$\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'$Sensitivity$ $\longrightarrow$', {'fontsize': 20})
plt.plot(Dv,sdmin,label=r'$max$$\left(min_{K,M}(S_{R}^{i_{f2}}),min_{K,M}(S_{K}^{i_{f2}})\right)$ ($\%$/$\%$)'
,linewidth=2.5)
#plt.plot(Dv,sdmax)
plt.plot(Dv,sVthmin,label=r'$min_{K,M}(S_{\Delta {V_{th}}}^{i_{f2}}$) ($\%$/mV)',linewidth=2) # Unit: %/V
plt.legend(borderpad=1.5)
plt.grid()
# AFM
plt.figure()
plt.xlabel(r'D$\longrightarrow$', {'fontsize': 20})
plt.ylabel(r'Area Figure of Merit (AFM) $\longrightarrow$', {'fontsize': 20})
plt.plot(Dv,afmSv,label=r'AFM $\left(\mathrm{max} \left(S_{R}^{i_{f2}},S_{K}^{i_{f2}}\right)\right)$',linewidth=2.5)
plt.plot(Dv,afmVv,label=r'AFM $\left(S_{\Delta {V_{th}}}^{i_{f2}}\right)$',linewidth=2)
plt.grid()
plt.legend(borderpad=1.5)
plt.show()
```

A.2 Python Script to Plot Sensitivities and AFM

```
from __future__ import print_function
import numpy as np
from scipy.optimize import bisect
import matplotlib.pyplot as plt
def fifr(i):
    """
    F(i_f(r)) from ACM model
    """
    sqi1 = np.sqrt(1. + i)
    return sqi1 - 2. + np.log(sqi1 - 1.)
def dfifr(i):
    """
    dF(i_f)/di_f from ACM model
    """
    sqi1 = np.sqrt(1. + i)
    return .5/(sqi1 - 1.)
def F(if2):
    """
    Zero function
    """
    return fifr(if2) + fifr(M * D * if2) \
        - fifr(M * if2) - fifr(K * if2)
def Fp(if2):
    """
    Derivative of F()
```

```
    """
    return dfifr(if2) + M * D * dfifr(M * D * if2) \
        - M * dfifr(M * if2) - K * dfifr(K * if2)
def dFdM(if2):
    return if2 * (D * dfifr(M * D * if2) - dfifr(M * if2))
def dFdD(if2):
    return M * if2 * dfifr(M * D * if2)
def dFdK(if2):
    return - if2 * dfifr(K * if2)
def k1dFdk1(if2):
    return M * dFdM(if2) - S34 * dFdD(if2) / k1
# Design parameters (based on layout plan)
S2oS1 = 14.
k2 = 1
S2oS3 = 84
k1 = 8.
# Main parameters for circuit
K = k2 * S2oS1
M = k1 * S2oS3
D = 0. # to be determined
Dv = np.arange(1.4, 10., .2)
nd = len(Dv)
if2v = np.ones((nd)) * np.nan
sensKv = np.ones_like(if2v) * np.nan
sensS34v = np.ones_like(if2v) * np.nan
sensMv = np.ones_like(if2v) * np.nan
sensk1v = np.ones_like(if2v) * np.nan
sensv = np.ones_like(if2v) * np.nan
sensVthv = np.ones_like(if2v) * np.nan
afmv = np.ones_like(if2v) * np.nan
for k in range (nd):
    D = Dv[k]
    S34 = (D-1)/(1+1./k1)
    print("D",Dv[k])
    # Calculate zero of F(if2)
    try:
        if2 = bisect(f = F, a = 1e-5, b = 200.)
        # Sensitivities
        dfi = Fp(if2) * if2
        sensKv[k] = abs(K * dFdK(if2) / dfi)
        sensS34v[k] = abs((D-1) * dFdD(if2) / dfi)
        sensMv[k] = abs(M * dFdM(if2) / dfi)
        sensk1v[k] = abs(k1dFdk1(if2) / dfi)
        # Save results
        if2v[k] = if2
        sensVthv[k] = 1./dfi
        sensv[k] = max(sensKv[k], sensS34v[k])
        print("if2",if2v[k])
```

```
        # AFM
        n2 = (2*K/k2)
        n3 = k2/(2*k1) * M/K
        n4 = k2/(2*(k1+1)) * (D-1)*M/K
        afmv[k] = (1 +n2 + n3 + n4) * K * if2
    except:
        pass
# Max Sensitivity respect to n1/n2 or n4/n3 (assumes sensVthv = 1/dfi)
# (Needs more revision to verify correctness)
sensn1n2v = sensVthv.copy()
for k in range(nd):
    f = max(abs(fifr(K*if2v[k])), abs(fifr(D*M*if2v[k])))
    sensn1n2v[k] *= f
sensn1n2v = abs(sensn1n2v)
# Sensitivity respect to Delta_Vth (assumes n=1.3)
sensVthv *= 100./1.3/26.
# Plot sensitivity respect to D
plt.figure()
plt.xlabel(r'$\mathbf{D} \longrightarrow$', {'fontsize': 20})
plt.ylabel(r'Sensitivity  $\longrightarrow$', {'fontsize': 15})
plt.grid()
plt.ylim(ymax=10.)
plt.plot(Dv,sensKv, label=r'$S_{K}^{i_{f2}}$ ($\%$/$\%$)',linewidth=2.5)
plt.plot(Dv,sensS34v, label=r'$S_{R}^{i_{f2}}$ ($\%$/$\%$)', linewidth=2.4)
plt.plot(Dv,sensMv, label=r'$S_{M}^{i_{f2}}$ ($\%$/$\%$)',linewidth=2.3)
plt.plot(Dv,sensk1v, label=r'$S_{k1}^{i_{f2}}$ ($\%$/$\%$)',linewidth=2.2)
plt.plot(Dv,sensn1n2v, 'x', label=r'$max\left(S_\mathbf{\frac{n1}{n2}}^{i_{f2}},

S_\mathbf{\frac{\mathbf{n4}}{n\mathbf{3}}}^{i_{f2}}\right)
(\%/\%)',linewidth=8)
plt.plot(Dv,sensVthv, label=r'$S_{\Delta {V_{th}}}^{i_{f2}}$ ($\%$/mV)',linewidth=2)
plt.legend(borderpad=1)
#AFM
plt.figure()
plt.ylim(ymax=min(100., max(afmv)))
plt.ylabel(r'Area Figure of Merit (AFM)  $\longrightarrow$', {'fontsize': 15})
plt.xlabel(r'$\mathbf{D} \longrightarrow$', {'fontsize': 20})
plt.plot(Dv,afmv,label='AFM')
plt.grid()
plt.legend(borderpad=2)
plt.show()
print("K =", K, "M =", M, "k1 = ", k1, "k2 = ", k2)
print("-------------------------------------------------------------")
print("Best S mismatch sensitivity:", np.nanmin(sensv))
idx = np.nanargmin(sensv)
print("AFM = ", afmv[idx])
D = Dv[idx]
print("D =", D)
```

```
if2 = if2v[idx]
print("if2 =", if2)
print("if1 = ", K*if2)
print("if3 = ", M*if2)
print("if4 = ", M*D*if2)
print("Delta_Vth sensitivity:", sensVthv[idx], "%/mV")
print("S3s4 sensitivity:",  sensS34v[idx])
print("K sensitivity:",  sensKv[idx])
print("k1 sensitivity:",  sensk1v[idx])
print("M sensitivity:",   sensMv[idx])
print("n1/n2 sensitivity:",   ( (1/dfi) *abs(fifr(K*if2v))[idx]))
print("n4/n3 sensitivity:",  ( (1/dfi)* abs(fifr(D*M*if2v))[idx]))
# Area
S3oS4 = (D-1)/(1+1./k1)
n2 = K/k2
n3 = k2/k1 * M/K
n4 = k2/(k1+1) * (D-1)*M/K
nNMOS = 1 + n2 + n3 + n4
nPMOS = k1 + k2 + 1
print("S3/S4 = ", S3oS4)
print("Units in M1: 1, M2: {} (p), M3: {} (s), M4: {} (s)".format(n2, n3, n4))
print("Number of NMOS = ", nNMOS)
print("Number of PMOS = ", nPMOS)
print("------------------------------------------------------------")
idx = np.nanargmin(sensVthv)
print("S mistmach sensitivity (best Vth mismatch):", sensv[idx])
print("AFM = ", afmv[idx])
D = Dv[idx]
print("D =", D)
if2 = if2v[idx]
print("if2 =", if2)
print("if1 = ", K*if2)
print("if3 = ", M*if2)
print("if4 = ", M*D*if2)
print("Delta_Vth sensitivity:", sensVthv[idx], "%/mV")
print("S3s4 sensitivity:",  sensS34v[idx])
print("K sensitivity:",  sensKv[idx])
print("k1 sensitivity:",  sensk1v[idx])
print("M sensitivity:",   sensMv[idx])
print("n1/n2 sensitivity:",   ( (1/dfi) *abs(fifr(K*if2v))[idx]))
print("n4/n3 sensitivity:",  ( (1/dfi)* abs(fifr(D*M*if2v))[idx]))
# Sensitivity respect to Delta_Vth (assumes n=1.3)
print("Delta_Vth sensitivity:", sensVthv[idx], "%/mV")
# Area
S3oS4 = (D-1)/(1+1./k1)
n2 = K/k2
n3 = k2/k1 * M/K
n4 = k2/(k1+1) * (D-1)*M/K
```

```
nNMOS = 1 + n2 + n3 + n4
nPMOS = k1 + k2 + 1
print("S3/S4 = ", S3oS4)
print("Units in M1: 1, M2: {} (p), M3: {} (s), M4: {} (s)".format(n2, n3, n4))
print("Number of NMOS = ", nNMOS)
print("Number of PMOS = ", nPMOS)
# Search maximum D for reasonable sens. n1n2
sn1n2max = 7.
f1 = True
idx = nd-1
for k in range(nd):
    if f1:
        if sensn1n2v[k] < sn1n2max:
            f1 = False
    else:
        if sensn1n2v[k] > sn1n2max:
            idx = k-1
            break
if f1:
    idx = np.nanargmin(sensn1n2v)
print("-----------------------------------------------------------------")
print("Maximum accepetable s. respect n1/n2, n4/n3:", sn1n2max)
print("S mistmach sensitivity (highest acceptable D):", sensv[idx])
print("AFM = ", afmv[idx])
D = Dv[idx]
print("D =", D)
if2 = if2v[idx]
print("if2 =", if2)
print("if1 = ", K*if2)
print("if3 = ", M*if2)
print("if4 = ", M*D*if2)
# Sensitivity respect to Delta_Vth (assumes n=1.3)
print("Delta_Vth sensitivity:", sensVthv[idx], "%/mV")
print("S3s4 sensitivity:",  sensS34v[idx])
print("K sensitivity:",  sensKv[idx])
print("k1 sensitivity:",  sensk1v[idx])
print("M sensitivity:",   sensMv[idx])
print("n1/n2 sensitivity:",   ( (1/dfi) *abs(fifr(K*if2v))[idx]))
print("n4/n3 sensitivity:",  ( (1/dfi)* abs(fifr(D*M*if2v))[idx]))
# Area
S3oS4 = (D-1)/(1+1./k1)
n2 = K/k2
n3 = k2/k1 * M/K
n4 = k2/(k1+1) * (D-1)*M/K
nNMOS = 1 + n2 + n3 + n4
nPMOS = k1 + k2 + 1
print("S3/S4 = ", S3oS4)
print("Units in M1: 1, M2: {} (p), M3: {} (s), M4: {} (s)".format(n2, n3, n4))
```

```
print("Number of NMOS = ", nNMOS)
print("Number of PMOS = ", nPMOS)
```

Bibliography

[1] E. Camacho-Galeano, C. Galup-Montoro, and M. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 2, pp. 61–65, Feb. 2005, ISSN: 1549-7747. DOI: 10.1109/TCSII.2004.842059.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, New York, 2001, ISBN: 978-0072380323.

[3] P. Luong, C. Christoffersen, C. Rossi-Aicardi, and C. Dualibe, "Sub-1 V, 4 nA CMOS voltage references with digitally-trimmable temperature coefficient," in *IEEE 2014 12th International New Circuits and Systems Conference (NEWCAS)*, Jun. 2014, pp. 345–348. DOI: 10.1109/NEWCAS.2014.6934053.

[4] H. Oguey and D. Aebischer, "CMOS current reference without resistance," *IEEE Journal of Solid-State Circuit*, vol. 32, no. 7, pp. 1132–1135, Jul. 1997, ISSN: 0018-9200. DOI: 10.1109/4.597305.

[5] A. Cunha, M. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998, ISSN: 0018-9200. DOI: 10.1109/4.720397.

[6] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. Wiley, New York, 2001, ISBN: 978-0-470-24599-6.

[7] R. J. Widlar, "New developments in IC voltage regulators," *IEEE Journal of Solid-State Circuits*, vol. 6, no. 1, pp. 2–7, Feb. 1971, ISSN: 0018-9200. DOI: 10.1109/JSSC.1971.1050151.

[8] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977, ISSN: 0018-9200. DOI: 10.1109/JSSC.1977.1050882.

[9] A. Hastings, *The Art of Analog Layout*. Pearson Prentice Hall, New Jersey, 2006, ISBN: 0-13-146410-8.

[10] B. D. Yang, Y. K. Shin, J. S. Lee, Y. K. Lee, and K. C. Ryu, "An accurate current reference using temperature and process compensation current mirror," in *IEEE Asian Solid-State Circuits Conference, 2009.*, Nov. 2009, pp. 241–244. DOI: 10.1109/ASSCC.2009.5357223.

[11] S. S. Chouhan and K. Halonen, "A modified CMOS nano-power resistorless current reference circuit," in *10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2014*, Jun. 2014, pp. 1–4. DOI: 10.1109/PRIME.2014.6872689.

[12] W. B. Yang, Z. Y. Huang, C. T. Cheng, and Y. L. Lo, "Temperature insensitive current reference for the 6.27 MHz oscillator," in *2011 International Symposium on Integrated Circuits*, Dec. 2011, pp. 559–562. DOI: 10.1109/ISICir.2011.6131924.

[13] A. Bendali and Y. Audet, "A 1-v CMOS current reference with temperature and process compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 7, pp. 1424–1429, Jul. 2007, ISSN: 1549-8328. DOI: 10.1109/TCSI.2007.900176.

[14] C. Rossi-Aicardi, "Techniques for ultra low power integrated temperature sensors," Universidad de la Republica: Uruguay, Feb 2013.

[15] E. M. Camacho-Galeano, J. Q. Moreira, M. D. Pereira, A. J. Cardoso, C. Galup-Montoro, and M. C. Schneider, "Temperature performance of sub-1V ultra-low power current sources," in *2008 IEEE International Symposium on Circuits and Systems*, May 2008, pp. 2230–2233. DOI: 10.1109/ISCAS.2008.4541896.

[16] F. Serra-Graells and J. L. Huertas, "Sub-1-V CMOS proportional-to-absolute temperature references," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 84–88, Jan. 2003, ISSN: 0018-9200. DOI: 10.1109/JSSC.2002.806258.

[17] C.Rossi, C.Galup-Montoro, and M. Schneider, "PTAT voltage generator based on an MOS voltage divider," *Technical Proceedings of the 2007 NSTI Nanotechnology Conference and Trade Show, Santa Clara, CA, USA*, pp. 625–628, May 2007, ISSN: 1-4200-6184-4.

[18] Peter-Luong, "Sub-1 V, 4 nA CMOS voltage references with digitally-trimmable temperature coefficient," MScE, Department of Electrical and Computer Engineering, Lakehead University, August 2014.

[19] C. Rossi-Aicardi, J. Oreggioni, F. Silveira, and C. Dualibe, "A MOSFET-only voltage source with arbitrary sign adjustable temperature coefficient," in *IEEE 2011 9th International New Circuits and Systems Conference (NEWCAS)*, Jun. 2011, pp. 366–369. DOI: 10.1109/NEWCAS.2011.5981246.

[20] C. Galup-Montoro and M. Schneider, *MOSFET modeling for circuit analysis and design*. World Scientific Pub. Co., Singapore, 2007, ISBN: 978-981-256-810-6.

[21] V. Krishnan, *Probability And Random Processes*. John Wiley and Sons, 2006, ISBN: 978-0-471-70354-9.