Robust Control of DC-DC Boost Converter

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To my lovely wife Zainab,
my wonderful parents and brothers,
my son Ali and
my in-laws
for their love and support

Abstract

In this thesis, a robust controller comprising of a PI with phase-lead compensator for a DC-DC boost converter designed using classical frequency response method is presented. The superior performance of this controller in comparison with H_∞ and passivity based integral controllers from the literature is shown. The robustness of the controller to boost converter parameter deviations, disturbance magnitudes and polarity which lead to worst case stability is investigated. This approach offers an alternative to the traditional unstructured uncertainty envelop approach used in the literature.

Investigation into the nonlinearity arising from parasitic parameters in a boost converter is also presented in this thesis. It is shown that this nonlinearity can cause instability in boost converter control. This nonlinearity makes robust controller design difficult due to the sensitivity to disturbances. Static and dynamic voltage collapses are then studied. New non-iterative formulae are derived using the bilinear averaged model to calculate the voltage collapse point due to the parasitic parameters. Using these simple formulae boost converter stable operating region and disturbance limits can be calculated in the design phase. The use of these formulae for the design of the boost converter control system is studied. Static characteristics formula and the proposed controller performance are verified experimentally.

Acknowledgment

I am highly indebted to Dr. Natarajan for his invaluable guidance, support and his patience during preparing this work. Also, I would like to express my sincere thanks to Dr. Natarajan for leading my first steps into the field of power electronics and for being my supervisor, teacher and mentor.

Contents

Chapter 1

Introduction

1-1 Literature Review

The objectives of the controller in PWM DC-DC converters are to guarantee the stability of the system while keeping the output voltage constant with zero steady state error along with robust dynamic behavior against load variations and line voltage perturbations. Also, the controller should promise robust stability and robust performance against system parameter changes and other operating point changes. The non-minimum phase nature of boost (and buck-boost) converter due to the RHP zero limits the loop bandwidth of the controlled systems. However, various techniques have been developed to control the boost converter.

In [1] the dynamics corresponding to RHP zero have been taken as uncertain and included into an I/O modeling error. A reduced order estimator is used to estimate this error signal which is used as a feedback signal. A PI controller along with inner current loop control has been used. Numerical simulation results have been shown for a boost converter nominally rated at 122W and operating at 200 KHz for a 5 volt change in reference voltage (27.5 V to 32.5 V) and for 20% load change followed by 20% line voltage change. The simulation results for each case shows a settling time of 200 ms and 18% undershoot in response to disturbances. The controller has been implemented using a PC through a dSPACE CARD and tested for 5V step change in reference voltage. No experimental results have been shown for the system performance in response to load and line voltage disturbances. The high overshoot, long settling time and the complexity of the developed technique are the main drawbacks of this method.

In [2] second order transfer function (from control input to output voltage) of the boost converter has been approximated by a first order transfer function so that the PID tuning methods used usually in process control can be applied. Different methods such as Ziegler-

Nichol's (Z-N), Equating coefficients, Internal model control, and Synthesis method [3] has been applied to the same boost converter used in [1]. Parasitic parameters have not been taken into account in the model. The designed PI and PID controllers have been tested by simulation using only 1% load and line voltage disturbances with no experimental work. Simulation results, for a boost converter nominally rated at 122W and operating at 200KHz, show that the PI controller designed using Synthesis method gives the best results compared to the other methods with overshoot of 11.7% and 150 ms settling time which is not a very good performance in response to only 1% disturbances. Also, the work done in [2] has not shown robust stability, gain and phase margin behavior in response to operating point changes and parameter deviations from the nominal values.

In the classical design methods such as Bode plot and Nyquist method, the controller reshapes the frequency response of the loop to acquire high loop gain for a frequency bandwidth as wide as possible without losing the stability margins. These margins are limited in the case of boost converter because of RHS zero as claimed in [4,5] because high bandwidth which provides a good disturbance rejection will result in phase margin reduction leading to a conflict between the high bandwidth (disturbance rejection) and the phase margin (robust stability) requirements . Hence, this provided the motivation to apply H_∞ robust control technique to the problem of boost control for the first time in [4]. Nevertheless, contrary to what has been stated in [4,5], it will be shown in Chapter 2 of this thesis that the frequency response technique can be used to design a simple controller consisting of a PI and a lead compensator which gives robust performance and robust stability better than that of the H_∞ controller designed in [4,5]. The main negative aspects of the controller in [4,5] is that it has a high pass filter behavior, the steady state error is minimized but is not zero, and more unfortunately it has poor robust stability. It is shown in [6], that for some reasonable change in the boost component values from the nominal values in [4,5] (-7.5% in L, -25% in C, -40% in r_C and -20% in R_{load}) the phase margin reduces to 2° which is unacceptable. Moreover, simulations have been done for a boost converter (load of 0.5 A at 24 V output voltage) with load disturbance of 10% and input voltage disturbance of only 8.33% (1 V) but no experimental results are shown in [4,5]. The experimental results of output impedance and of audiosusceptibility have been shown in [5]. In [6], μ Synthesis

procedure has been used to design a robust controller to handle the uncertainties in the system characteristics. Uncertainties in component values are modeled as structured uncertainties so that they can be incorporated right into the design. The design results in a 79^{th} order controller which is reduced then to 2^{nd} order controller that has a high pass filter characteristic which in turn leads to noise amplification. No simulation or experimental results are shown to judge the performance of this controller in [6].

In [7] and [8], an H_∞ controller has been designed for boost and buck-boost converters (load of 0.5 A at 24 V output voltage). Simulations and also experimental results (in [8]) are shown for boost converter for load disturbance of 20% (0.1 A) and line voltage disturbance of 25% (3 V). The authors have not discussed robust stability and robust performance against operating point changes and boost converter component changes from nominal values and have assumed that the selected weighting functions satisfy these requirements. It will be shown in Chapter 2 of this thesis that a simple controller consisting of a PI and a lead compensator can achieve the same or even better results than those in [4, 5, 6, 7, 8].

All the design procedures used in [4, 5, 6, 7, 8] modeled the load disturbance as an ideal current source. This is done so that the transfer function from load disturbance to output voltage can be derived and used later in norm minimization. This is a realistic approximation for small load disturbances. However, for larger load change the effect on the dynamics and stability margins when it is modeled as a result of resistance change is more pronounced. Moreover, load resistance has a direct effect on the nonlinear behavior of boost converter. This will be studied in Chapter 3. Due to this nonlinearity, the feedback loop will switch at some operating conditions from negative feedback to positive feedback leading to output voltage collapse as will be seen and investigated in detail in Chapter 3.

It is claimed in [9] that the RHP zero limits the loop bandwidth of the controlled system which in turn puts a hard limit on the achievable performance using classical Lead-Lag compensators. This reason is cited in [9] as the motivation to develop nonlinear and adaptive controllers to improve the achievable performance. Different nonlinear techniques to control the boost converter have been compared in [9]. Linear averaged controller (LAC), feedback

linearizing controller (FLC), passivity based controller (PBC), sliding mode controller (SMC), and sliding mode plus passivity based controller (SM+PBC) were examined with a boost converter with the following parameters: L=170mH, C=1000μF, R_{load}=100Ω, f_s= 50 KHz, V_i=10 V and V_o=20 V. All the investigated techniques show non-robust behavior with high steady state error against line voltage and load disturbances of (3 V) and (-50 Ω), respectively. A heuristic approach of adding an integral loop around the output voltage (for continuous control laws- LAC, FLC and PBC) was reported in [9] to remove the steady state error. For adaptive PBC and adaptive SM+PBC the system still shows a steady state error in response to load disturbance because the parameter estimate converges close but not exactly to the true values which induces a steady state error. Adding the integral term for the non-adaptive version of LAC, FLC and PBC shows more acceptable performance than that of the full adaptive schemes. This motivates the authors in [9] to conclude the necessity of adding the integral term to remove the steady state error, even in the adaptive system despite there being no theory to assess the stability of the closed loop for the proposed schemes. However, there are other major drawbacks in the proposed nonlinear techniques of [9] and these are summarized below:

1- The output response is constrained by the open loop time constant in PBC, SMC and SM+PBC.
2- Energy losses with SMC are very high as usual.
3- All the reported nonlinear techniques require current measurements through the inductor.
4- Steady state error in response to input voltage and load disturbances is present in all non-adaptive techniques.
5- Adaptive schemes have a relative high cost and there is a steady state error in adaptive PBC and SM+PBC.
6- There is a high frequency oscillation in the inductor current in adaptive SM, adaptive SM+PBC, LAC plus integral term and PBC plus integral term.

7- Finally, all of the non-adaptive controllers, adaptive controllers and non-adaptive plus integral term controllers, show a high overshoot and very slow response (100-250 ms) to load disturbances of 0.2 A which is not acceptable in many applications.

It will be shown that the proposed simple linear controller of this thesis can achieve a highly competitive performance superior to all of the nonlinear techniques of [9] with voltage measurements only.

Most of the reviewed literature considered only small disturbances in the design and in the test of the presented controllers. Nevertheless, for large disturbances, the boost converter nonlinearity is the main challenge in the analysis and design of the robust controllers. Large-signal stability literature for boost converter control system analysis and design will be reviewed in Chapter 3.

1-2 Thesis Outline

The thesis is organized in five chapters as follows. In Chapter 1 two models for boost converter are discussed. Small-signal averaged model and large-signal discrete-time model. The linear small-signal model has been derived in detail and the state-space describing the dynamic behavior of the boost converter operating in continuous conduction mode is presented in this chapter. The main relations to calculate the discrete-model, which describes the boost behavior in both continuous and discontinuous conduction modes, are provided in Chapter 1. A simple controller for boost converter, consisting of PI and lead compensator, is introduced in Chapter 2. An easy-to-use design procedure and tuning tips based on frequency response are presented .The new controller is compared to H_∞ controller designed in [8]. The proposed controller shows a superior performance to that of the H_∞ controller based on simulation results. Worst case stability frequency response approach to examine the robust stability of the boost converter control system is investigated and compared to the unstructured uncertainty approach used in literature. In Chapter 3, simulated responses of the boost converter show that small signal analysis and even some nonlinear analysis does not reveal the instability problems, which can lead to output voltage collapse, caused by the nonlinearity inherent in boost converter in the presence of parasitic parameters. This

nonlinearity is investigated in detail in Chapter 3 and new non-iterative formulae have been derived, for the first time, to calculate the collapse point and the boost converter operating regions in terms of the boost converter parameters. Solutions to this problem have been suggested, and verified by simulation in this chapter to guarantee large-signal stability. Also, the proposed controller is compared to the passivity based integral control designed for large disturbances in this chapter. In Chapter 4, the proposed controller, consisting of a PI and a lead compensator, for a boost converter has been designed and experimentally verified. Chapter 5 suggests the future work and provides the main conclusions of this thesis.

1-3 Boost Converter Models

Two models have been used in this thesis to describe the dynamic behavior of the boost converter; small signal linear-time invariant models which are based on the state averaging method in [10] and [11] for continuous conduction mode of operation for boost converter, and the large signal discrete-time model in [12] which can be used for continuous and discontinuous conduction mode.

1-3-1 Boost Converter Differential Equations

Pulse-width modulated (PWM) switched power converters are nonlinear systems which are switched sequentially between two or more linear systems for certain time interval in accordance with the duty ratio. Nonlinearity arises when the time interval of switching depends on states. For a boost converter operating in continuous conduction mode (CCM), the system is switched periodically between two linear systems. For this CCM mode, the ratio of the time intervals is decided independently by the duty ratio. On the other hand, for a boost converter operating in discontinuous conduction mode (DCM), the system is switched periodically between three linear systems for certain time intervals. One of the intervals is decided by the duty ratio while the other intervals are determined by the inductor current state variable.

Figure 1-1 shows the traditional boost converter. The non-ideal behavior of the inductor and the capacitor is modeled using r_L as the inductor resistance and r_C as the capacitor equivalent series resistance (ESR). Also, the non-ideal effect of the switch and the

diode is modeled using r_{DS} as a MOSFET resistance when the MOSFET is ON and r_D as the diode resistance when the diode is ON. The ideal current source at the output simulates the load current change. As mentioned in Section 1-1, modeling load changes as an ideal current source is realistic only for small load changes. However, modeling the load change in this way has the advantage of providing the transfer function from line voltage and load disturbances to the output voltage so that the infinity norm or the L_2 norm of the closed loop from the input disturbances to output voltage can be minimized by choosing an appropriate controller as in H_∞ and H_2 robust control techniques.

Figure 1-2 illustrates the three possible topological configurations for the boost converter. It is obvious that the three systems are linear systems. For CCM the system is periodically switch between (a) and (b) as in the Figure 1-2 while in DCM mode the system is switching between (a) , (b) and (c) with the switching instant from (b) to (c) determined by the inductor current at the start of (b). The state space model of these topological modes can be derived as follows:

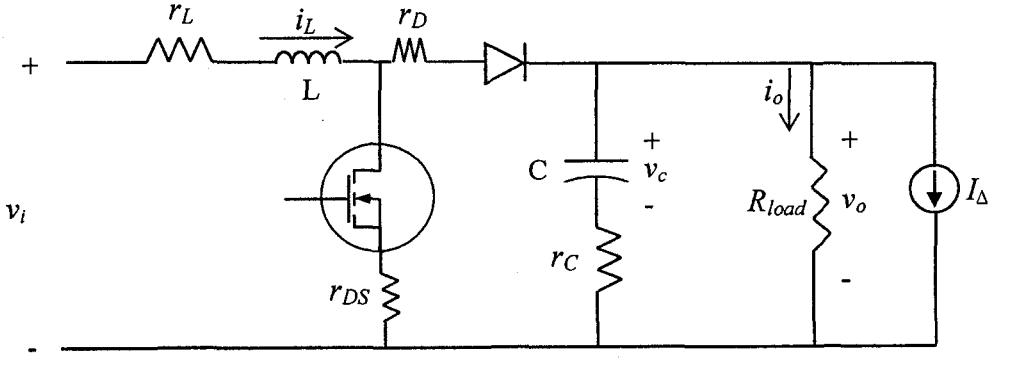
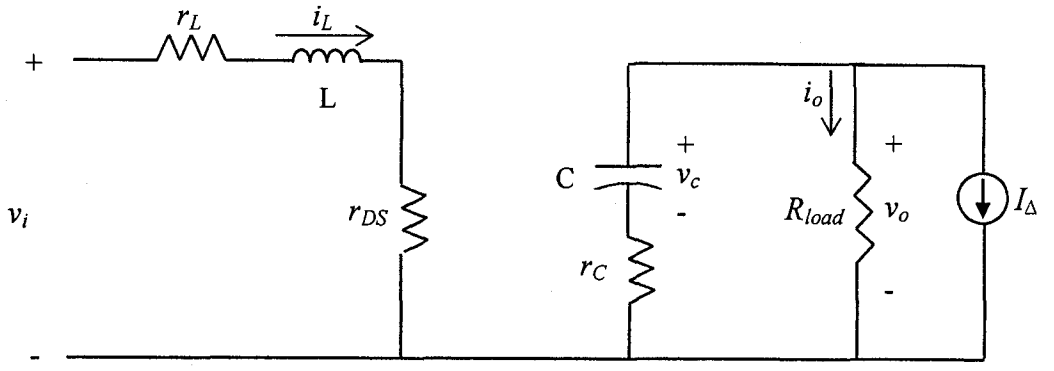
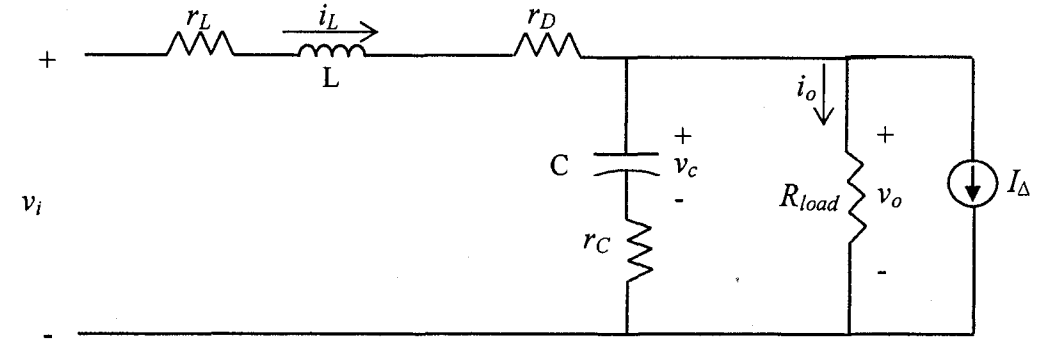


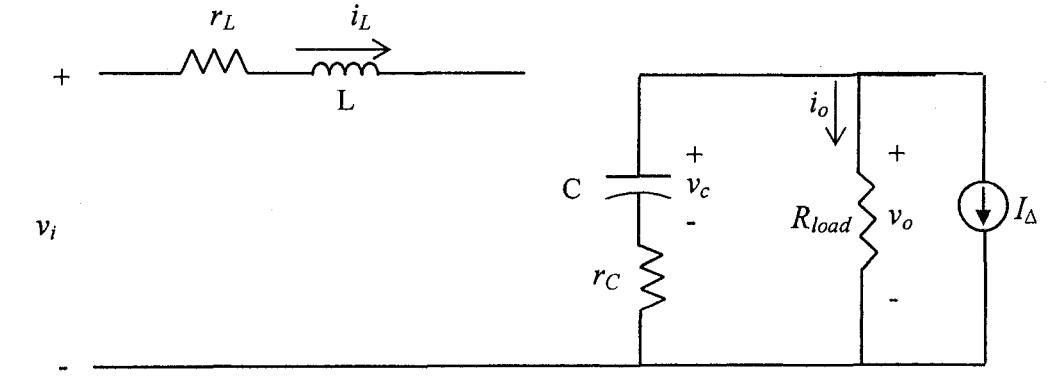
Figure 1-1: Boost converter circuit



(a) Switch ON; Diode OFF



(b) Switch OFF; Diode ON



(c) Switch OFF; Diode OFF

Figure 1-2: Three Topological modes of the boost converter operating in DCM

For (a):

The differential equations describing the linear system in Figure 1-2(a) are:

$$L\frac{di_L}{dt}+(r_L+r_{DS})\cdot i_L=v_i \tag{1-1}$$

$$C\frac{dv_C}{dt}+\frac{1}{R_{load}}(v_C+r_C C\frac{dv_C}{dt})+I_\Delta=0 \tag{1-2}$$

Let $x_1=i_L, x_2=v_C, x=\begin{bmatrix}x_1\\x_2\end{bmatrix}, u=\begin{bmatrix}v_i\\I_\Delta\end{bmatrix}$, then the state-space model describing the linear system in Figure 1-2(a) is:

$$\begin{aligned}\dot{x}&=A_1x+B_1u\\ v_o&=C_1x+D_1u\end{aligned} \tag{1-3}$$

Where A_1, B_1, C_1 and D_1 are given by:

$$A_1=\begin{bmatrix}-\dfrac{(r_L+r_{DS})}{L} & 0\\ 0 & -\dfrac{1}{C(r_C+R_{load})}\end{bmatrix},$$

$$B_1=\begin{bmatrix}\dfrac{1}{L} & 0\\ 0 & -\dfrac{R_{load}}{C(r_C+R_{load})}\end{bmatrix}, \tag{1-4}$$

$$C_1=\begin{bmatrix}0 & \dfrac{R_{load}}{r_C+R_{load}}\end{bmatrix},\quad D_1=\begin{bmatrix}0 & -\dfrac{R_{load}\cdot r_C}{r_C+R_{load}}\end{bmatrix}$$

For (b):

The differential equations describing the linear system in Figure 1-2(b) are:

$$-v_i + (r_L + r_D)\cdot i_L + L\frac{di_L}{dt} + v_o = 0 \tag{1-5}$$

$$v_C + C\frac{dv_C}{dt}\cdot r_C = v_0 \tag{1-6}$$

$$(i_L - C\frac{dv_C}{dt} - I_\Delta)\cdot R_{load} = v_o \tag{1-7}$$

The state-space for this linear system can be obtained by substituting (1-7) in (1-6) and rearranging terms:

$$\frac{dv_C}{dt} = \frac{R_{load}}{C(r_C + R_{load})} i_L - \frac{1}{C(r_C + R_{load})} v_C - \frac{R_{load}}{C(r_C + R_{load})} I_\Delta \tag{1-8}$$

and substituting (1-8) in (1-6) and rearranging terms:

$$v_o = \frac{R_{load}\cdot r_C}{r_C + R_{load}}\cdot i_L + \frac{R_{load}}{r_C + R_{load}} v_C - \frac{R_{load}\cdot r_C}{r_C + R_{load}} I_\Delta \tag{1-9}$$

Finally, substituting (1-9) in (1-5) and rearranging terms:

$$\frac{di_L}{dt} = -\left(\frac{r_L + r_D}{L} + \frac{R_{load}\cdot r_C}{L(r_C + R_{load})}\right)\cdot i_L + \left(\frac{-R_{load}}{L(r_C + R_{load})}\right)\cdot v_C + \frac{v_i}{L} + \frac{R_{load}\cdot r_C}{L(r_C + R_{load})} I_\Delta \tag{1-10}$$

Assuming $x_1 = i_L, x_2 = v_C, x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, u = \begin{bmatrix} v_i \\ I_\Delta \end{bmatrix}$, (1-8), (1-9) and (1-10) can be described by the state-space model:

$$\dot{x} = A_0 x + B_0 u$$
$$v_o = C_0 x + D_0 u \tag{1-11}$$

Where A_0, B_0, C_0 and D_0 are given by:

$$A_0 = \begin{bmatrix} -\dfrac{(r_L + r_D)}{L} - \dfrac{r_C \cdot R_{load}}{L(r_C + R_{load})} & -\dfrac{R_{load}}{L(r_C + R_{load})} \\ \dfrac{R_{load}}{C(r_C + R_{load})} & -\dfrac{1}{C \cdot (r_C + R_{load})} \end{bmatrix},$$

$$B_0 = \begin{bmatrix} \dfrac{1}{L} & \dfrac{R_{load} \cdot r_C}{L(r_C + R_{load})} \\ 0 & -\dfrac{R_{load}}{C \cdot (r_C + R_{load})} \end{bmatrix}, \tag{1-12}$$

$$C_0 = \begin{bmatrix} \dfrac{R_{load} \cdot r_C}{(r_C + R_{load})} & \dfrac{R_{load}}{r_C + R_{load}} \end{bmatrix}, \quad D_0 = \begin{bmatrix} 0 & -\dfrac{R_{load} \cdot r_C}{r_C + R_{load}} \end{bmatrix}$$

For (c):

In this case both the diode and the switch are OFF , and i_L=0. The differential equation describing the system is:

$$\frac{dv_C}{dt} = \frac{-1}{C(r_C + R_{load})} v_C - \frac{R_{load}}{(r_C + R_{load})} I_\Delta \tag{1-13}$$

1-3-2 Small-Signal State-Space Averaged Model

For duty ratio d, the dynamics of the system working in CCM is described by A_1, B_1, C_1 *and* D_1 in the interval dT_s , where T_s is the switching period. For the remaining time interval $(1\text{-}d)T_s$, the system dynamics are described by A_0, B_0, C_0 *and* D_0 . The state-space averaging is based on describing the system by one equivalent set:

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B}u \\ v_o &= \mathbf{C}x + \mathbf{D}u \end{aligned} \tag{1-14}$$

Where **A**, **B**, **C** and **D** are given by:

$$\begin{aligned} \mathbf{A} &= dA_1 + (1-d)A_0 \\ \mathbf{B} &= dB_1 + (1-d)B_0 \\ \mathbf{C} &= dC_1 + (1-d)C_0 \\ \mathbf{D} &= dD_1 + (1-d)D_0 \end{aligned} \tag{1-15}$$

Substituting equations (1-4) and (1-11) in (1-14) the averaged system is described by the following differential equations:

$$\begin{aligned} \dot{x}_1 = f_1(x_1,x_2,v_i,I_\Delta,d) &= \left(-(\frac{r_L + r_{DS}}{L}) \cdot d - (\frac{r_L + r_D}{L} + \frac{r_C \cdot R_{load}}{L(r_C + R_{load})}) \cdot \bar{d} \right) x_1 \\ &\quad - \frac{R_{load}}{L(r_C + R_{load})}(\bar{d}) \cdot x_2 + \frac{v_i}{L} + \frac{r_C \cdot R_{load}}{L(r_C + R_{load})} \cdot \bar{d} \cdot I_\Delta \\ \dot{x}_2 = f_2(x_1,x_2,v_i,I_\Delta,d) &= \frac{R_{load}}{C(r_C + R_{load})} \cdot \bar{d} \cdot x_1 - \frac{1}{C(r_C + R_{load})} \cdot x_2 - \frac{R_{load}}{C(r_C + R_{load})} \cdot I_\Delta \\ v_o = f_3(x_1,x_2,v_i,I_\Delta,d) &= \frac{r_C \cdot R_{load}}{(r_C + R_{load})} \cdot \bar{d} \cdot x_1 + \frac{R_{load}}{r_C + R_{load}} \cdot x_2 - \frac{r_C \cdot R_{load}}{(r_C + R_{load})} \cdot I_\Delta \end{aligned} \tag{1-16}$$

Where $\bar{d} = 1 - d$. Equations (1-16) can be described using state-space matrices given by:

$$\mathbf{A}=\begin{bmatrix} -\dfrac{(r_L + d\cdot r_{DS} + \bar{d}\cdot r_D)}{L} - \bar{d}\cdot\dfrac{r_C\cdot R_{load}}{L(r_C+R_{load})} & -\bar{d}\cdot\dfrac{R_{load}}{L(r_C+R_{load})} \\ \bar{d}\cdot\dfrac{R_{load}}{C(r_C+R_{load})} & -\dfrac{1}{C\cdot(r_C+R_{load})} \end{bmatrix},$$

$$\mathbf{B}=\begin{bmatrix} \dfrac{1}{L} & \dfrac{R_{load}\cdot r_C}{L(r_C+R_{load})} \\ 0 & -\dfrac{R_{load}}{C\cdot(r_C+R_{load})} \end{bmatrix}, \qquad (1\text{-}17)$$

$$\mathbf{C}=\begin{bmatrix} \dfrac{R_{load}\cdot r_C}{(r_C+R_{load})}\cdot\bar{d} & \dfrac{R_{load}}{r_C+R_{load}} \end{bmatrix},\quad \mathbf{D}=\begin{bmatrix} 0 & -\dfrac{R_{load}\cdot r_C}{r_C+R_{load}} \end{bmatrix}$$

Where $\bar{d}=1-d$. The steady state operating point (x_{1o}, x_{2o}, D) can be found from (1-16) as follows:

$$\begin{aligned} \dot{x}_1 &= f_1(x_{1o}, x_{2o}, V_i, I_{\Delta o}, D) = 0 \\ \dot{x}_2 &= f_2(x_{1o}, x_{2o}, V_i, I_{\Delta o}, D) = 0 \\ V_o &= f_3(x_{1o}, x_{2o}, V_i, I_{\Delta o}, D) \end{aligned} \qquad (1\text{-}18)$$

Where V_i : Nominal line Voltage

V_o: Desired output voltage

$I_{\Delta o}=0$,

Equation (1-18) can be solved to find the unknown operating point (x_{1o}, x_{2o}, D). It is clear that equations (1-16) that describe the boost dynamics are nonlinear with bilinear nature due to the product of control input (d duty cycle) and the states x_i. The duty ratio d appears as an input in equations (1-16). Applying the ac small-signal approximation: $x_1 = x_{1o} + \hat{x}_1$, $x_1 = x_{2o} + \hat{x}_2$, $v_i = V_i + \Delta v_i$, $I_\Delta = I_{\Delta o} + \Delta I_o$ and $d = D + \Delta d$, neglecting the ac quantities beyond first order and subtracting out the dc terms, the linear averaged small-signal system can be derived ([10,11]). However, the linear averaged small-signal system can also be derived by linearizing equations (1-16) around the operating point using Taylor Series. The latter approach is followed in this thesis. The linear averaged small-signal model is given by the following linear differential equations:

$$
\begin{aligned}
\dot{\hat{x}}_1 &= \frac{-1}{L}\left(r_L + r_{DS}\cdot D + (r_D + \frac{r_C \cdot R_{load}}{r_C + R_{load}})\cdot \overline{D}\right)\cdot \hat{x}_1 \\
&+ \frac{1}{L}\left(\frac{-R_{load}}{r_C + R_{load}}\cdot \overline{D}\right)\cdot \hat{x}_2 + \frac{1}{L}\cdot \Delta v_i \\
&+ \frac{1}{L}\left(\frac{r_C \cdot R_{load}}{r_C + R_{load}}\cdot \overline{D}\right)\cdot \Delta I_o \\
&+ \frac{1}{L}\left(-(r_{DS} - r_D - \frac{r_C \cdot R_{load}}{r_C + R_{load}})x_{1o} + \frac{R_{load}}{r_C + R_{load}} x_{2o}\right)\cdot \Delta d \\
\dot{\hat{x}}_2 &= \left(\frac{R_{load}}{C(r_C + R_{load})}\cdot \overline{D}\right)\cdot \hat{x}_1 + \left(\frac{-1}{C(r_C + R_{load})}\right)\cdot \hat{x}_2 \\
&+ \left(\frac{-R_{load}}{C(r_C + R_{load})}\right)\cdot \Delta I_o + \left(\frac{-R_{load}}{C(r_C + R_{load})} x_{1o}\right)\cdot \Delta d \\
\Delta v_o &= \left(\frac{r_C \cdot R_{load}}{r_C + R_{load}}\cdot \overline{D}\right)\cdot \hat{x}_1 + \left(\frac{R_{load}}{r_C + R_{load}}\right)\cdot \hat{x}_2 + \left(\frac{-r_C \cdot R_{load}}{C(r_C + R_{load})}\right)\cdot \Delta I_o \\
&+ \left(\frac{-r_C \cdot R_{load}}{C(r_C + R_{load})} x_{1o}\right)\cdot \Delta d
\end{aligned}
\tag{1-19}
$$

Where $\overline{D} = 1 - D$. By considering the control input $u = \Delta d$ and the disturbance input $w = \begin{bmatrix} \Delta v_i \\ \Delta I_o \end{bmatrix}$, the state space description of the system is given by:

$$
\begin{aligned}
\dot{\hat{x}} &= \mathbf{A}\hat{x} + \mathbf{B}_1 w + \mathbf{B}_2 u \\
\Delta v_o &= \mathbf{C}\hat{x} + \mathbf{D}_1 w + \mathbf{D}_2 u
\end{aligned}
\tag{1-20}
$$

Where:

$$\mathbf{A}=\begin{bmatrix} \frac{-1}{L}\left(r_L + r_{DS}\cdot D + (r_D + \frac{r_C \cdot R_{load}}{r_C + R_{load}})\cdot \overline{D} \right) & \frac{-R_{load}}{L(r_C + R_{load})}\cdot \overline{D} \\ \frac{R_{load}}{C(r_C + R_{load})}\cdot \overline{D} & \frac{-1}{C(r_C + R_{load})} \end{bmatrix}$$

$$\mathbf{B}_1=\begin{bmatrix} \frac{1}{L} & \frac{r_C \cdot R_{load}}{L(r_C + R_{load})}\cdot \overline{D} \\ 0 & \frac{-R_{load}}{C(r_C + R_{load})} \end{bmatrix},\quad \mathbf{B}_2=\begin{bmatrix} \frac{1}{L}\left(-(r_{DS} - r_D - \frac{r_C \cdot R_{load}}{r_C + R_{load}})x_{1o} + \frac{R_{load}}{r_C + R_{load}} x_{2o} \right) \\ \frac{-R_{load}}{C(r_C + R_{load})} x_{1o} \end{bmatrix} \qquad (1\text{-}21)$$

$$\mathbf{C}=\begin{bmatrix} \frac{r_C \cdot R_{load}}{r_C + R_{load}}\cdot \overline{D} & \frac{R_{load}}{r_C + R_{load}} \end{bmatrix}$$

$$\mathbf{D}_1=\begin{bmatrix} 0 & \frac{-r_C \cdot R_{load}}{C(r_C + R_{load})} \end{bmatrix},\quad \mathbf{D}_2=\frac{-r_C \cdot R_{load}}{C(r_C + R_{load})} x_{1o}$$

The state-space described by (1-20) and (1-21) is the linear averaged small-signal system that describes the dynamics of the boost converter in the CCM. For boost converter working in DCM either the small signal model derived in [13] or the large-signal discrete-time model in [12] can be used. However, the CCM is the common case and is the case discussed in this thesis. The large-signal discrete-time model will be discussed in the next subsection.

1-3-3 Large-Signal Discrete-Time Model

A large-signal discrete-time model of the boost converter is presented in this section following [12]. The same boost converter circuit and topological modes shown in Figures 1-1 and 1-2, respectively, are used to derive the discrete model assuming $I_\Delta = 0$. Hence, the system described by (1-3), (1-11) and (1-13) can be used considering $I_\Delta = 0$. Systems (1-3) and (1-11) can be combined in one matrix form given by:

$$\dot{x} = \mathbf{A}(S)x + \mathbf{B}(S);\quad v_o = \mathbf{C}(S)x \qquad (1\text{-}22)$$

Where S is an integer variable which is 1 (0) if the switch is ON (OFF); while $\overline{S} = 1 - S$. The matrices **A***(S)*, **B***(S)* and **C***(S)* are given by:

$$\mathbf{A}(S)=\begin{bmatrix} -\dfrac{(r_L+S\cdot r_{DS}+\overline{S}\cdot r_D)}{L} - \overline{S}\cdot\dfrac{r_C\cdot R_{load}}{L(r_C+R_{load})} & -\overline{S}\cdot\dfrac{R_{load}}{L(r_C+R_{load})} \\ \overline{S}\cdot\dfrac{R_{load}}{C(r_C+R_{load})} & -\dfrac{1}{C\cdot(r_C+R_{load})} \end{bmatrix};$$

$$\mathbf{B}(S)=\begin{bmatrix} \dfrac{v_i}{L} \\ 0 \end{bmatrix}; \tag{1-23}$$

$$\mathbf{C}(S)=\begin{bmatrix} \dfrac{R_{load}\cdot r_C}{(r_C+R_{load})}\cdot\overline{S} & \dfrac{R_{load}}{r_C+R_{load}} \end{bmatrix},$$

For DCM when i_L=0, (1-22) will be reduced to:

$$\frac{dv_C}{dt}=\frac{-1}{C(r_C+R_{load})}v_C \tag{1-24}$$

Two assumptions have been made to develop the discrete-time model. First assumption is that the duty cycle $d\,(0\le d\le 1)$ can be affected only once during the switching period T_s. The other assumption is the switching frequency is higher than the resonant frequency of the main inductor and capacitor in the boost circuit which is a reasonable assumption in practice. Within the intervals of switching periods the evolution of the state vector $x=\begin{bmatrix} i_L & v_C \end{bmatrix}'$ is described by [12] as:

$$x_{(k+d_k)T_s}=F_1x_{kT_s}+G_1 \qquad \text{Switch ON: } d_kT_s \tag{1-25}$$

$$x_{(k+1)T_s}=F_3F_2x_{(k+d_k)T_s}+F_3G_2 \qquad \text{Switch OFF: } (1-d_k)T_s \tag{1-26}$$

Where F_1, F_2, F_3 (state transition matrices), and G_1, G_2 are given by:

$$F_1=e^{A(1)d_kT_s}, \qquad G_1=(F_1-I)A(1)^{-1}B(1) \tag{1-27}$$

$$F_2=e^{A(0)(1-d_k)T_s} \qquad if \quad \phi\ge(1-d_k)T_s \tag{1-28}$$

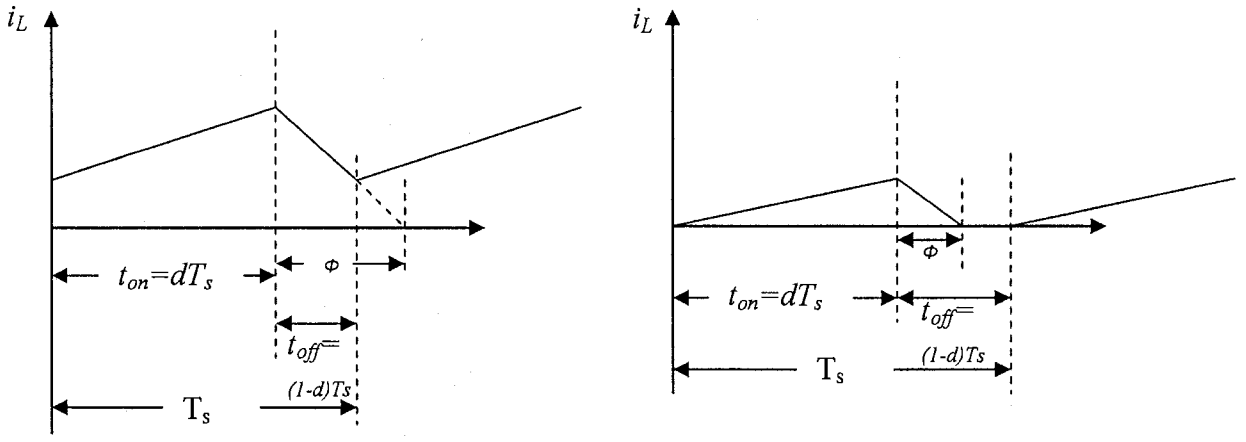
$$F_2=e^{A(0)\phi_k} \qquad if \quad \phi<(1-d_k)T_s \tag{1-29}$$

$$G_2=(F_2-I)A(0)^{-1}B(0) \tag{1-30}$$

$$F_3 = I \qquad if \quad \phi_k \geq (1-d_k)T_s \tag{1-31}$$

$$F_3 = \begin{bmatrix} 1 & 0 \\ 0 & e^{a_{22}((1-d_k)T_s-\phi_k)} \end{bmatrix} \quad if \quad \phi_k < (1-d_k)T_s \tag{1-32}$$

where k is the switching period index. a_{22} in (1-32) is the element in the second row and second column of A(S) matrix given by (1-23) and also in (1-24). ϕ_k is the time taken by inductor current to reach zero after the switch is opened at $(k+d_k)T_s$. Hence, if $\phi_k < (1-d_k)T$, the converter is in DCM (Figure 1-3(b)), otherwise it is in CCM (Figure 1-3(a)).



(a) CCM (b) DCM

Figure 1-3: Inductor Current and i_L and φ in continuous (a) and discontinuous (b) conduction mode

ϕ_k can be calculated by solving the following equation [12]:

$$\alpha_1 e^{\lambda_1 \phi_k} + \alpha_2 e^{\lambda_2 \phi_k} = \alpha_3 \tag{1-33}$$

where

$$\alpha_1 = t_{11}\left(\frac{t_{22}}{\lambda_1} B_1(0) + t_{22} i_{L_{(k+d_k)T_s}} - t_{12} v_{C_{(k+d_k)T_s}}\right) \tag{1-34}$$

$$\alpha_2 = -t_{12}\left(\frac{t_{21}}{\lambda_2} B_1(0) + t_{21} i_{L_{(k+d_k)T_s}} - t_{11} v_{C_{(k+d_k)T_s}}\right) \tag{1-35}$$

$$\alpha_3 = B_1(0)\left(\frac{t_{11}t_{22}}{\lambda_1} - \frac{t_{12}t_{21}}{\lambda_2}\right) \tag{1-36}$$

$B_1(0)$ is the first element of the vector $B(0)$ given in (1-23). t_{ij} are the elements of the eigenvector matrix T of A(0) and $i_{L_{(k+d_k)T_s}}, v_{C_{(k+d_k)T_s}}$ are the inductor current and capacitor voltage when the switch is opened and given by (1-25). Since equation (1-33) involves exponential function and depends on previous state variables at the time when the switch is opened, it can only be solved numerically using, for example, Newton-Raphson method [12].

Chapter 2

Boost Converter Control

In this chapter a robust controller for a boost converter operating in CCM will be designed using the classical frequency response design method and then compared with the H_∞ controller designed for the same boost converter. Section 2-1 provides the motivation to use the classical frequency response design method over the H_∞ design technique. In Section 2-2 the H_∞ controller designed in [8] will be reviewed. Frequency domain design guidelines, and tuning tips based on frequency response are introduced in Section 2-3. Using these guidelines a controller for the same boost converter parameters used in [8] will be designed in this section and will be compared to the H_∞ controller based on simulated performance. In Section 2-4, robustness against boost converter component tolerances and system disturbances, will be examined for both the H_∞ and the proposed designed controllers. Also, in this section, worst case frequency response approach to determine robust stability of the boost converter control system will be investigated and compared to the unstructured uncertainty approach used in robust control theory.

2-1 H_∞ Vs. Classical Frequency Response Control Design for Boost Converter

The classical frequency response design methods are based on reshaping the frequency response of the closed loop system to attain high loop gain for frequency bandwidth as wide as possible without losing stability margins ([4, 5]). However, it is claimed in [4] and [5] that due to the boost converter's non-minimum phase nature caused by the RHP zero, classical methods are limited because it leads to phase margin reduction. In other words, there is a conflict between the high bandwidth (disturbance rejection) and the phase margin (robust stability) requirements. However, it will be

shown in this chapter that a simple PI along with lead compensator designed by classical frequency response methods can achieve better results than those of the H_∞ controllers designed in [4, 5, 6, 7, 8]. The reasons behind the continued success of the frequency response methods for dealing with single-loop controller since the 1940's are [14]:

1- "There is a clear connection between the frequency response plots and the experimentally collected data.
2- Engineers find these methods relatively easy to learn.
3- Graphical nature provides an important visual aid.
4- These methods supply the designer with a rich variety of manipulative and diagnostic aids that enable the design to be refined in a systematic way.
5- Simple rule of thumb for standard controller configurations and systems can be developed."

On the other hand, robust control theory (H_∞, H_2, μ synthesis) is unlikely to find its way easily into engineering practice because of its complexity [14] unless it can be shown that performance from robust control theory far exceeds those provided by simpler techniques. To successfully use robust control theory, engineers must be familiar with this complex theory and how to choose the weighting functions to design the controller. Subsequently, the design must be tested to guarantee the system robustness which may lead to design iteration. Alternatively, the designer may choose initially to reduce the loop bandwidth to gain robustness [6, 15] then iterate. Moreover, the controller in this case is a result of an optimization problem which results in a controller transfer function where it is so difficult to interpret the function of each part of the controller for future tuning or diagnostic purposes. In the case of boost converter controller using a PI and lead compensator, the designer knows exactly the function of each part and can retune it against any change in the system. Moreover, as mentioned in the literature review, robust control techniques model the load disturbance as an ideal current source so that the transfer function from load disturbance to output voltage can be derived to be used later in norm minimization. This is a realistic approximation for small disturbances because changing the load resistance during the real operation by small value will not affect the

dynamics and stability margins to a large extent; however, for larger load change the effect on the dynamics and stability margins when it is modeled as a resistance change is more pronounced.

2-2 H_∞ Controller Design

Figure 2-1 shows the schematic of the boost converter used in [8] with parameters and nominal operating values. Figure 2-2 shows the block diagram of the boost converter along with the weighting functions used to design the H_∞ controller in [8]. P in Figure 2-2 is the boost converter model. Variations of input voltage, output voltage, load current and duty ratio are represented by Δv_i, Δv_o, ΔI_o, and Δd, respectively. The linear small-signal state-space model describing P is given by:

$$\begin{aligned} \dot{x} &= Ax + B_1 w + B_2 u \\ z &= C_1 x + D_{11} w + D_{12} u \\ e &= C_2 x + D_{21} w + D_{22} u \\ u &= Ke \end{aligned} \tag{2-1}$$

where $x = [i_L \quad v_C]^T, z = [\Delta v_o \quad \Delta d]^T, w = [\Delta v_i \quad \Delta I_o]^T, e = [\Delta v_o \quad \Delta v_i]^T, u = \Delta d$ and the system matrices calculated using (1-20) and (1-21) are given by:

$$\begin{aligned} A &= \begin{bmatrix} -1823.1 & -2186.7 \\ 2186.7 & -103.2 \end{bmatrix}, \quad B_1 = \begin{bmatrix} 4545.5 & 87.5 \\ 0 & -4541.3 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 108680 \\ -5140 \end{bmatrix} \\ C_1 &= \begin{bmatrix} 0.0192 & 0.9991 \\ 0 & 0 \end{bmatrix}, \quad D_{11} = \begin{bmatrix} 0 & -0.04 \\ 0 & 0 \end{bmatrix}, \quad D_{12} = \begin{bmatrix} -0.0453 \\ 1 \end{bmatrix}, \\ C_2 &= \begin{bmatrix} 0.0192 & 0.9991 \\ 0 & 0 \end{bmatrix}, \quad D_{21} = \begin{bmatrix} 0 & -0.04 \\ 1 & 0 \end{bmatrix}, D_{22} = \begin{bmatrix} -0.0453 \\ 0 \end{bmatrix} \end{aligned} \tag{2-2}$$

The steady-state duty ratio D is 0.5185 for this system. K_∞ is the H_∞ controller. W_{vi}, W_{Io}, W_e, and W_d are the weighting functions used to weight input and output signals to guarantee the required closed loop transfer function in the frequency domain.

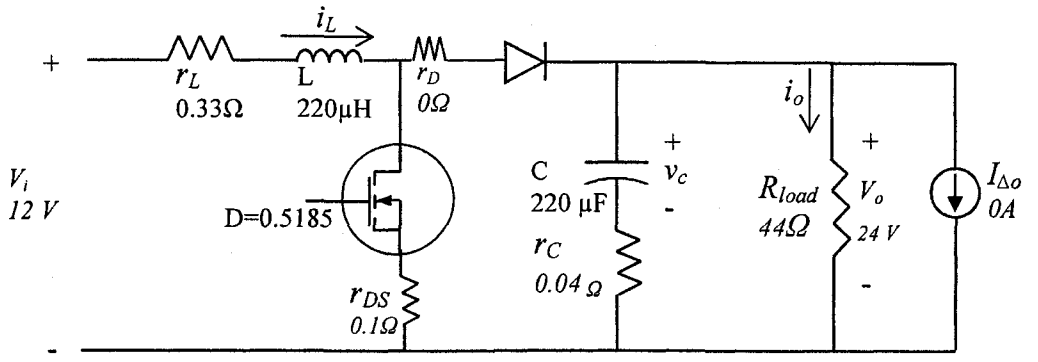


Figure 2-1: Boost converter circuit operating at 100 KHz

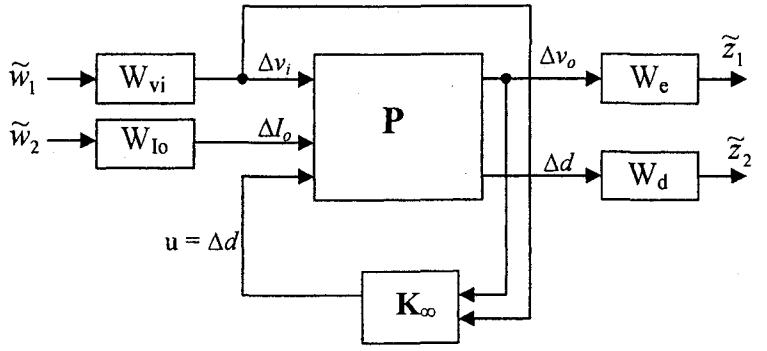


Figure 2-2: Block diagram used to design H_∞ controller

The transfer functions W_{vi}, W_{Io}, W_e, and W_d used in [8] are given by:

$W_{vi} = 3$ (For input voltage disturbance of 3 V)

$W_{Io} = 0.1$ (For output current disturbance of 0.1 A)

$$W_e = \frac{10^4}{s + 10^{-5}}$$ (Approximation of pure integrator)

$$W_d = 2.75 \times 10^4 \frac{(s + \pi 10^4)}{(s + \pi 10^8)}$$ (To impose an upper limit to $|\Delta d|$)

The transfer function from control to output can be calculated from (2-1) and (2-2) and it is given by at $D = 0.5185$:

$$H_{\Delta vo\Delta d}(s)=\frac{-0.0453(s+1.136\times10^{5})(s-4.437\times10^{4})}{(s+(0.9632+j2.0105)\times10^{3})(s+(0.9632-j2.0105)\times10^{3})} \quad (2\text{-}3)$$

The frequency response of $H_{\Delta vo\Delta d}$ is shown in Figure 2-3. The closed-loop transfer function matrix from $\tilde{w}$ to $\tilde{z}$ is defined by $T_{\tilde{z}\tilde{w}}$. The design objective is to find the controller K_∞ that minimize the infinity norm of $T_{\tilde{z}\tilde{w}}$ such that

$$\left\|T_{\tilde{z}\tilde{w}}\right\|_\infty < \gamma \quad (2\text{-}4)$$

where γ corresponds to an optimal ($\gamma = \gamma_{\min}$) or suboptimal case ($\gamma_{\min} < \gamma \le 1$) [8]. The problem of finding K_∞ has been solved in [8] using the hinfopt function of MATLAB Robust Control Toolbox which provides the asymptotically stable controller that guarantees $\left\|T_{\tilde{z}\tilde{w}}\right\|_\infty < \gamma$. The H_∞ controller obtained in [8] is as follows:

$$K_\infty(s)=\left[\frac{-1.87568\times10^{5}(s+(2.746+j0.476)\times10^{3})(s+(2.746-j0.476)\times10^{3})}{s(s+5.167\times10^{4})(s+1.13636\times10^{5})} \quad -0.039\right] \quad (2\text{-}5)$$

Frequency response of the loop gain using H_∞ controller is shown in Figure 2-4. The loop gain reveals a phase margin of 47.6° and gain margin of 15 dB. The closed loop bandwidth in this case is 8.44×10^{3} rad/sec.

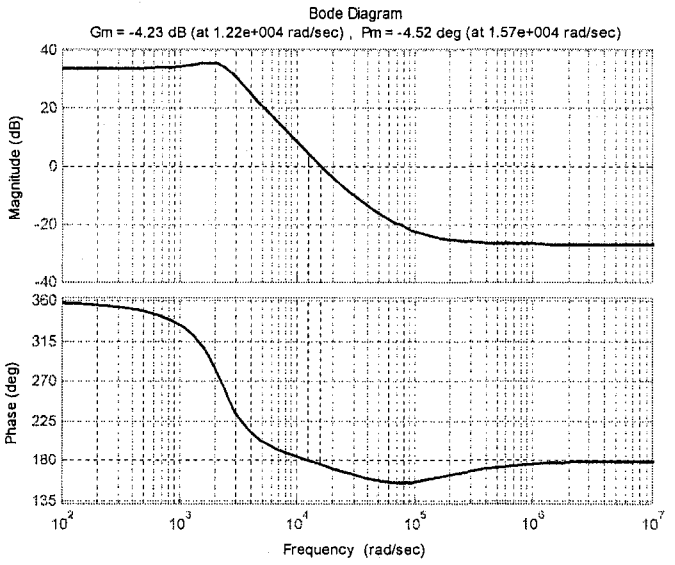


Figure 2-3: Frequency response of control-to- output transfer function

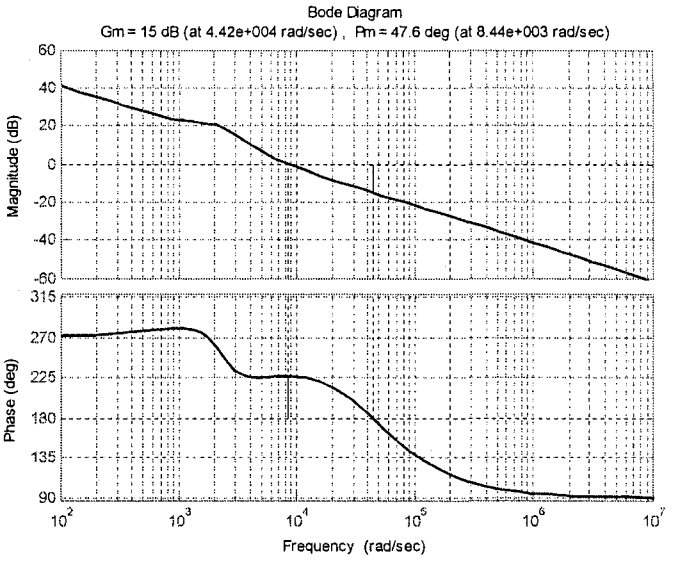


Figure 2-4: Loop gain frequency response using H_∞ controller

2-3 Controller Design Using Classical Frequency Response Method (Bode Plot):

In this section a classical controller will be designed for the same boost converter in [8] which is discussed in the last section. The transfer function from control input to

output ($G(s) = H_{\Delta vo \Delta d}$) of the boost converter is now given per (2-3) and the frequency response is shown in Figure 2-3.

2-3-1 Controller Formulation

Obviously, from Figure 2-3, because of the excessive phase lag caused by the RHP zero, a PI controller is not enough to provide acceptable gain margin and phase margin along with a reasonable bandwidth. Hence, standard classical design uses a lead compensator to compensate for the extreme phase lag caused by RHP zero. So, the controller will consist of two parts: the PI controller and a cascaded lead compensator. PI controller transfer function is given by:

$$G_{PI} = K_p + \frac{K_i}{s}$$

Practically, proportional part of the controller K_p is physically implemented with a low-pass filter to avoid noise amplification. Consequently, the PI controller transfer function is as follows:

$$G_{PI} = \frac{K_p}{1 + T_p s} + \frac{K_i}{s} \qquad (2\text{-}6)$$

where T_p is the filter time constant.

The lead compensator transfer function is as follows:

$$G_{lead} = K_c \alpha \frac{Ts + 1}{\alpha Ts + 1} = K_c \frac{s + \frac{1}{T}}{s + \frac{1}{\alpha T}} \qquad (2\text{-}7)$$

Since $0 < \alpha < 1$, the zero $-\frac{1}{T}$ is always placed to the right of the pole $-\frac{1}{\alpha T}$ in the s-plane. The minimum value of α is limited by the physical implementation constraints and it usually taken to be about 0.05 [16]. For minimum value of 0.05 the maximum phase lead that might be added by the lead compensator is about 65°.

Consequently, the feedback controller will be:

$$G_c = G_{PI} \cdot G_{lead} \tag{2-8}$$

The feedforward controller from line voltage change (V_{iref} - v_i) to control input d used in this thesis is a proportional controller with a gain K_v. So, the boost converter controller K will be:

$$K = [G_c \quad K_v] \tag{2-9}$$

Figure 2-6 shows the block diagram of the controller K along with the boost converter. Design guidelines to choose the controller parameters will be discussed in the next subsection.

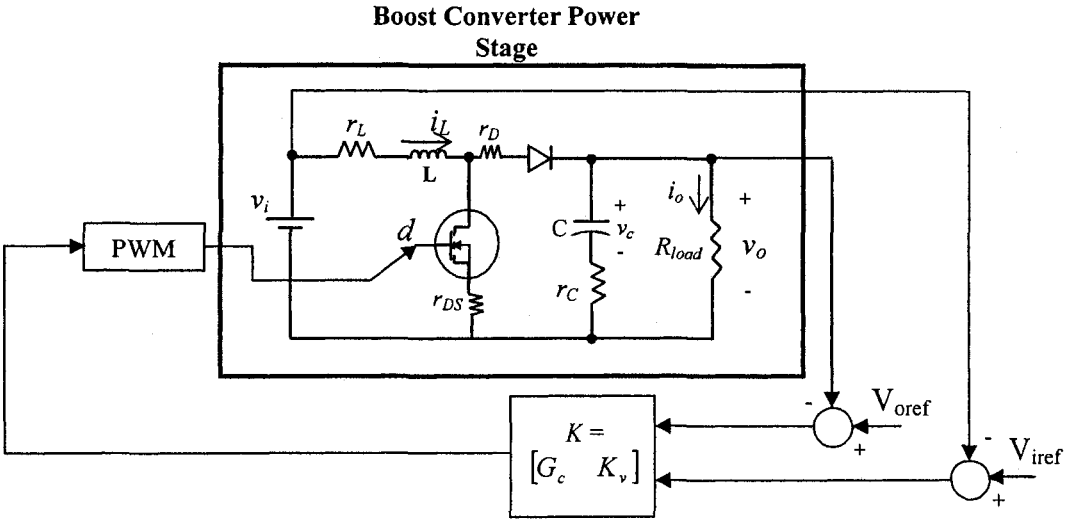


Figure 2-6: Controller diagram of the boost converter

2-3-2 Design Guidelines:

Simple and comprehensible tuning guidelines to choose the PI and the lead compensator parameters to control boost converter are given by the following procedure:

Step 1: Initially, $T_p = 0$ will set a pure PI controller.

Step 2: A reasonable value for K_p will be chosen which is not very far from unity to minimize the proportional control effort to avoid noise amplification. Practically, it would be in the range between 1 and 5.

Step 3: K_i is chosen taking into account two conflicting objectives. Firstly, K_i is chosen to attain high loop gain at low frequencies and high bandwidth as much as possible.

Secondly, K_i should be chosen so that the zero introduced by PI controller will roughly cancel the -90° phase lag added by the integrator before the system phase lag starts to increase beyond 180° phase lag leaving the lead compensator to take care of this excessive phase lag. The PI zero can be determined as follows:

$$G_{PI} = K_p + \frac{K_i}{s} = K_i \frac{1 + \frac{K_p}{K_i} s}{s}$$

$$G_{PI} = K_i \frac{1 + T_{pi} s}{s} \qquad (2\text{-}10)$$

where

$$T_{pi} = \frac{K_p}{K_i} \qquad (2\text{-}11)$$

Therefore, K_i is chosen so that the zero $1/T_{pi}$ will be located somewhere to the left of the phase crossover frequency guaranteeing the reduction of the -90° added by the integrator. Then, the frequency response (Bode plot) of $(G_{pi}G)$ will be plotted to ensure that the appropriate values of K_p and K_i have been chosen.

Step 4: K_c and α are set initially to 1 and 0.05, respectively. The minimum value for α is chosen to acquire the maximum phase lead from the lead compensator which is 65° [16]. The maximum phase lead $\varphi_m = 65°$ is introduced at a frequency ω_m (rad/sec.) which is the geometric mean of $1/T$ and $1/\alpha T$ [16] and can be calculated by:

$$\omega_m = \frac{1}{\sqrt{\alpha} T} \qquad (2\text{-}12)$$

And $|G_{lead}(j\omega_m)|$ can be calculated from (2-7) as follows:

$$|G_{lead}(j\omega_m)| = 20\log\left(K_c\sqrt{\alpha}\right) \text{ dB} \qquad (2\text{-}13)$$

Then, ω_m will be chosen as the frequency at which $\left|G_{pi}(j\omega)G(j\omega)\right| = -\left|G_{lead}(j\omega_m)\right|$. Finally, T can be calculated from (2-12). In conclusion, the lead compensator initial design will be in three steps as follows:

1- Determine $\left|G_{lead}(j\omega_m)\right|$ from (2-13) assuming $K_c = 1$ and $\alpha = 0.05$

2- From the frequency response of $G_{pi}(j\omega)G(j\omega)$, find the frequency at which $\left|G_{pi}(j\omega)G(j\omega)\right| = -\left|G_{lead}(j\omega_m)\right|$ and consider it as ω_m

3- Calculate T from (2-12)

Finally, the frequency response (Bode plot) of $G_{pi}G_{lead}G$ will be plotted to check the gain and phase margins.

Step 5: The pole $1/T_p$ of the proportional controller filter will be initially chosen approximately at the corner frequency of the last break point of the asymptotic Bode plot of $G_{pi}G_{lead}G$ to attenuate the high frequency components. Then, the Bode plot of the final system will be plotted to check the gain and phase margin and assess the system performance toward retuning the controller parameters if there is a need.

Step 6: The controller will be assessed based on gain and phase margins, system bandwidth, time response simulation of the system against the expected input voltage and load disturbances. Based on this assessment the controller parameters will be retuned using the tips given bellow.

Tuning Tips:

1- Shifting the pole $1/T_p$ to the right in the Bode plot will slightly increase the gain margin and phase margin because this will reduce the effect of the phase lag added by the pole, consequently, increasing the phase margin, phase crossover frequency and the gain margin. Also, shifting $1/T_p$ will cause a very small decrease in the system bandwidth because $1/T_p$ is far away to the right of the gain

crossover frequency in the Bode plot. However, pushing the pole $1/T_p$ to the right will increase the high frequency components in the system leading to a higher noise transmission in the practical system.

2- Shifting ω_m slightly to the right will increase the gain and phase margins because it will shift the phase crossover frequency to the right which increases the gain margin, and shift the gain crossover frequency to the left increasing the phase margin. However, shifting the gain crossover frequency to the left means decreasing the system bandwidth.

3- When phase lead greater than 65° is needed, the gain crossover frequency should be shifted a little to the left to avoid the region where the phase lag is too high. This can be done by choosing $K_c < 1$ and then recalculating ω_m using Step 4.

4- When changing K_i vastly during retuning, K_p should be changed by the same ratio to guarantee that Step 3 second objective is fulfilled.

2-3-3 Controller Design:

The design procedure and tips will be used in this section to design the controller for the boost converter in [8] for which the control-to-output transfer function and frequency response are given by (2-3) and Figure 2-3, respectively. The design is carried out in the following steps:

1- let $T_p = 0$, choose $K_p = 2$. It is obvious from Figure 2-3 that the phase lag of the system starts to increase beyond 180° at 12.2×10^3 rad/sec. Choosing $K_i = 4300$ (1/sec) will locate the PI zero at 2.15×10^3 rad/sec which compensates for most of the phase lag added by the integrator and produces a reasonable high gain at low frequencies (reasonable bandwidth). Figure 2-7 shows the Bode Plot of G, G_{pi} and $G_{pi}G$. It is clear from Figure 2-7 how the zero of the PI compensates for the -90° added by the integrator.

2- For $K_c = 1$ and $\alpha = 0.05$, $|G_{lead}(j\omega_m)|$ is calculated using (2-13) and it is given by:

$$|G_{lead}(j\omega_m)| = -13 \text{ dB}$$

From the frequency response of $G_{pi}G$ (Figure 2-7):

$$|G_{pi}(j\omega)G(j\omega)| = -|G_{lead}(j\omega_m)| = 13 \text{ dB at } \omega \cong 10.6\times10^3 \text{ rad/sec}$$

Considering $\omega_m = 10.6\times10^3$ rad/sec, 1/T will be calculated using (2-12) with α =0.05 as :

$$\frac{1}{T} = \omega_m\sqrt{\alpha} = 2370.23 \text{ rad/sec}$$

So that, the lead compensator will have a zero at $-1/T$ = –2370.23 rad/sec and a pole at $-1/\alpha T$ = –47404.64 rad/sec. This completes the lead compensator primary design. Figure 2-8 shows the frequency response of $G_{pi}G$, G_{lead}, $G_{pi}G_{lead}G$ and the gain margin and phase margin of $G_{pi}G_{lead}G$. The figure shows that the gain crossover frequency (10.5×10^3 rad/sec) is so close to what is expected above (10.6×10^3 rad/sec).

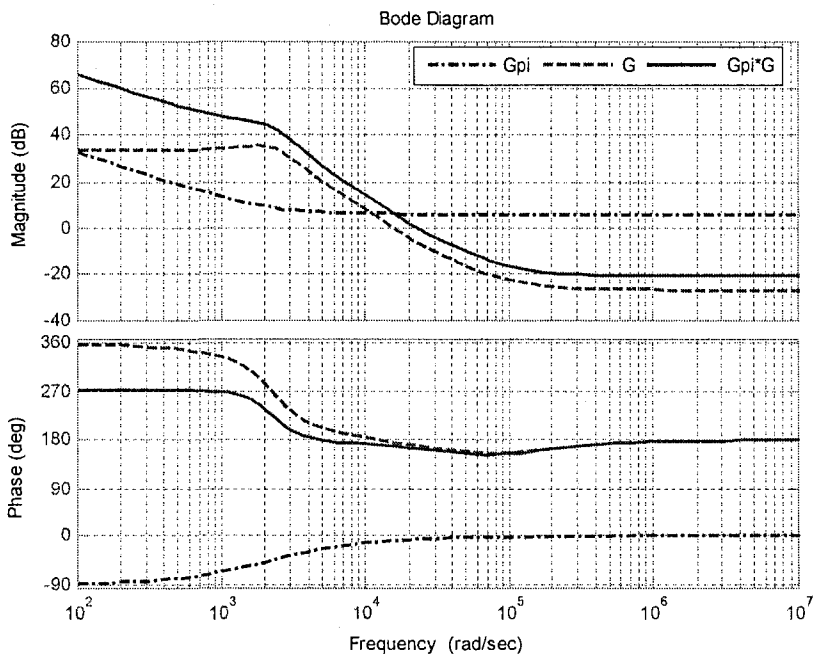


Figure 2-7: Frequency response of G, G_{pi} and $G_{pi}G$

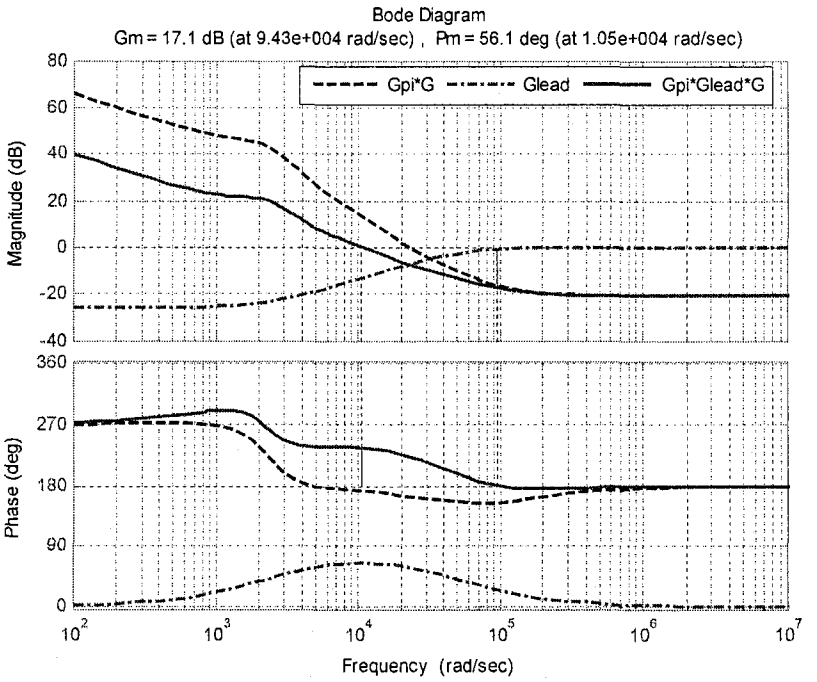


Figure 2-8: Frequency response of $G_{pi}G$, G_{lead}, $G_{pi}G_{lead}G$

3- The only remaining parameter to choose is $1/T_p$ which according to Step 5 will be located roughly at the corner frequency of the last asymptote in the frequency response. Using Figure 2-8, $1/T_p$ will be located at 0.1×10^6 rad/sec which is the corner frequency of the last asymptote. The ensuing controller will be called G_{c1} to compare it to other retuned controllers. This controller is shown in Table 2-1 as a part of the controller K_1.

Figure 2-9 shows the loop gain of the resultant system controlled by G_{c1} which demonstrates a gain margin of 12.3 dB, phase margin of 50.2°, and bandwidth of 10.6×10^3 rad/sec

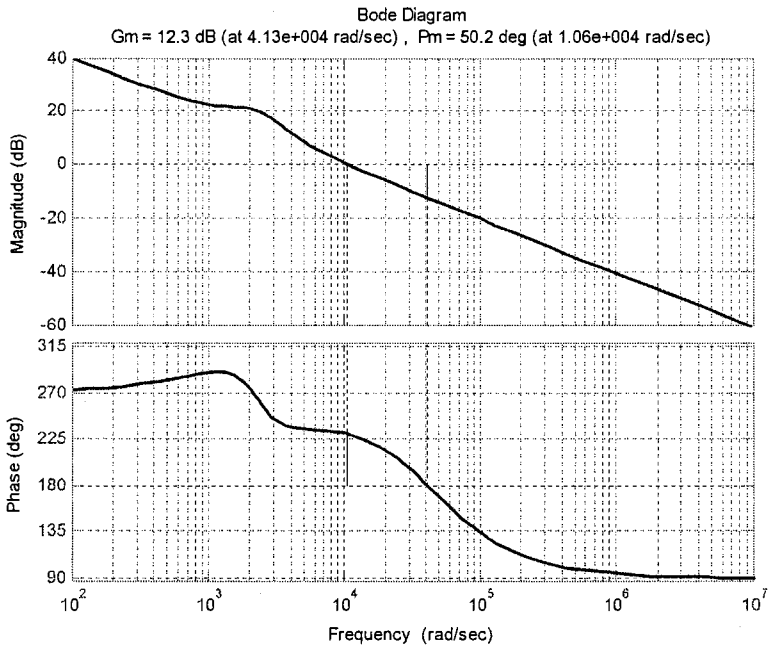


Figure 2-9: Loop gain frequency response of the G_{c1} controlled system

4- As mentioned in Step 6, the controller assessment will be based on the ensuing gain margin, phase margin, bandwidth of the system and the simulated time response. It is quite obvious that the gain and phase margin values and bandwidth of the system using the controller G_{c1} are quite reasonable. However, gain margin and phase margin can be increased using Tip 1 and Tip 2 as follows:

a) According to Tip1, margins can be increased a little by shifting the pole $1/T_p$ to the right of the Bode plot. By shifting $1/T_p$ from 0.1×10^6 to 0.25×10^6 rad/sec, the new controller G_{c2} is obtained. This is shown in Table 2-1 as a part of the controller K_2.

Figure 2-10 shows the frequency response of the loop gain using the Controller G_{c2}. It is clear from the figure that the gain margin increased from 12.3 dB to 14.1 dB and phase margin increased from 50.2° to 53.7°.

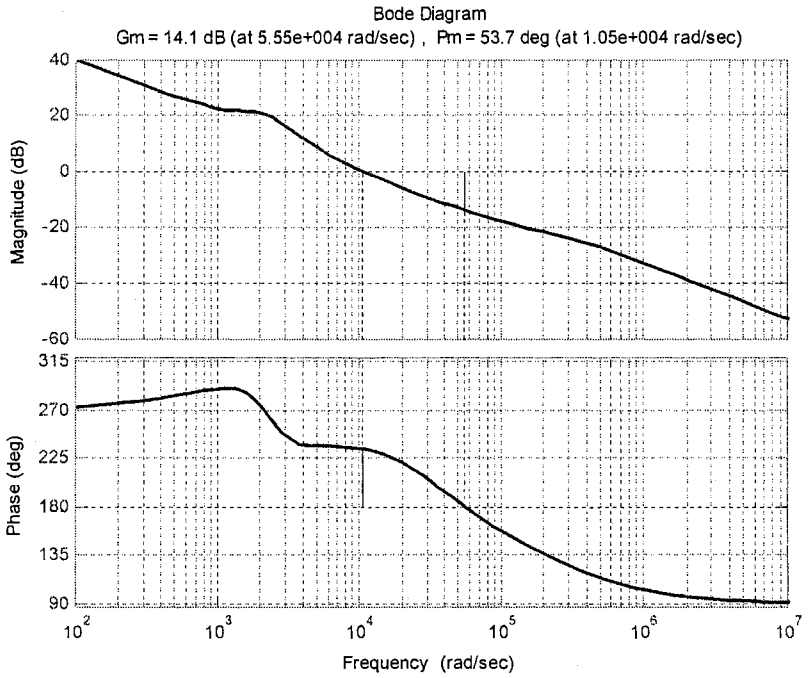


Figure 2-10: Loop gain frequency response in the G_{c2} controlled system

b) Consistent with Tip 2, the gain and phase margin can be increased by shifting ω_m to the right but this will be done at the expense of decreasing the bandwidth. It can be seen that by shifting ω_m to the right from 10.6×10^3 rad/sec to 14.5×10^3 rad/sec, the controller G_{c3} will produce a loop gain frequency response (Figure 2-11) very close to that of the H_∞ controller designed in [8] and discussed in the previous section. G_{c3} parameters are given in Table 2-1 as a part of the controller K_3.

Figure 2-11 shows the loop gain frequency response of H_∞ controlled system and G_{c3} controlled system along with the gain and phase margins for the G_{c3} controlled system which shows the close match between the two controllers with slightly larger gain and phase margins in G_{c3} case.

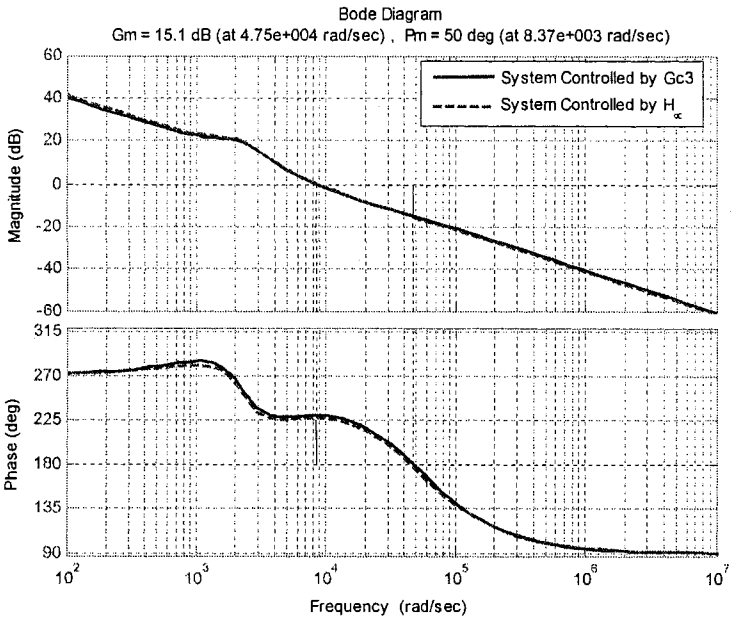


Figure 2-11: Loop gain frequency response of H_∞ controlled system and G_{c3} controlled system

The forward control gain (K_v) has been chosen by experience and based on simulation results as $K_{v1} = K_{v2} = 0.042$ while K_{v3} has been chosen the same as the feed forward gain used in the H_∞ controller in [8] which is 0.039 to show the match in the time response between the two controllers. Hence, the three controllers are given by:

$$\begin{aligned} K_1 &= [G_{c1} \quad K_{v1}], \\ K_2 &= [G_{c2} \quad K_{v2}], \\ K_3 &= [G_{c3} \quad K_{v3}] \end{aligned} \tag{2-14}$$

Table 2-1

Controller	G_c						K_v
	K_p	K_i	$1/T_p$	K_c	α	$1/T$	
K_1	2	4300	0.1×10^6	1	0.05	2370.23	0.042
K_2	2	4300	0.25×10^6	1	0.05	2370.23	0.042
K_3	2	4300	0.1×10^6	1	0.05	3249.61	0.039

2-3-4 Simulation Results:

Simulation has been carried out using MATLAB Simulink environment. The boost converter power stage dynamic behavior was simulated using S-Function. There are three different sets of the differential equations describing the three topological modes of the boost converter. However, instead of using the averaged and linearized approximated model, S-Function allows solving the corresponding differential equations based on switch status and conduction mode. Hence, the S-Function will describe dynamic behavior of the boost converter using different sets of differential equations combined by (1-22), (1-23) and (1-24) based on switch status and conduction mode.

Boost converter parameters used in the simulation are shown in Figure 2-1 with a switching frequency of 100 KHz. An input voltage disturbance of 3 V (25%) over a line voltage of 12 V and a load disturbance of 0.1 A ($\cong 20\%$) over an average load current of 0.545 A were used in simulation to test the controllers. These disturbance values used in simulation are the same as those used in [8] to compare the controller designed using classical frequency response method with the H_∞ controller designed in [8].

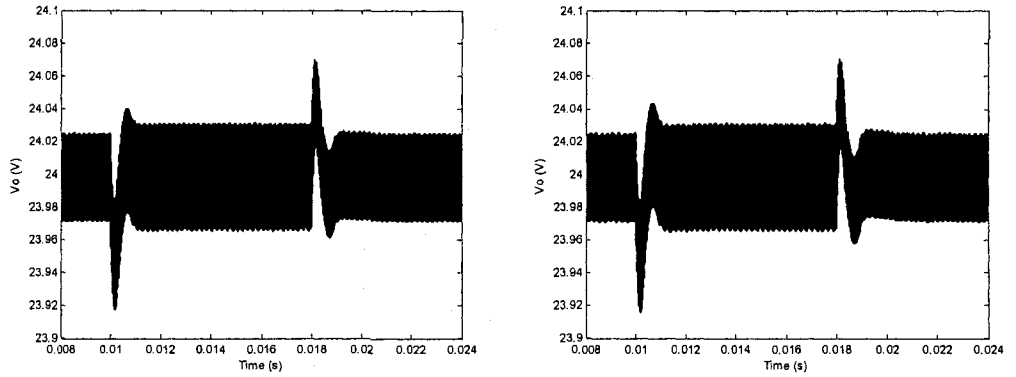
A load perturbation of 0.1 A is introduced at t=0.01s and -0.1 A at t=0.018s. Similarly, input voltage perturbation of -3 V is introduced at t=0.01s and +3 V at t=0.018s. All of the four controllers K_1, K_2, K_3, and H_∞ were used in the simulation to compare performance of these controllers.

Figure 2-12 and Figure 2-13 show the response of the systems controlled by H_∞ and K_3 against the mentioned disturbances. As expected from the well matched frequency responses of the two systems, the time responses are also close indicating the ability of the frequency response design method to produce a controller similar to the H_∞ controller.

Figure 2-14 and Figure 2-15 show the response of the systems controlled by H_∞ and K_1 against the load and input voltage perturbations. The responses show a superior performance of K_1 controller to the H_∞ controller in terms of settling time and damping behavior. Also, the value of $K_{v1} = K_{v2} = 0.042$ produces better disturbance rejection for line voltage disturbance than that of $K_{v3} = 0.039$ used in [8].

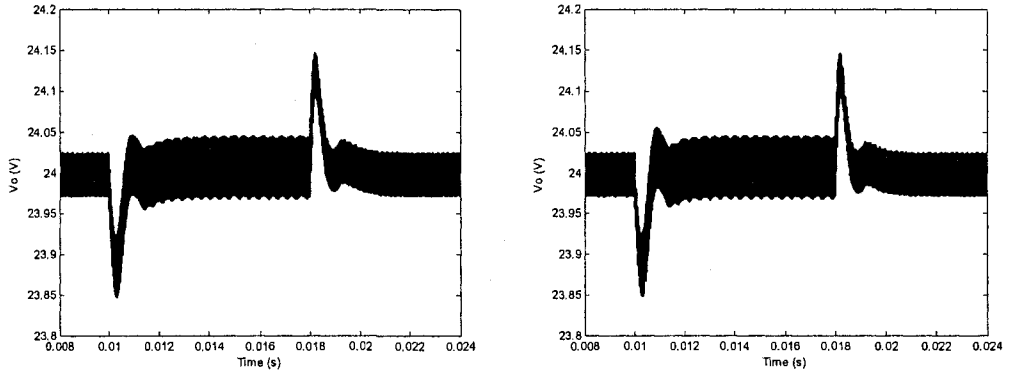
Finally, performance of K_1 and K_2 controllers for load and line voltage disturbances is shown in Figure 2-16 and Figure 2-17. Recalling that K_2 parameters are the same as

those of K_1 except that $1/T_p$ is shifted to the right from 0.1×10^6 rad/sec in K_1 to 0.25×10^6 rad/sec in K_2, the response of the system controlled by K_2 shows less damping illustrated by the larger overshoot. As mentioned before, this is already expected because shifting $1/T_p$ to the right will increase the high frequency components in the output response. Thus, Figure 2-16 and Figure 2-17 are shown to illustrate the effect of shifting $1/T_p$ further to the right during retuning process.



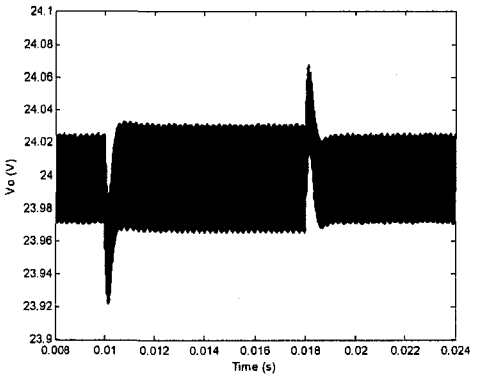
(a) K_3 Controller (b) H_∞ Controller

Figure 2-12: Simulated output behavior for load disturbance

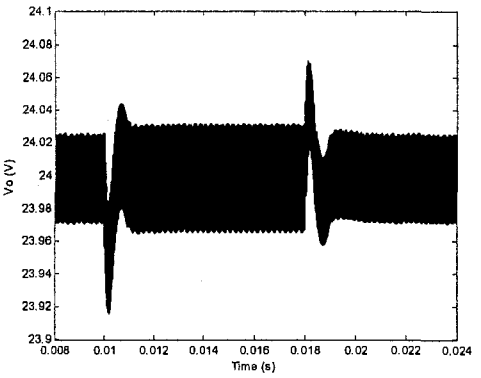


(a) K_3 Controller (b) H_∞ Controller

Figure 2-13: Simulated output behavior for line voltage disturbance

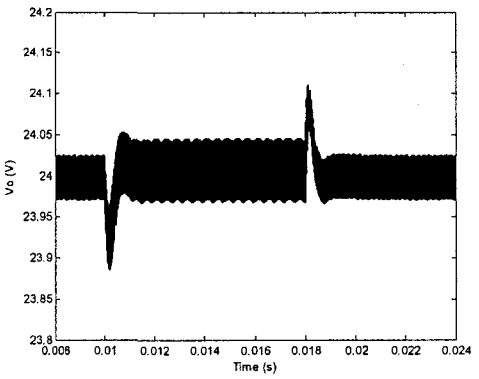


(a) K_I Controller

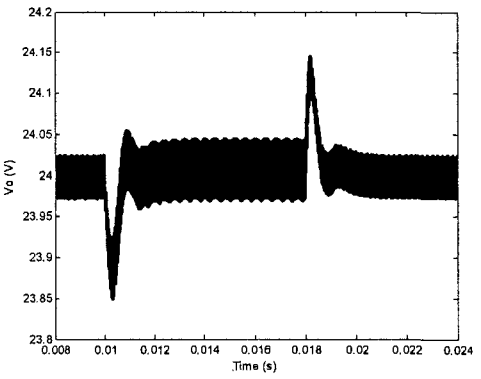


(b) H_∞ Controller

Figure 2-14: Simulated output behavior for load disturbance

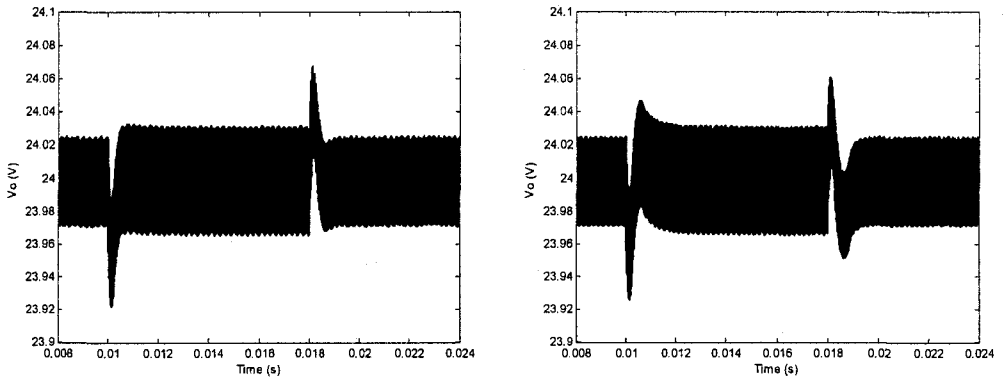


(a) K_I Controller



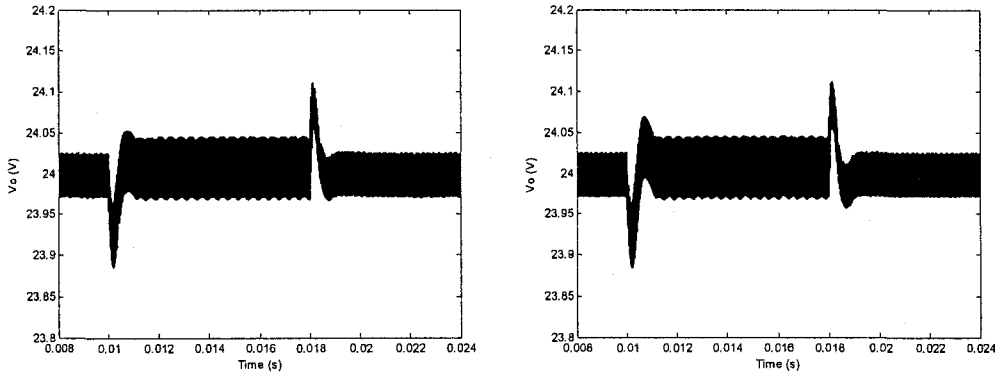
(b) H_∞ Controller

Figure 2-15: Simulated output behavior for line voltage disturbance



(a) K_1 Controller (b) K_2 Controller

Figure 2-16: Simulated output behavior for load disturbance



(a) K_1 Controller (b) K_2 Controller

Figure 2-17: Simulated output behavior for line voltage disturbance

To summarize, the simulations demonstrate the superiority of K_1 controller over the other designed controllers and the H_∞ controller. K_3 and H_∞ controllers produce very close responses and margins as expected by their frequency responses. K_2 controller is used only to illustrate the effect of pushing the pole $1/T_p$ further to the right in the Bode plot during the retuning process.

2-4 Robust Stability:

Robust stability of the designed systems against input voltage disturbance, load disturbance and boost converter parameters uncertainty will be examined in this section. Boost converter components variations and system disturbances that will be used to investigate the robustness of the system are given in (2-15).

$$\begin{aligned} C &= C_n \pm \Delta C \\ L &= L_n \pm \Delta L \\ V_i &= V_{in} \pm \Delta V_i \\ I_o &= I_{on} \pm \Delta I_o \end{aligned} \qquad (2\text{-}15)$$

Where C_n, L_n, V_{in} and I_{on} are the nominal values of C, L, V_i and I_o. Frequency responses of the uncertain system controller by K_1 in Section (2-3) corresponding to all combination of parameter variations and system disturbances (nominal and limit values) given in (2-15), with ΔC, ΔL, ΔI_o=20% and ΔV_i =25% from the nominal are shown in Figure 2-18. Using this combination of frequency responses it is too hard to determine robust stability. However, two approaches are available in robust control theory to determine the robustness of linear systems. Unstructured uncertainty is the most common approach. In this approach, the variation in the uncertain system frequency response is modeled using frequency dependent weighting functions.

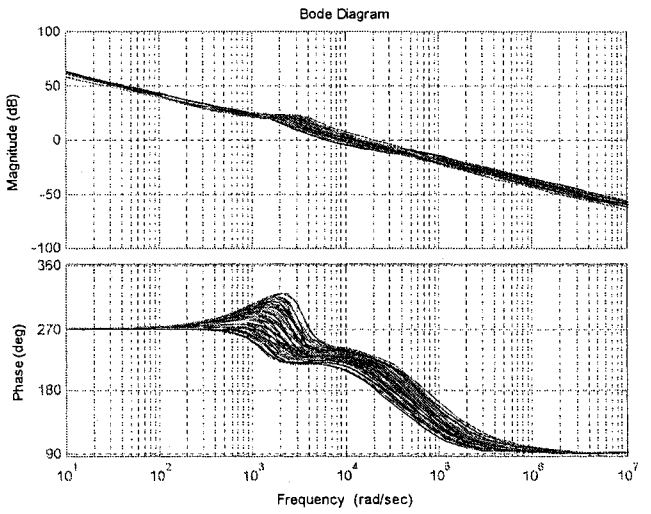


Figure 2-18: Frequency responses of the uncertain systems (controlled by K_1) subsequent to the parameters variations and disturbances (nominal and limit values)

The conservative result is the main drawback of this approach [6, 15] because of the following two reasons:

1- The controller will be designed to accommodate for a conservative level of uncertainty which is larger than what is really needed to represent physical parameter variations and system disturbances variations [6].

2- Uncontrolled phase variability [15] because this method is based on fitting the envelope magnitude of the relative error, between the nominal and the uncertain frequency responses, to a weight transfer function without any attention to the phase.

The second approach is the structured uncertainty approach developed in [6]. In this approach boost component variations are modeled as a structured uncertainty to be used in the initial design steps to avoid the conservativeness of the unstructured uncertainty approach. The main drawback is the complexity of the method which is based on complicated matrix decompositions. Further, [6] does not include the line voltage perturbations in the analysis. To avoid the drawbacks of the previous two methods, simple robustness test is proposed and presented in the next section.

2-4-1 Worst case Stability Frequency Response Approach:

The effect of each parameter variation and system disturbance on the dynamics of the boost converter closed loop system has been investigated to obtain a certain set of variations that lead to the worst case stability frequency response, in terms of gain and phase margin. This parameter variation set is given by (2-16)

$$\begin{aligned} C &= C_n - \Delta C \\ L &= L_n + \Delta L \\ V_i &= V_{in} - \Delta V_i \\ I_o &= I_{on} + \Delta I_o \end{aligned} \qquad (2\text{-}16)$$

Any change in the conditions (2-16) will result in a more stable system, larger phase and gain margin. Investigating the stated conditions in (2-16) shows that negative line

disturbance and positive load disturbance will increase inductor current in the regulated system and the inductance value is expected to decline, due to the flux saturation effect of the inductor, or at least stay at its nominal value rather than increase as postulated. So that, conditions in (2-16) are not expected to happen concurrently. However, in practice it is hard to predict the nominal value of the inductance and a range for inductance value is usually supplied by the manufacturer; hence, it is safer to use the conditions in (2-16).

Boost converter parameter variations and disturbances used to examine the robustness of the system designed in Sections (2-2) and (2-3) are given by:

C=220μF±20%

L=220μH±20%

V_i =12V±25% ≡ (12±3V)

I_o =0.545A±20% ≡ (0.545±0.1A), which is equivalent to R_{load} range of [37.183Ω, 53.9Ω]

Hence, Figures 2-19, 2-20 and 2-21 show the frequency response along with gain and phase margins for the worst case stability for systems controlled by K_1, K_3 and H_∞, respectively. All figures show stable systems with gain and phase margins given in Table 2-2. Therefore, the three systems are robustly stable against the given parameters uncertainty and the given small disturbances when examined with frequency response technique.

Table 2-2

Controller	Gain Margin (dB)	Phase Margin (°)
K_1	5.78	31.2
K_3	8.52	31.8
H_∞	8.23	28.3

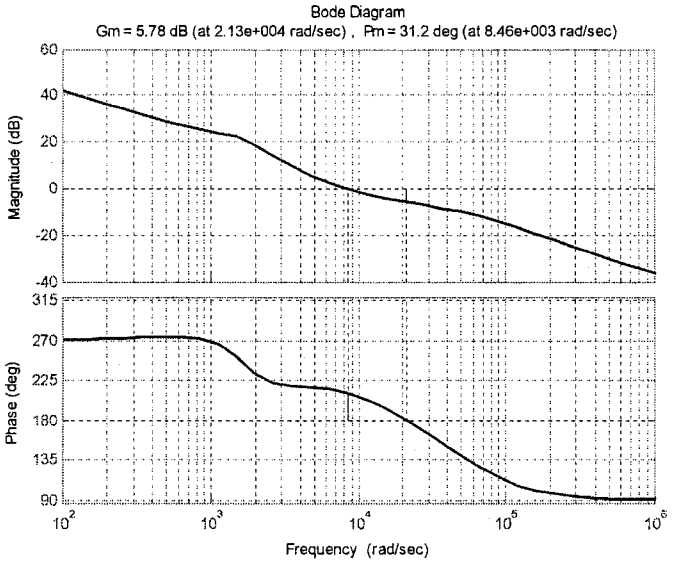


Figure 2-19: Worst case stability margins for K_1 controlled system

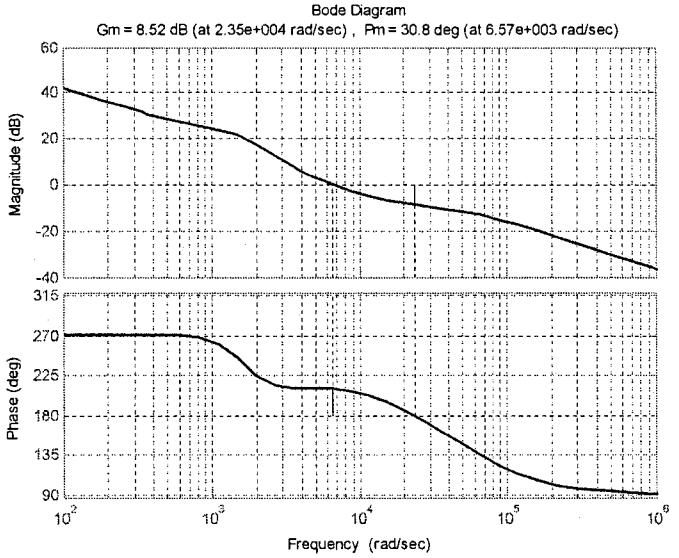


Figure 2-20: Worst case stability margins for K_3 controlled system

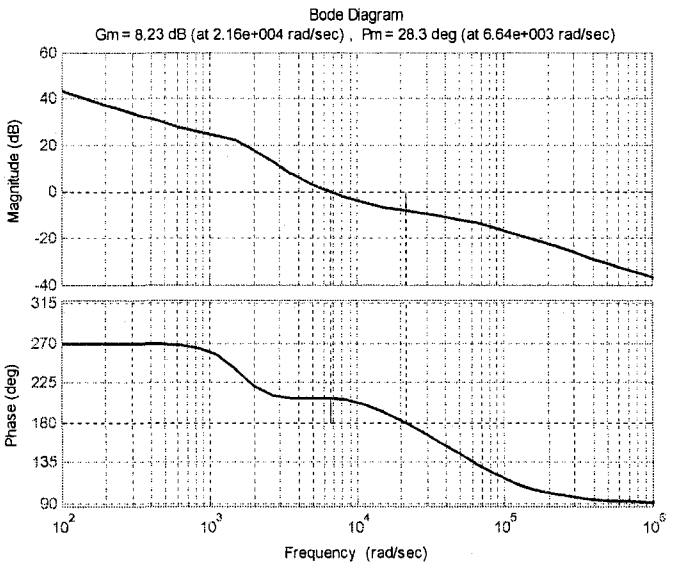


Figure 2-21: Worst case stability margins for H_∞ controlled system

Robust performance is examined for the worst case frequency response by applying a load perturbation of 0.1A (20%) at t=0.01s followed by line voltage perturbation of -3V (25%) at t=0.018s for the boost converter in Figure 2-5 with C = 176μF (220μF-20%) and L= 264μH (220μH + 20%). Figures 2-22, 2-23 and 2-24 show the system performance for the worst case for systems controlled by K_1, K_3 and H_∞, respectively.

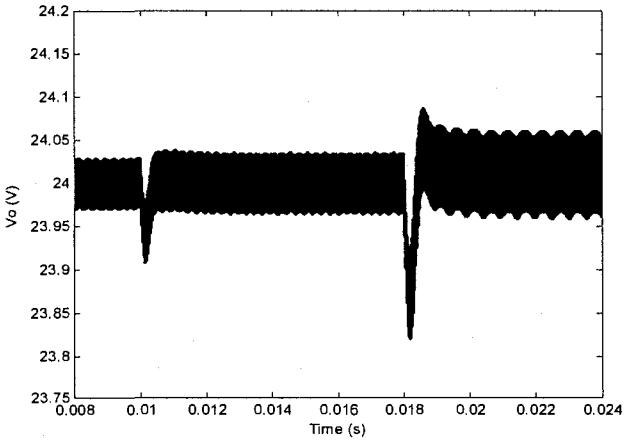


Figure 2-22: v_o performance of the worst case stability for system controlled by K_1,
20% load disturbance at 0.01s followed by
25% line voltage disturbance at 0.018s

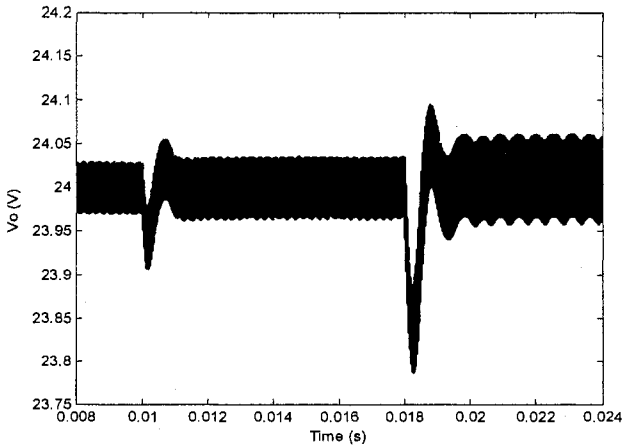


Figure 2-23: v_o performance of the worst case stability for system controlled by K_3,
20% load disturbance at 0.01s followed by
25% line voltage disturbance at 0.018s

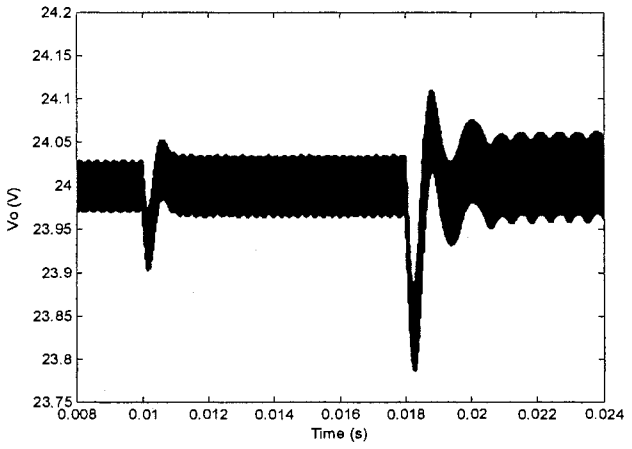


Figure 2-24: v_o performance of the worst case stability for system controlled by H_∞,
20% load disturbance at 0.01s followed by
25% line voltage disturbance at 0.018s

Again, K_3 shows a similar or slightly better performance than that of H_∞, and K_1 shows robust performance which is superior to K_3 and H_∞ for small disturbances.

2-4-2 Unstructured Uncertainty Approach:

In this section, multiplicative input uncertainty will be used to determine robust stability of the boost converter control systems designed in Sections 2-2 and 2-3. Figure 2-25(a) shows the boost converter control system block diagram with the presence of the multiplicative input uncertainty used to model the uncertainty in the system parameters and system disturbances. Figure 2-25(b) shows the augmented block diagram of the system that will be used to determine the robust stability using μ analysis for robust stability.

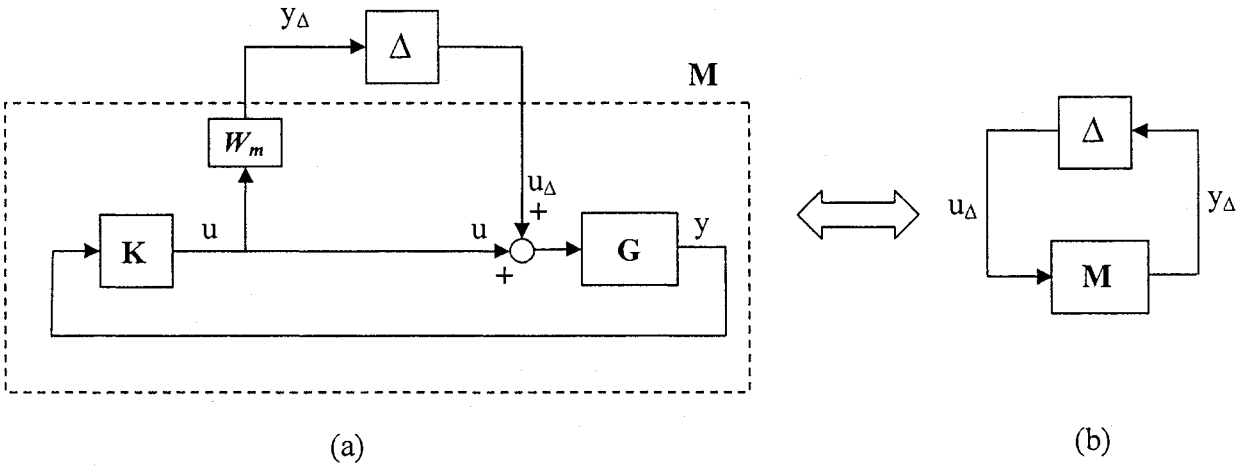


Figure 2-25: Block diagram of the boost converter system in the presence of multiplicative input uncertainty

Where:

$$|W_m(j\omega)| \geq \frac{|G_p(j\omega) - G(j\omega)|}{|G(j\omega)|} = l_i(j\omega) \qquad (2\text{-}17)$$

$W_m(j\omega)$: Multiplicative uncertainty weight
$G(j\omega)$: Nominal boost converter transfer function
$G_p(j\omega)$: Perturbed transfer function
$l_i(j\omega)$: Relative error
Δ(jω) : Stable transfer function with $\max_{\omega} \bar{\sigma}[\Delta(j\omega)] \leq 1$

An uncertain system is stable if [17]

$$\max_{\omega} \ \mu_{\Delta}(j\omega) < 1 \tag{2-18}$$

where:

$$\mu_{\Delta}(M) := \frac{1}{\min\{\bar{\sigma}(\Delta) : \Delta \in \mathbf{\Delta},\ \det(I - M\Delta) = 0\}} \tag{2-19}$$

and $\bar{\sigma}$ is the maximum singular value.

The same boost converter component deviations and system disturbances limits used in Section 2-4-1 will be used here to determine the robust stability using this approach. Corresponding to these uncertainties, the magnitude of the relative errors and the multiplicative uncertainty (W_m) frequency response are shown in Figure 2-26. It is quite obvious that the magnitude of W_m represents the envelope of the magnitude of the relative errors, taking into account only the maximum outcoming magnitude of the relative errors and without any consideration for phase variability of the W_m which are the main reasons for the conservative results of this method. The multiplicative weight transfer function W_m (the envelope) is represented by the 8th order transfer function, calculated following steps in [18], and given by:

$$W_m = \frac{0.683s^8 + 1.753*10^5 s^7 + 8.75*10^9 s^6 + 2.671*10^{14} s^5 + 2.186*10^{18} s^4 + 9.308*10^{21} s^3 + 1.676*10^{25} s^2 + 2.783*10^{28} s + 9.79*10^{30}}{s^8 + 1.849*10^5 s^7 + 1.011*10^{10} s^6 + 2.481*10^{14} s^5 + 1.812*10^{18} s^4 + 7.794*10^{21} s^3 + 2.141*10^{25} s^2 + 3.113*10^{28} s + 3.143*10^{31}}$$

(2-21)

The μ_{Δ} analysis for robust stability for systems controlled by K_1, K_3 and H_∞ controllers, and according to the mentioned uncertainties, is illustrated in Figure 2-27. As can been seen from Figure 2-27 the three systems are not robustly stable according to this approach because $\max_{\omega} \ \mu_{\Delta}(j\omega) \geq 1$ for certain range of frequency. The controllers should be redesigned to guarantee the robust stability. As an example, the controller gain of K_1 (Table 2-1) will be reduced by using K_p=0.25 and K_i=900, with the same lead compensator parameters. This new controller is referred to as K_4. The μ_{Δ} analysis for robust stability for systems controlled by K_4, is illustrated in Figure 2-27(d).

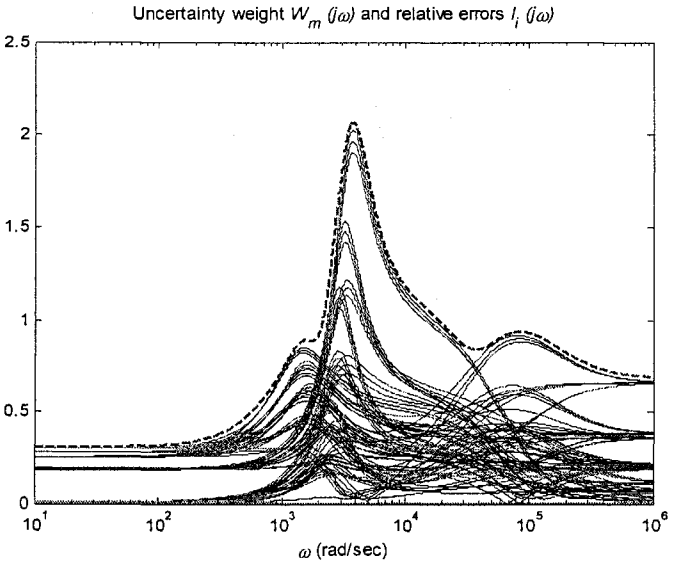
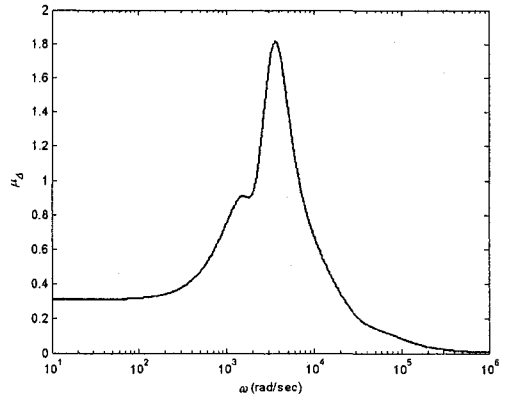


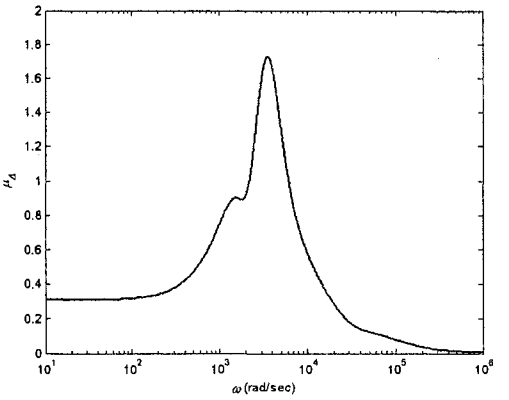
Figure 2-26: Uncertainty weight and relative errors

_____ relative errors

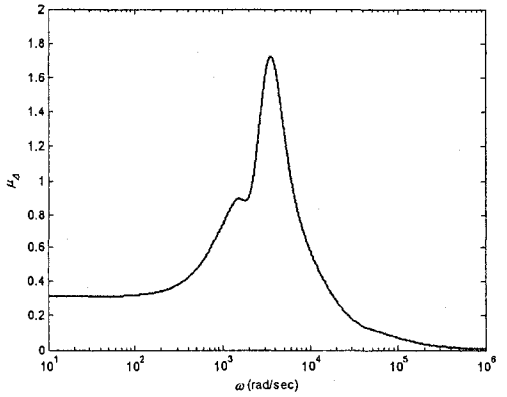
---------- uncertainty weight



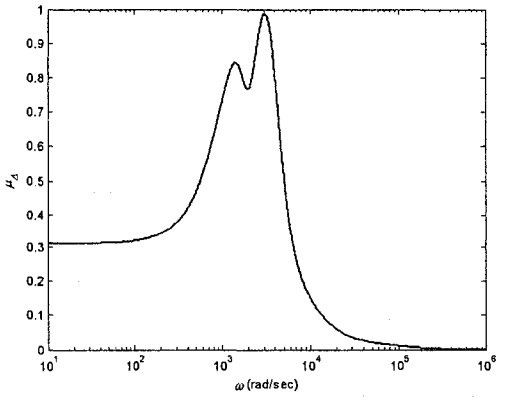
(a) K_1 Controller



(b) K_3 Controller



(a) H_∞ Controller

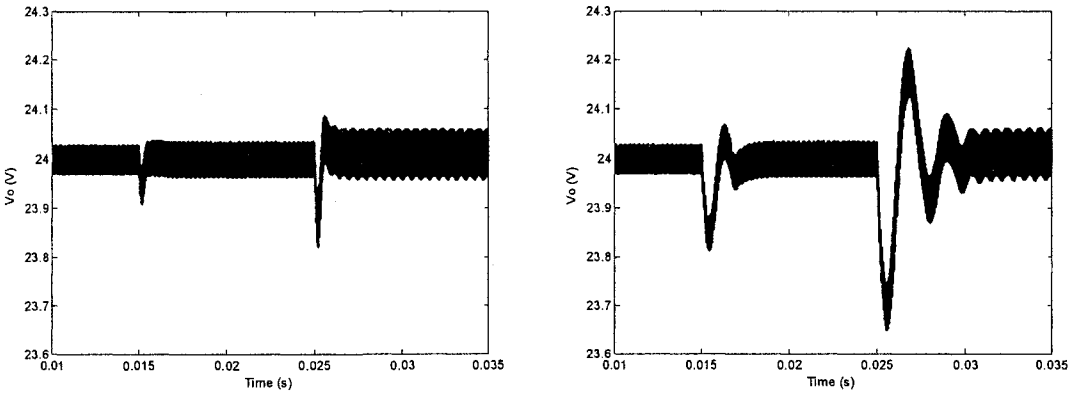


(b) K_4 Controller

Figure 2-27: μ_Δ analysis for robust stability

As can bee seen from Figure 2-27(d) the peak of μ_Δ for the system controlled by K_4 is 0.9869 and occurs at ω=3709 rad/sec. Therefore, the system is robustly stable, according to this approach, for the investigated uncertainties and for $\max_{\omega} \bar{\sigma}[\Delta(j\omega)] < \frac{1}{0.9869} = 1.0133$.

Now, the performance of the controllers K_1 and K_4 will be compared based on the worst case parameters and disturbances that can happen. Figure 2-28 presents the simulation results corresponding to the worst case stability conditions set discussed in Section (2-4-1). Practically, both controllers are robustly stable; however, controller K_4 shows a much poorer response than K_1 because of the conservative unstructured uncertainty approach used to examine robust stability which applies conservative virtual restrictions that can not happen in reality, on the design of the controller.



(a) K_1 Controller (b) K_4 Controller

Figure 2-28: Output voltage performance of the worst case stability

Chapter 3

Parasitics and Voltage Collapse of the Boost Converter

Most of the reviewed literature and the boost converter controllers designed in previous chapters considered only small disturbances in the design and in the test of the control system. For large disturbances, the boost converter nonlinearity is the main challenge in the analysis and design of the robust controllers. The nonlinearity arising from parasitic parameters in a boost converter is investigated in this chapter. It is shown that this nonlinearity can cause a serious instability problem for boost converter control because it makes robust controller design difficult due to the sensitivity to disturbances in the presence of parasitic parameters. Static and dynamic voltage collapse is studied. New non-iterative formulae are derived using the bilinear averaged model to calculate the voltage collapse point due to the parasitic parameters. Using these simple formulae boost converter operating region and disturbance limits can be calculated in the design phase. The use of these formulae in the design of the boost converter control system is studied. Boost converter disturbance and operating limits calculated using the derived formulae are verified using switched nonlinear circuit model based simulations. Also, in this chapter, a passivity based integral control designed for large disturbances will be investigated and compared to the proposed controller of Section 2-3.

3-1 Introduction

Boost converter nonlinearity is the main challenge in the analysis of the boost converter behavior and in the design of appropriate robust controllers. To avoid the difficulty of designing the controller for the nonlinear converter, small-signal linear models are widely used for design purposes and the boost converter is linearized around a chosen operating point. However, these linear models are valid only for a small region

around the operating point where the disturbances are small compared to the operating point values. The small-signal linear model can not give reliable information about the system performance for large disturbances. Large-signal stability analysis and control design has been investigated in [19, 20, 21, 22, 23].

In [19], the instabilities of the boost converter caused by large variations of system parameters are investigated using multiple-parameter, bifurcation-theory oriented approaches for the special case of full state-feedback control. It is shown that, both static bifurcation (jump phenomenon) and dynamic bifurcation (limit cycles) can occur at critical points.

Large-signal stability analysis and design is also discussed in [20, 21, 22]. Linear state-feedback control is assumed in these papers as it leads to simple derivation of the closed loop model of the system making it conducive to apply the stability condition and obtain the feedback gains to guarantee large-signal stability. However, the designed linear state-feedback regulators exhibit poor regulation and slow response and therefore cannot be used in practice. The requirement of continuous current measurements for state-feedback controllers adds to the cost of the controllers for such converters. In [23], a passivity based principle has been used as in [22] but with additional integral control to produce a nonlinear controller to guarantee global stability and zero steady state error. Nevertheless, the polarity of the applied input voltage and load disturbances to examine the stability for large disturbance are in a direction that pushes the system towards a more stable region. This cannot reveal the robust performance of the system for practical disturbances that might excite the boost converter nonlinearity leading to instability as will be seen in Section 3-5-2.

Beside bilinear dynamic nature of boost converter, the duty-cycle (control) saturation between 0 and 1 is also considered as a source of nonlinearity in [20, 22, 23]. This reason motivated authors in [22, 23] to include control saturation in the analysis and in the designed control law. However, as will be shown in this thesis the more critical type of nonlinearity in a boost converter is caused by the parasitic parameters of the boost converter which leads to instability under certain operating conditions rather than due to control saturation. This problem was introduced as a power balance problem in the low-input voltage, low-power context in [24] and shown to lead to a voltage collapse at the

output of the boost converter. An approximate quadratic power balance equation was used to calculate the collapse point in an iterative manner in [24]. The equation is solved for input current iteratively using different values of line voltage until the roots become complex indicating non-existence of solution for a certain value of line voltage. This line voltage defines the voltage collapse condition for the boost converter.

The terms "global stability", "large signal stability" and "large disturbance" have been used in [19, 20, 21, 22, 23]. However, it is impossible to guarantee global stability for a boost converter with perfectly regulated output voltage. As will be shown in this chapter boost converter system stability can be guaranteed only for a limited operating region. The operating region limit is governed by nonlinearity arising from parasitic parameters and load resistance. Based on these limits the "large disturbance" scale can be defined for each boost converter.

Boost converter nonlinearity due to parasitic parameters can cause serious stability problem for input line voltage disturbance, particularly when the line voltage falls and the load current drawn from the converter increases. The boost converter can become unstable for an operating point with a duty cycle between 0 and 1 when subjected to such disturbances. The nonlinearity caused by control effort saturation between 0 and 1 is not as serious as the nonlinearity due to the parasitic parameters. This nonlinearity will be investigated in detail in this chapter and non-iterative formulae will be derived using the bilinear averaged model to calculate the voltage collapse point. Based on the derived formulae, the disturbance and operating limits for any boost converter can be calculated independent of the controller used.

3-2 Illustrative Example:

A boost converter (Figure 1-1) operating in continuous conduction mode is used to investigate the parasitic nonlinearity and to verify the derived formulae with V_i=12V, V_o=24V, r_L=0.33Ω, r_{DS}=0.1Ω, r_C= 0.1Ω, r_D=0.1Ω, L=220μH, C=220μF, and switching frequency of 50 kHz. Different values for load resistance are used throughout this analysis to show the crucial effect of load on the boost converter operating and disturbance limits.

A robust controller consisting of PI and lead compensator along with feedforward gain on line voltage change, has been designed following the design guidelines in Section 2-3, to guarantee robustness against a wide range of load variations and line voltage changes. This controller is given by:

$$K = \left[\frac{20370\,(s + 2370)(s + 1816)}{s(s + 1 \times 10^{5})(s + 4.74 \times 10^{4})} \quad 0.042 \right] \tag{3-1}$$

This controller ensures gain and phase margins of 32.8 dB and 108°, respectively, for R_{load}=44 Ω. The closed loop performance of the controller and the boost converter is examined for a line voltage disturbance of -6V (50%) and a load disturbance of 63% applied as an R_{load} step change of -17Ω .Simulation is done using the boost converter PWM switched nonlinear circuit model using S-Functions in MATLAB-Simulink environment. In Figure 3-1, a disturbance of -6V is applied at t=0.03s and +6V at t=0.05s. In Figure 3-2, a load disturbance of -17 Ω is applied at t=0.03s and +17 Ω at t=0.05s. The good large disturbance rejection by the controller in terms of overshoot and settling time is evident in these Figures.

However, to examine the effect of both load resistance and line voltage change, a load disturbance of -17Ω is applied at t=0.02s followed by a line voltage disturbance of -5.7 V is applied at t=0.035s in Figure 3-3. The boost converter is now unstable, even though the open-loop system of controller and the linearized boost converter model for a load of 27Ω and line input voltage of 6.3V indicates stablility with gain and phase margins of 10.3dB and 33.1° respectively. The linear model cannot predict the voltage collapse!

A closer look at Figure 3-3 illustrates that the system is trying to recover but at some point it starts to collapse and the duty-cycle reaches 1 eventually. The point at which the duty cycle reaches 1 and stays at 1 is evident in Figure 3-3 at t=0.0428s where the trace starts to have no fuzziness on it. The collapse thus started before the duty ratio reached 1. This motivates the investigation into the static characteristics of the boost converter.

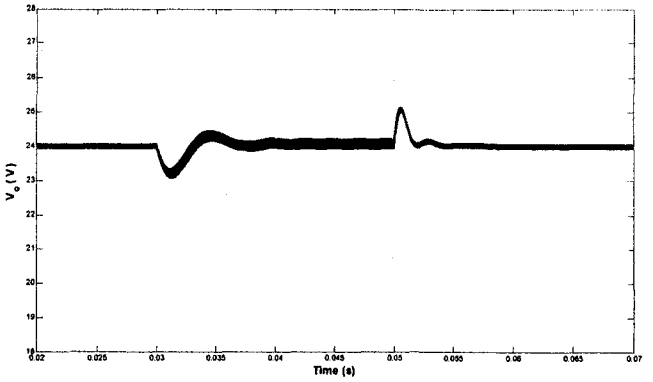


Figure 3-1: Output voltage performance for line disturbance, ±6V

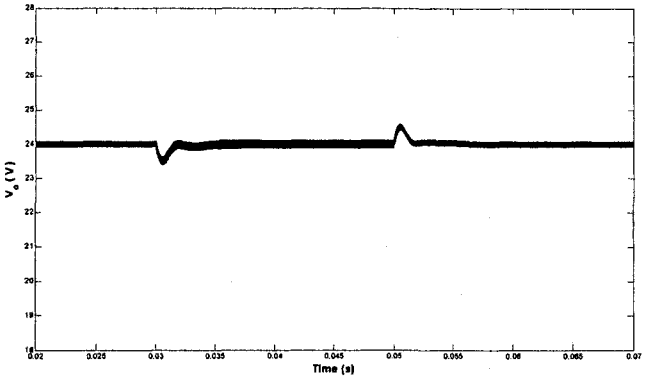


Figure 3-2: Output voltage performance for load disturbance, ±17Ω

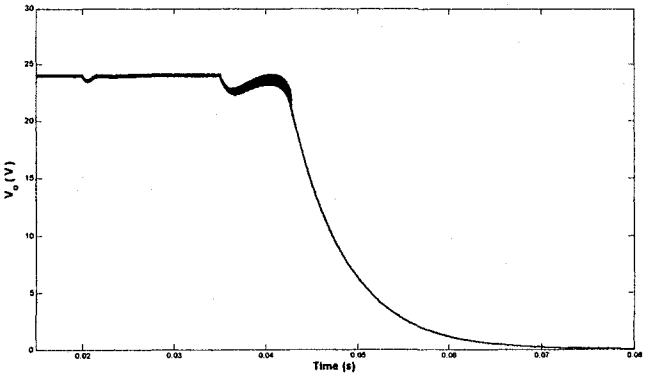


Figure 3-3: Output voltage performance for load disturbance and input voltage disturbance leading to voltage collapse

3-3 Static Characteristics Considering Parasitic Parameters

The static characteristic of the boost converter in the presence of parasitic parameters is derived in this section using the bilinear averaged model. The steady-state static characteristics of the boost converter are described by equations (1-18). These equations, with D as the steady-state duty-cycle and x_{1o} and x_{2o}, the steady-state inductor current, and capacitor voltage, respectively, are given by:

$$\left(-\left(\frac{r_L+r_{DS}}{L}\right)\cdot D-\left(\frac{r_L+r_D}{L}+\frac{r_C\cdot R_{load}}{L(r_C+R_{load})}\right)\cdot(1-D)\right)x_{1o}-\frac{R_{load}}{L(r_C+R_{load})}(1-D)\cdot x_{2o}+\frac{V_i}{L}=0 \tag{3-2}$$

$$\frac{R_{load}}{C(r_C+R_{load})}\cdot(1-D)\cdot x_{1o}-\frac{1}{C(r_C+R_{load})}\cdot x_{2o}=0 \tag{3-3}$$

$$\frac{r_C\cdot R_{load}}{(r_C+R_{load})}\cdot(1-D)\cdot x_{1o}+\frac{R_{load}}{r_C+R_{load}}\cdot x_{2o}=V_o \tag{3-4}$$

In the following, these equations are solved analytically:

From (3-3):

$$x_{2o}=R_{load}(1-D)\cdot x_{1o} \tag{3-5}$$

Substituting (3-5) in (3-2) and solving for x_{1o} :

$$x_{1o}=\frac{V_i}{(r_L+r_{DS})D+(r_L+r_D+\frac{r_C R_{load}}{r_C+R_{load}})(1-D)+\frac{R_{load}^2(1-D)^2}{(r_C+R_{load})}} \tag{3-6}$$

Substituting (3-6) in (3-5):

$$x_{2o}=\frac{R_{load}(1-D)V_i}{(r_L+r_{DS})D+(r_L+r_D+\frac{r_C R_{load}}{r_C+R_{load}})(1-D)+\frac{R_{load}^2(1-D)^2}{(r_C+R_{load})}} \tag{3-7}$$

Finally, Substituting (3-6) and (3-7) in (3-4):

$$\frac{V_o}{V_i} = \frac{\frac{r_C \cdot R_{load}}{(r_C + R_{load})} \cdot (1-D) + \frac{R_{load}^2}{r_C + R_{load}} \cdot (1-D)}{(r_L + r_{DS})D + (r_L + r_D + \frac{r_C R_{load}}{r_C + R_{load}})(1-D) + \frac{R_{load}^2 (1-D)^2}{(r_C + R_{load})}} \tag{3-8}$$

Let $\frac{V_o}{V_i} = \Gamma(D, R_{load})$. Rearranging terms in (3-8), (3-9) is obtained:

$$\Gamma(D, R_{load}) = \frac{R_{load} \cdot (1-D)}{(r_L + r_{DS})D + (r_L + r_D + \frac{r_C R_{load}}{r_C + R_{load}})(1-D) + \frac{R_{load}^2 (1-D)^2}{(r_C + R_{load})}} \tag{3-9}$$

$\Gamma(D, R_{load})$ is the averaged boosting gain as a function of duty cycle and load resistance. Figure 3-4 shows $\Gamma(D, R_{load})$ for the boost converter in the illustrative example for three different values of load resistance. Also, the operating points for R_{load}=27 Ω before the input voltage disturbance and after -5.7V input disturbance are shown in Figure 3-4. This illustrates the reason behind the instability occurring in Figure 3-3. After the line voltage disturbance occurs the controller tries to recover by increasing the duty cycle and the system starts to recover but at some point, the small overshoot of the duty cycle beyond the peak of $\Gamma(D, R_{load})$ decreases the output voltage. This, output voltage decrease forces the controller to increase the control effort trying to reduce the voltage error. This in turn decreases the output voltage as can be seen from Figure 3-4 leading to the voltage collapse and the controller continues to increase the duty-cycle to saturate at 1.

It is obvious that any operating point beyond the peak of $\Gamma(D, R_{load})$ for any R_{load} is a statically unstable operating point. On the other hand, even if the operating point is to the left of this limit (statically stable), due to transient controller response, the voltage can still collapse and such a voltage collapse is a dynamic collapse because it caused by the dynamics of the system in the presence of the parasitic parameters even if the system is small-signal stable at such an operating point. Dynamic collapse should be taken into account when designing the controller. Slower controls can avoid this collapse. However, a better solution as will be seen later is to limit the duty-cycle below the peak in Figure 3-4.

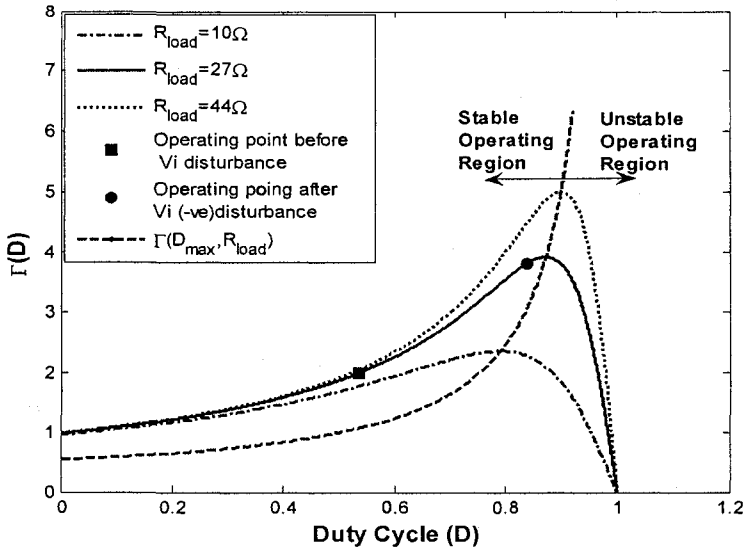


Figure 3-4: Static characteristic of the boost converter (Illustrative Example)

The limited boosting ability of the converter due to parasitic parameters causes a limited range of operating points for the converter. Static voltage collapse is caused if the operating point is beyond the peak of the curves in Figure 3-4, by the parasitic parameters inducing the nonlinearity in the static characteristics of the boost system as shown in Figure 3-4. This collapse can not be avoided by control design.

Assuming that $\Gamma_{max}= \Gamma(D_{max}, R_{load})$ is the maximum averaged boosting gain of the converter for a given load resistance, Static collapse will occur when:

$$v_i < \frac{V_o}{\Gamma_{max}} \tag{3-10}$$

Where V_o is the desired regulated output voltage, v_i is the perturbed line voltage. In this case, the controller continues to increase the duty cycle (control effort) until it passes D_{max} point. Passing D_{max}, the boost system starts collapsing.

The corresponding D_{max} is an important parameter because it defines the stable range of the duty cycle (which is strictly less than 1 in the presence of parasitic parameters). D_{max} and ($v_i = V_o / \Gamma_{max}$) determine the voltage collapse operating point. Γ_{max}

and $D_{\max}$ can be found by partial differentiation of $\Gamma(D, R_{load})$ with respect to D and equating it to zero for $D = D_{\max}$ as follows:

$$\left.\frac{\partial\Gamma(D,R_{load})}{\partial D}\right|_{D=D_{\max}} = -(r_L + r_{DS})D_{\max} - (r_L + r_D + \frac{r_C R_{load}}{r_C + R_{load}})(1 - D_{\max}) - \frac{R_{load}^2}{r_C + R_{load}}(1 - D_{\max})^2 - (1 - D_{\max})(r_{DS} - r_D) + \frac{r_C R_{load}}{r_C + R_{load}}(1 - D_{\max}) + \frac{2R_{load}^2(1 - D_{\max})^2}{r_C + R_{load}} = 0 \quad (3\text{-}11)$$

Rearranging terms in (3-11) and solving for $D_{\max}$:

$$D_{\max} = 1 - \sqrt{\frac{(r_L + r_{DS})(r_C + R_{load})}{R_{load}^2}} \quad (3\text{-}12)$$

Note that r_D does not play a role in determining $D_{\max}$ but it is involved in determining Γ and $\Gamma_{\max}$.

For $D_{\max} \geq 0$:

$$R_{load}^2 - (r_L + r_{DS})R_{load} - r_C(r_L + r_{DS}) \geq 0 \quad (3\text{-}13)$$

Hence, the minimum value for R_{load} is given by:

$$R_{load} \geq 0.5(r_L + r_{DS}) + 0.5\sqrt{(r_L + r_{DS})^2 + 4r_C(r_L + r_{DS})} \quad (3\text{-}14)$$

For $r_C << R_{load}$, then:

$$D_{\max} = 1 - \sqrt{\frac{(r_L + r_{DS})}{R_{load}}} \quad (3\text{-}15)$$

It is clear that for $r_C << R_{load}$, the steady state duty cycle at which the boost converter exhibits the maximum averaged gain depends only on the ratio of inductor resistance plus MOSFET resistance to load resistance. And, the condition in (3-13) will be given by:

$$R_{load} \geq (r_L + r_{DS}) \quad (3\text{-}16)$$

For R_{load} equal to the minimum value of

$$R_{load(\min)} = 0.5(r_L + r_{DS}) + 0.5\sqrt{(r_L + r_{DS})^2 + 4r_C(r_L + r_{DS})} \qquad (3\text{-}17)$$

the stable range of the boost converter will be zero (D_{max} =0) i.e., the boost converter is always operating in the unstable region for loads less than or equal this resistance value. $\Gamma(D_{max}, R_{load})$ is plotted in Figure 3-4 as a boundary between stable and unstable regions, for $R_{load} \geq R_{load(\min)}$. Figure 3-5 illustrates the stable duty cycle limit D_{max} as a function of $1/R_{load}$ for different r_C values. It can be seen that D_{max} decreases rapidly with increasing load current.

The stability regions will be studied for more practical load resistances for the illustrative example of Section (3-2) in terms of load current for nominal V_i and V_o of 12V and 24V, respectively. Figure 3-6 shows the maximum boosting gain calculated using ((3-9) and (3-12)) as a function of load current for the boost converter of Section (3-2). It is seen that the boost gain reduces rapidly with increasing load. Decreasing boosting gain ($\Gamma(D, R_{load})$) with increasing load requires increasing V_i to guarantee the desired output voltage and avoid the voltage collapse. This is depicted in Figure 3-7 which shows minimum V_i (V_o / Γ_{max}) needed to maintain the nominal output voltage without collapse. Alternatively in Figure 3-8, the sensitivity of the boost converter system for negative line voltage disturbance from the nominal V_i =12V is shown. For any negative disturbance beyond the limits shown in Figure 3-8, no normal controller with regulated output can avoid static collapse. It can be seen that the load limit for this boost converter is 3.35A. At this load limit, as can be noticed from Figure 3-8, the negative V_i disturbance limit is 0V and the boost converter system can not handle any negative line disturbance or any positive load disturbance. For this load current the boost converter should be redesigned using components with lower parasitic values. However, for loads between 2 and 3.35A the boost system is very sensitive even for small disturbances and the converter redesign should be considered. For example, for I_o=2.4A, the system will collapse for any negative line voltage disturbance beyond -1.86V regardless of the controller used (but it can handle a positive line input disturbance of 6V, for example, quite well). Hence, the term "large disturbance" in a boost converter is a relative term and depends on the polarity of the disturbance and the load current being drawn, a point often missed in the simulations/experiments in the literature cited earlier.

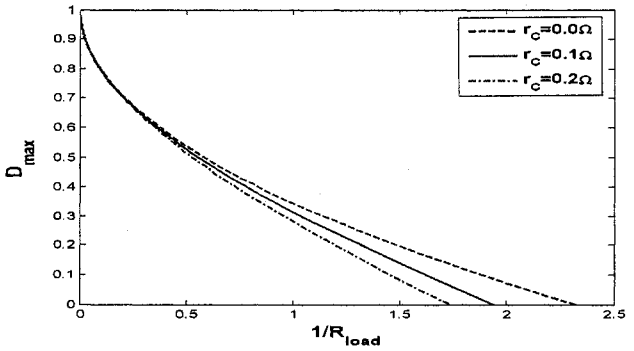


Figure 3-5: Stable duty cycle limit D_{max} versus $1/R_{load}$

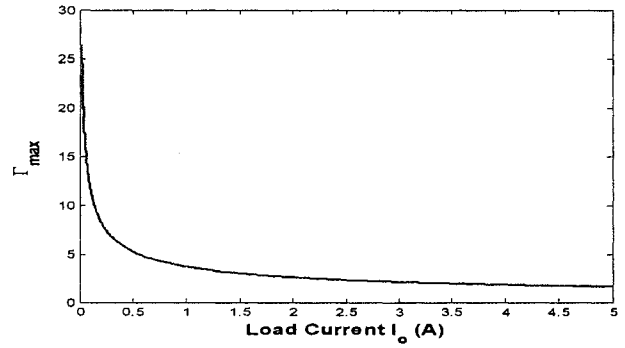


Figure 3-6: Maximum boosting gain as a function of load current

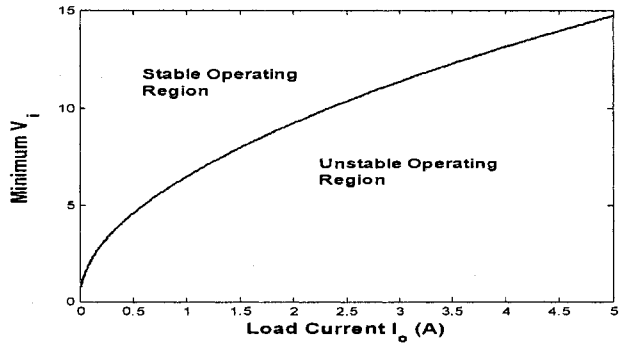


Figure 3-7: Minimum line input voltage required to avoid static output voltage collapse

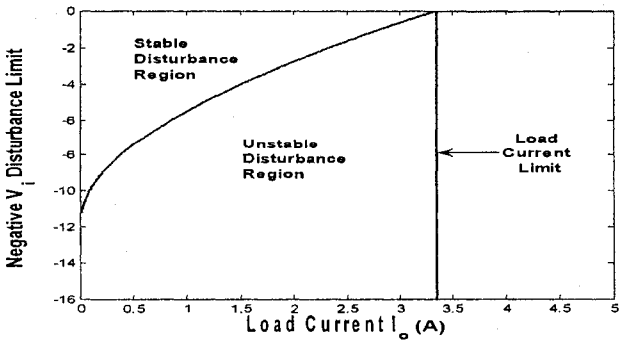


Figure 3-8: Negative V_i disturbance limit and load current limit

Therefore, not withstanding what has been stated in the large signal stability literature (Section 3-1), it is impossible to guarantee global stability for boost converter control system with regulated output.

The issues clarified herein should be taken into account in the design phase of boost converters because the parasitic parameters induced nonlinearity and the voltage collapse operating point depend on the ratio of the load resistance to the parasitic parameters values not on the load resistance alone. Even though boost parameters with low parasitic parameter values can be selected for high power converters, the load resistance value is also small compared to the parasitic parameter values and therefore the problem of voltage collapse may be met in this case too.

3-4 Duty Cycle Saturation

As discussed in last section the stable operating range of duty cycle is limited by D_{max} <1. Hence, to avoid voltage collapse, the duty cycle should be saturated at D_{max} not at 1. Anti-windup integrator to avoid integrator wind-up must be used. A saturation element will not cause a dynamic problem (limit cycles) if the system is linearly stable. This can be shown by using the describing function (N) of the saturation element. Even though due to the harmonics, the traditional describing function using only fundamental component and even the bias + sinusoid describing function [25] can not predict the amplitude and frequency of limit cycles accurately, these traditional describing functions N can always predict the presence of limit cycles. Since the gain of saturating element in the linear region is always 1, and -1/N always starts from -1 in all such cases, hence, if the system is linearly stable then there is no limit cycle.

As an example, for R_{load}=10Ω , D_{max} =0.7916, the negative disturbance limit is -1.8583V. Using saturation element at $D_{sat} = D_{max}$ will prevent any possibility of dynamic collapse completely and cause steady error instead of static collapse for disturbances beyond -1.8583 V. Steady state voltage error is shown in Figure (3-9) for different values of input voltage disturbances beyond the limit with the controller given earlier in (3-1).

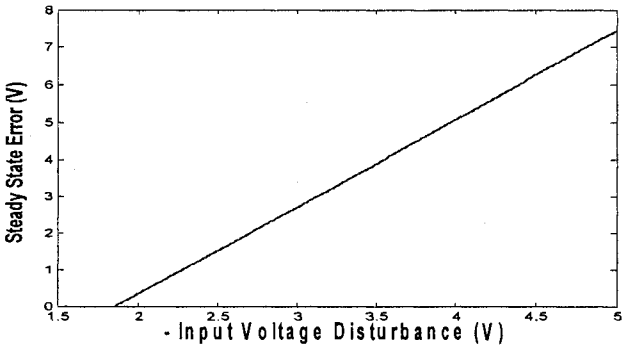


Figure 3-9: Steady state error with D_{sat}=$D_{\max}$=0.7916 (R_{load}=10Ω)

3-5 Simulation Results

A PWM switched nonlinear circuit model is used to verify the derived formulae, saturation and disturbance limits by simulations. In the illustrative example of Section (3-2), dynamic collapse occurred for R_{load} = 27 Ω and for input disturbance of -5.7 V. For R_{load}=27Ω, we have $D_{\max}$ =0.8736 and the line disturbance limit is -5.8651V. Using saturation limit at D_{sat} = $D_{\max}$ =0.8736 prevents dynamic collapse as shown in Figure 3-10. In Figure 3-10, a voltage disturbance of -5.7V is applied at t=0.02s and a disturbance of 6V is applied at t=0.055s. To verify the derived formulae and examine the disturbance limits, shown in Figure (3-8), R_{load}=10Ω (I_o=2.4A, $D_{\max}$ =0.7916, $\Gamma_{\max}$=2.4238) will be used. For this case the disturbance limit is -1.8583 V. First, the boost system will be examined for an input voltage disturbance of -1.85V which lies in the stable disturbance region of Figure 3-8 and very close to the limit, for which the linearized model and controller predict a gain margin of 6.44 dB and phase margin of 58.7°. The negative input voltage disturbance is applied at t=0.03s in Figure 3-11 and the system shows stable performance and no collapse happens. A line disturbance of -2V which lies in the unstable disturbance region of Figure 3-8 and very close to the limit is applied in Figure 3-12 at t=0.03s. Obviously, static collapse occurs when controller is not correctly saturated and no controller can stabilize the system for this small disturbance. Using saturation element at D_{sat} = $D_{\max}$ =0.7916 prevents static collapse with small steady state error for this case as shown in Figure 3-13. The steady state error increases with increasing input voltage disturbance beyond the limit as shown in Figure 3-9. Both Figure 3-9 and Figure 3-8 have been verified by simulation using the switched nonlinear model.

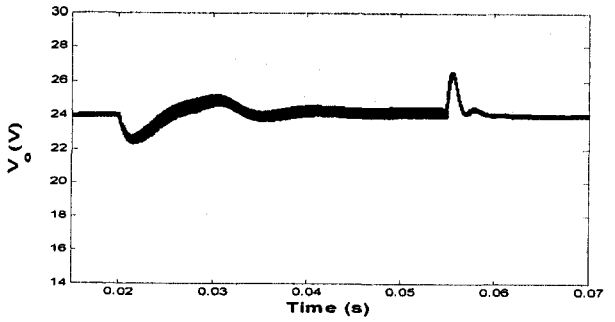


Figure 3-10: Output voltage response (avoiding dynamic collapse of Figure 3-4, D_{sat} =0.8736)

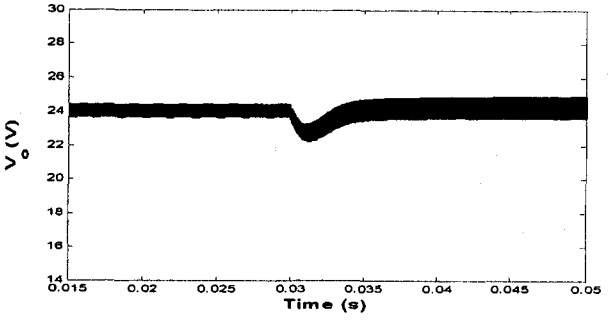


Figure 3-11: Output voltage response to input voltage disturbance of -1.85V, $D < D_{max}$

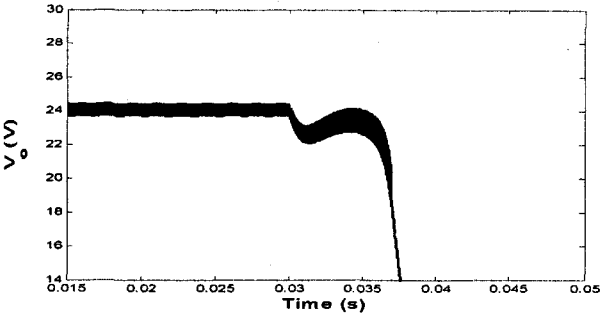


Figure 3-12: Output voltage response to input voltage disturbance of -2V, $D > D_{max}$

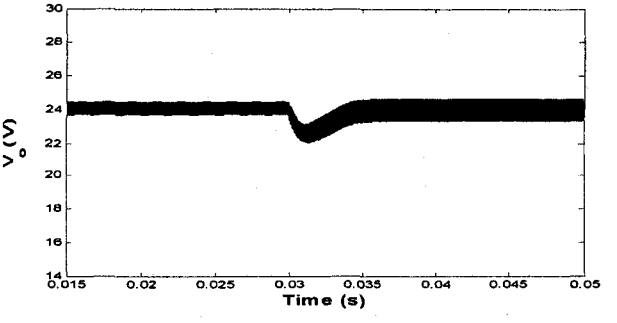


Figure 3-13: Output voltage response to input voltage disturbance of -2V, ($D > D_{max}$ with $D_{sat} = D_{max}$)

3-6 Passivity Based Integral Control Vs. the Proposed Controller

In this section the performance of the passivity based integral control designed in [23] is compared with that of the proposed linear controller designed following the design guidelines from Chapter 2 of this thesis. It is claimed in [23] that the designed passivity based integral control guarantees global stability.

The control law that guarantees the passivity of the closed loop system is given in [23] by:

$$d = -\phi(y).y \tag{3-18}$$

Where $y = v_e i - i_e v + k(V_g + d_e' v)(d_e' z + Li)$

d : duty cycle (duty cycle deviation from the nominal duty cycle)

d_e: nominal steady state duty cycle,

$d_e' = 1 - d_e$,

v_e : nominal steady state output voltage,

i_e : nominal steady state inductor current,

v : output voltage incremental deviation from the nominal output voltage,

i : inductor current deviation from the nominal,

V_g: nominal input voltage,

k : constant value,

$\frac{dz}{dt} = v$

and

$$\phi(y) = \begin{cases} \phi_{\max} & -\frac{(1-d_e)}{\phi_{\max}} \le y \le \frac{d_e}{\phi_{\max}} \\ \frac{d_e}{y} & y > \frac{d_e}{\phi_{\max}} \\ -\frac{(1-d_e)}{y} & y < -\frac{(1-d_e)}{\phi_{\max}} \end{cases} \tag{3-19}$$

The function ϕ is used to incorporate the nonlinearity effect caused by the duty cycle saturation between 0 and 1 (due to PWM) by saturating the duty cycle deviation (d) from the nominal within [$-d_e$, $1-d_e$]. ϕ_{max} was chosen as 0.003 using the root locus of the linearized loop gain of the controlled system with k =500 in [23].

The boost converter parameters used in [23] are V_i=V_g=12 V, V_o= v_e=24 V, L=200 μH, C=200 μF, r_L=0.22 Ω, f_s=50 KHz. Parasitic parameters are not included in the analysis and the design of the controller parameters in [23] and only r_L is used in the simulation.

The proposed controller has been designed using the design guidelines from Chapter 2 of this thesis with the following parameters:

K_p=2, K_i=2000, T_p=0, 1/T=1788.854 rad/sec, α=0.05, K_c=0.1, K_v=0.042

Note that T_p= 0 because the boost converter with r_C =0 has a low-pass filter characteristic and, hence, there is no need to include extra low-pass filter in the controller. Figure 3-14 shows the frequency response of the controlled system loop gain with a gain margin and phase margin of 16 dB and 80.4°, respectively. The linear controller is given by:

$$K = \left[\frac{0.2(s+1789)(s+1000)}{s(s+3.578\times10^4)} \quad 0.042 \right] \tag{3-20}$$

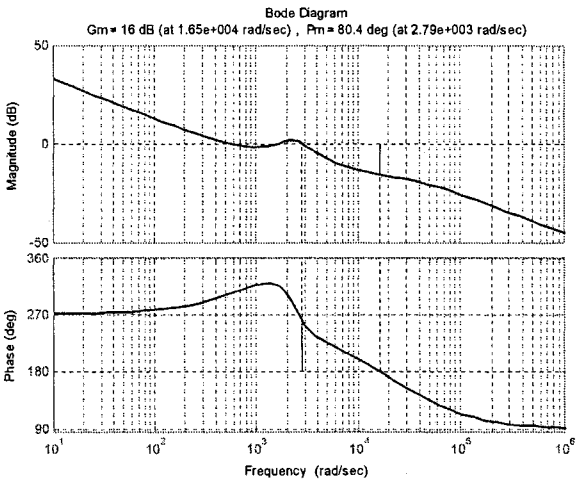


Figure 3-14: Frequency of the designed controlled system loop gain

Passivity based integral control has some drawbacks, comparing to the proposed linear controller, which can be summarized as follows:

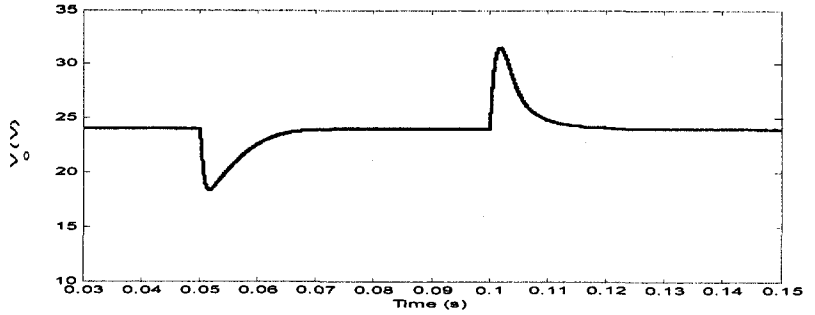
1- A nonlinear controller with analog multiplication comparing to the simple linear proposed controller.
2- It requires a current measurement to obtain the inductor current deviation
3- Slower dynamic response comparing to the response of the designed linear controller as will be seen in the next subsection.

3-6-1 Simulation Results:

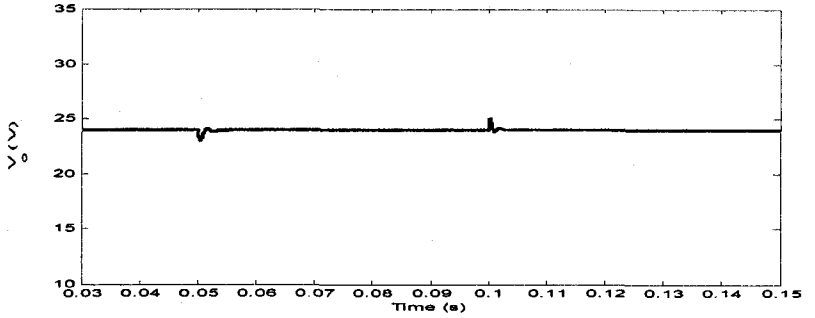
The performance of the passivity based integral control and the proposed controller will be judged based on the same disturbances applied in [23]. A -5 V line voltage disturbance, which is considered as a large disturbance, is used in [23] to examine the performance of the controlled system. However, this disturbance is applied as a V_i transition from 17 V to 12 V and then from 12 V to 17 V which does not reveal the performance of the system, during the nominal operation (V_i=12V), for practical disturbances that might excite the boost converter nonlinearity leading to unstable behavior. The load disturbance used in [23] is equivalent to -2Ω R_{load} step from 10 Ω to 8 Ω and then a disturbance of +2 Ω to return to R_{load} of 10 Ω which is the nominal.

Figure 3-15 illustrates the output voltage performance of the both controllers for a line voltage disturbance equivalent to a V_i transition from 17 V to 12 V at t=0.05s, and from 12 V to 17 V at t=0.1s. Figure 3-16 presents the output voltage performance of the controllers for an R_{load} disturbance from 10 Ω to 8 Ω at t=0.05s and then from 8 Ω to 10 Ω at t=0.1s.

As can be seen from Figure 3-15 and Figure 3-16 the proposed simple linear controller illustrates a superior performance to that of the passivity based integral control using only voltage measurements.

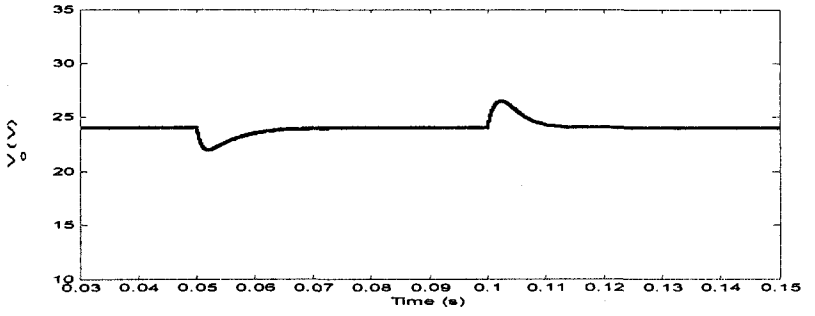


(a) Passivity Based Controller

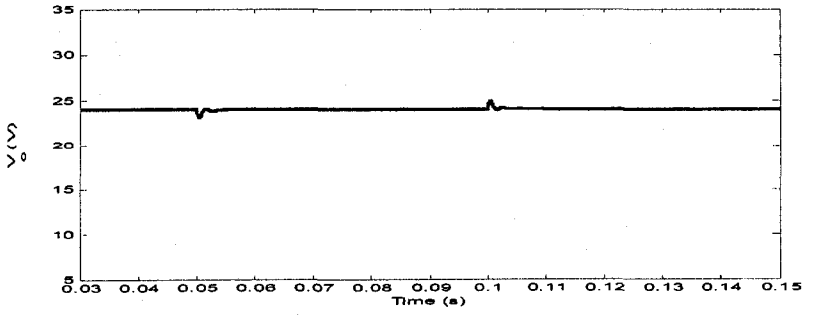


(b) Proposed Linear Controller

Figure 3-15: Output voltage performance for line voltage disturbances



(a) Passivity Based Controller



(b) Proposed Linear Controller

Figure 3-16: Output voltage performance for load disturbances

3-6-2 Global Stability:

As stated before the passivity based integral control designed in [23] is claimed to be globally stable; however, it is concluded in Section 3-3 that it is impossible to guarantee global stability for boost converter control with regulated output. Also, the term "large disturbance" is a relative term which depends on the polarity of the disturbance, parasitic parameters, load resistance and, also, on the operating point at which the disturbance is applied which is logically assumed to be the nominal in Section 3-3.

Applying the new formulae derived in Section 3-3 on the boost converter parameters used in [23] with r_L=0.22Ω and R_{load}=10Ω, it is found that:

Γ_{max} =3.371	(Maximum boosting gain)
D_{max} = 0.8517	(Maximum stable duty cycle)
$V_{i(min)}$=7.12 V	(Minimum V_i required to avoid static collapse)
-ve V_{dis}= -4.88V	(Negative disturbance limit)

Hence, static voltage collapse will occur for a -5V line voltage disturbance when the boost converter operating at the nominal input operating point of V_i=12V has its line voltage changed to 7V. Figure 3-17 shows the voltage collapse of the boost converter system controlled by the passivity based controller. Figure 3-18 illustrates the performance of the proposed controller and the passivity based controller after incorporating a saturation element with $D_{sat}=D_{max}$.

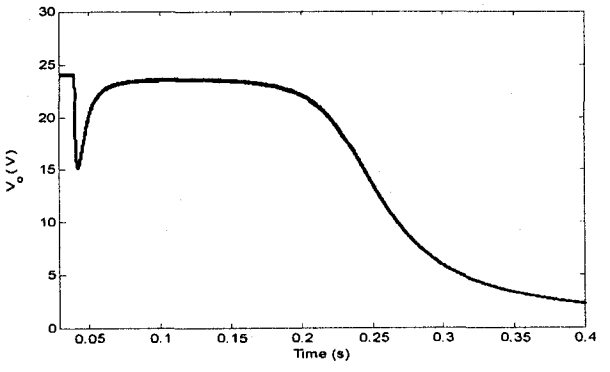
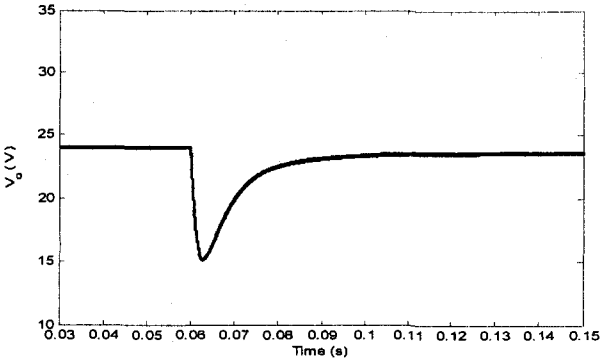
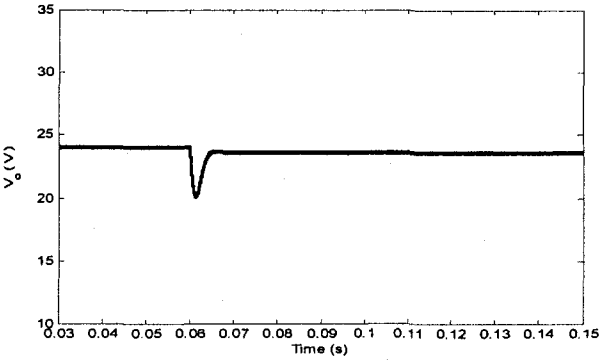


Figure 3-17: V_o performance for -5 line voltage disturbance (Static voltage collapse)



(a) Passivity Based Controller



(b) Proposed Linear Controller

Figure 3-18: V_o performance with D_{sat}=$D_{\max}$ (avoiding static collapse)

Moreover, for practical (non-ideal) MOSFET (IRFP250) and DIODE (MBR 1660) used in the experimental setup of [23] with r_{DS} and r_D of 0.085Ω and about 0.06Ω, respectively, $D_{\max}$ is 0.8254 and the system will collapse for any negative line voltage change beyond - 3.6772V from the nominal 12V.

Chapter 4

Experimental Setup and Results

The performance of the controller designed using the design guidelines in Chapter 2 and the static characteristics of the boost converter derived in Chapter 3 are verified experimentally in this chapter. In Section 4-1 the boost converter system experimental setup and the experimental static characteristics will be investigated. Controller design and implementation are discussed in Section 4-2. The experimental results illustrating the performance of the control system for load disturbances will be presented in Section 4-3. In Section 4-4 the experimental circuit used to apply the line voltage disturbances along with the experimental response of the controlled system is presented. System performance for the worst case disturbances is illustrated in Section 4-5.

4-1 Boost Converter Experimental Setup and Static Characteristics

Figure 4-1 shows the synchronous boost converter used in the experimental setup. This boost converter operates on a nominal line voltage of 12V with a nominal output of 24V and switching frequency (f_s) of 50 KHz. The boost converter components used in the experimental setup are as follows:

Inductor (L) (FIT106-6): FIT106-6 is a toroidal inductor which is specifically designed to minimize transients with a minimum inductance of 70.05 μH at no bias and 35.3 μH when biased at the rated DC current of 9.7 A with $r_{L(DC)}$ =0.024 Ω according to its manufacturer. The inductance measured in the laboratory, using a Z-meter, was 74 μH at no bias. Three inductors connected in series is used in the experimental setup producing an inductance of 222 μH with $r_{L(DC)}$ =0.072 Ω. The total inductor equivalent resistor r_L,

however, should include the core loss and the ac resistance. "Core loss measurements are difficult because they involve the estimation of the hysteresis loop areas. Many inductor manufacturers do not supply this data; however, curves are available from ferrite manufacturers, to help estimate the core loss, if the ferrite core type is known [26]". The total inductor equivalent resistance will be calculated using the experimental static characteristic curve matching later in this section. An inductance value of 222 μH is used in the control design and simulation which is practically the maximum possible inductance for the implemented setup.

Capacitor (C) (Panasonic-FM Series): It has a value 220μF, 50V with r_C (ESR) = 0.02Ω.

Diode MUR1520: This diode turns ON during the dead time when both MOSFETs are OFF (about 0.6 μs). In nominal operation S_1 is ON while S_2 OFF or vice versa. However, practically there is a dead time when both S_1 and S_2 are OFF. In this time, rather than depending on the slow substrate diode of the MOSFET, the fast diode MUR1520 turns ON.

MOSFET (IRF450): Power MOSFET with V_{DSS}=100 V, I_D=28 A and $r_{DS(on)}$=0.07Ω.

Load Resistor (R_{load}) (MPS930): 50 Ω (30 W, 1%) low inductance type is used as the nominal load.

Input Capacitor C_{in}: A 2200 μF capacitor used to maintain the line voltage constant and to reduce the dynamic effect of the power supply. This capacitor is used in the experimental setups for static characteristics, load disturbance and worst case disturbances tests. In line voltage disturbance test this capacitor value is dropped to a lower value and is discussed in Section 4-4.

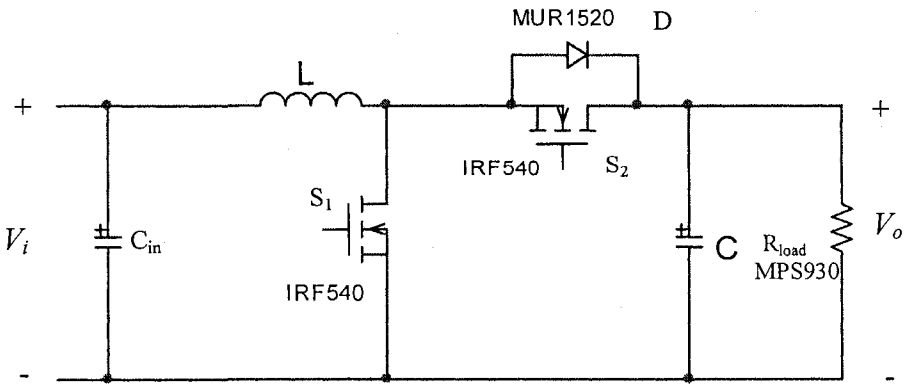


Figure 4-1: Synchronous Boost Converter used in the experimental setup

Detailed experimental setup for boost converter and driver circuits are shown in Appendix-A (Figure A-1).

Open-loop boost converter system was used to measure the static characteristic of the boost converter. This technique is also used to estimate r_L. To avoid high current at the input of the uncontrolled boost converter an extra protection resistor of 1 Ω ($2 \times 0.5\,\Omega$ MPS9100) is added in series with the inductor to limit the input current approximately within the nominal operating range. Also, for the same purpose an input voltage (V_i) of 6V was used in this experiment. The experimental static characteristics of the boost converter are shown in Figure 4-2 for R_{load} of 50 Ω and 25 Ω along with the calculated characteristics. Theoretical averaged boosting gain has been calculated using equation (3-9) with, $r_{DS}=r_{DS1}=0.07\ \Omega$, $r_D=r_{DS2}=0.07\ \Omega$ and $r_C=0.02\ \Omega$. For the case of R_{load}= 50 Ω, r_L= 1.15 Ω shows the best match between the calculated and the experimental data, while r_L= 1.12 Ω results in the best match for R_{load}=25 Ω. Hence, r_L=0.15 Ω for R_{load}= 50 Ω and R_{load}=0.12 Ω for R_{load}=25 Ω. Practically, determining an accurate exact value for r_L is quite hard due to the difficulty of matching an accurately calculated value with measurements done in a noisy environment in the presence of other practical factors like the other temperature dependent components' tolerances and the measurements error. Also, increasing the inductor bias current (at R_{load}=25 Ω instead of R_{load}=50 Ω) decreases the hysteresis loop created over the switching period which in turn reduces the core loss associated with the hysteresis loop resulting in smaller r_L. Also, the determined r_L is a bulk parameter in that all parasitics not modeled explicitly are lumped into this parameter. Hence, the averaged value of r_L=0.135Ω is considered as an estimate of the inductor resistance.

Figure 4-3 shows the final boost converter static characteristics with r_L=0.135 Ω. Using the formulae derived in Section 3-3, the static characteristics for R_{load}= 25 Ω can be summarized as follows:

Γ_{max} = 5.5 (Maximum boosting gain)

D_{max} = 0.9094 (Maximum stable duty cycle)

$V_{i(min)}$ = 4.37V (Minimum Vi required to avoid static collapse)

-ve V_{dis}=- 7.63V (Negative disturbance limit)

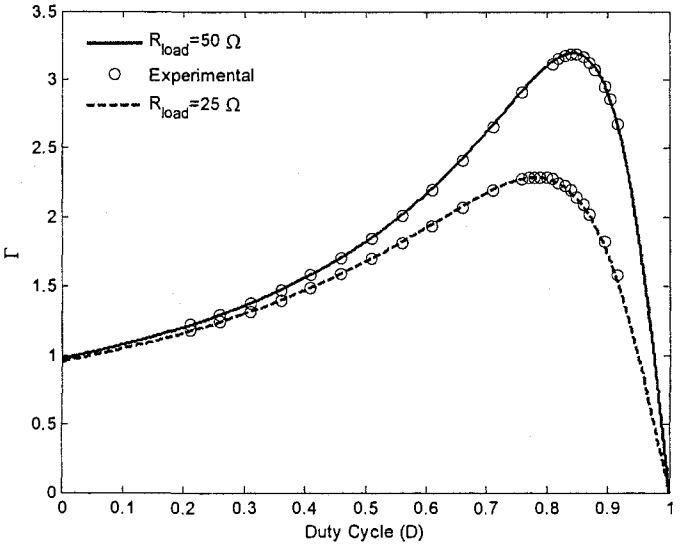


Figure 4-2: Experimentally measured static characteristics vs. the calculated characteristics (with an additional input series resistance of 1 Ω)

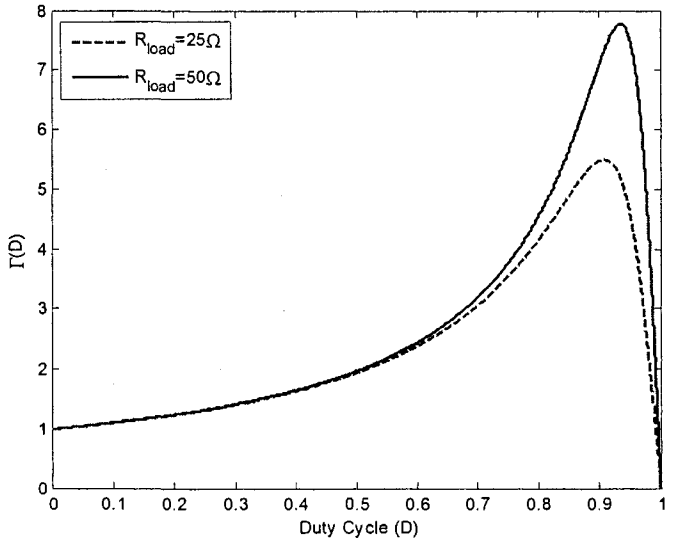


Figure 4-3: Static characteristics with r_L=0.135Ω

It is obvious that the boost converter can statically handle a 100% load disturbance and a 50% line voltage disturbance individually and simultaneously with a nominal operating conditions of V_i=12 V, V_o=24V and R_{load}= 50 Ω. The robust controller design to handle these disturbances is presented in the next section.

4-2 Controller Design and Implementation

A PI plus phase lead compensator controller has been designed according to the guidelines presented in Chapter 2 (Section 2-3-2). The designed controller parameters are as follows:

K_p=4.8, K_i=4800 1/sec , T_p= 7.92×10^{-6} sec, $1/T$= 1245.49 rad/sec, α =0.05, K_c= 0.1, K_v=0.042

This controller guarantees a gain and phase margin of 19.6 dB and 60.6°, respectively. For the worst case stability, with L=222 μH, C=176μF (220-20%), V_i=6V (50% line voltage disturbance) and R_{load}=25Ω (100% load disturbance), this controller ensures a gain and phase margins of 5.12 dB and 29°, respectively.

The detailed controller circuit is illustrated in Appendix-A (Figure A-2). As can be seen from Figure A-2 the controller filter is implemented as a separate unit directly before the PI controller, to gain more flexibility in setting the proportional gain, which results in a good match to the theoretical frequency response of the designed system as illustrated in Figure 4-4. Figure 4-4 shows the frequency response of the loop gain calculated using the implemented controller and that calculated using the theoretical calculated controller with the gain and phase margin of the implemented system.

The lead compensator is implemented as shown in Figure A-2 using R_{17}=82 KΩ, C_4= 0.01 μF, R_{18}=4.1 KΩ and C_5=0.01μF which results in:

$1/T=1/(R_{17}C_4)$=1219.512 rad/sec

$1/\alpha T=1/(R_{18}C_5)$= 24390.244 rad/sec

α= 0.05

$K_c=C_5/C_4$= 1

The lead compensator gain K_c is designed as 0.1 which is achieved inherently by the equivalent gain of the PWM unit (K_{pwm}= 0.1) [27] with a saw-tooth peak to peak

voltage of 10 V. Again, the implemented lead compensator shows a good match between the experimentally implemented controller and the theoretical controller in Figure 4-4. Note that in Figure A-2 the controller is implemented in stages for academic purpose to show the functionality of each stage; however, for industrial applications, the controller filter and scaling gain can be included in one compact PI controller stage.

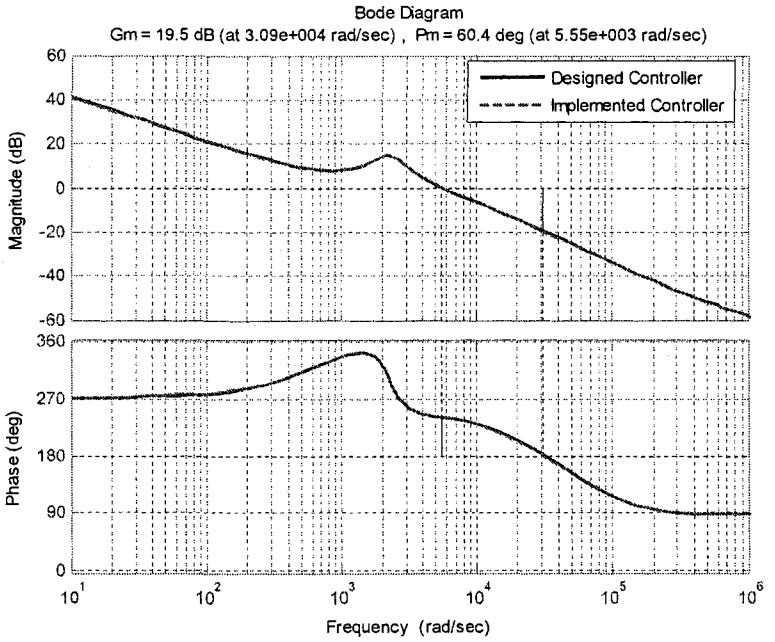


Figure 4-4: Loop gain frequency response using the theoretically designed controller and the experimentally implemented controller

4-3 Load Disturbances Experimental Results:

Figure 4-5 shows the experimental setup used to apply load disturbances. Figure 4-6(a) illustrates the simulated output voltage performance for a 100% load disturbances applied as R_{load} step change from 50Ω to 25 Ω at t=0.03 s and then from 25 Ω to 50 Ω at t=0.055 s. Figure 4-6(b) present the experimental output voltage performance for the same applied disturbances. The amplified filtered negative error voltage measured at the input of the PI controller is shown in Figure 4-7. Figure 4-8 shows the detail of the simulated and the experimental output voltage performance for the negative and the positive load disturbances, individually. Both Figure 4-6 and Figure 4-8 exhibits a good match between the simulation results and the experimental results.

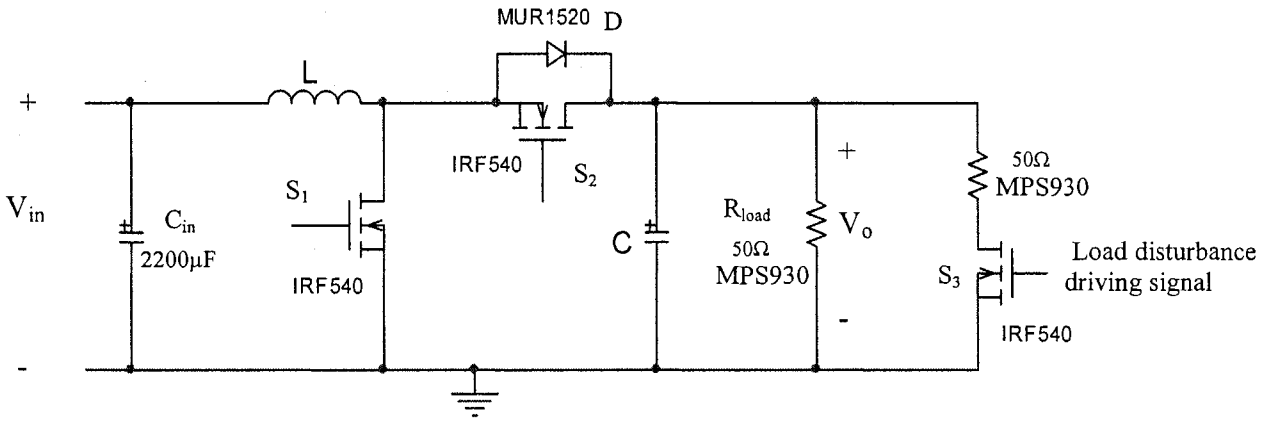
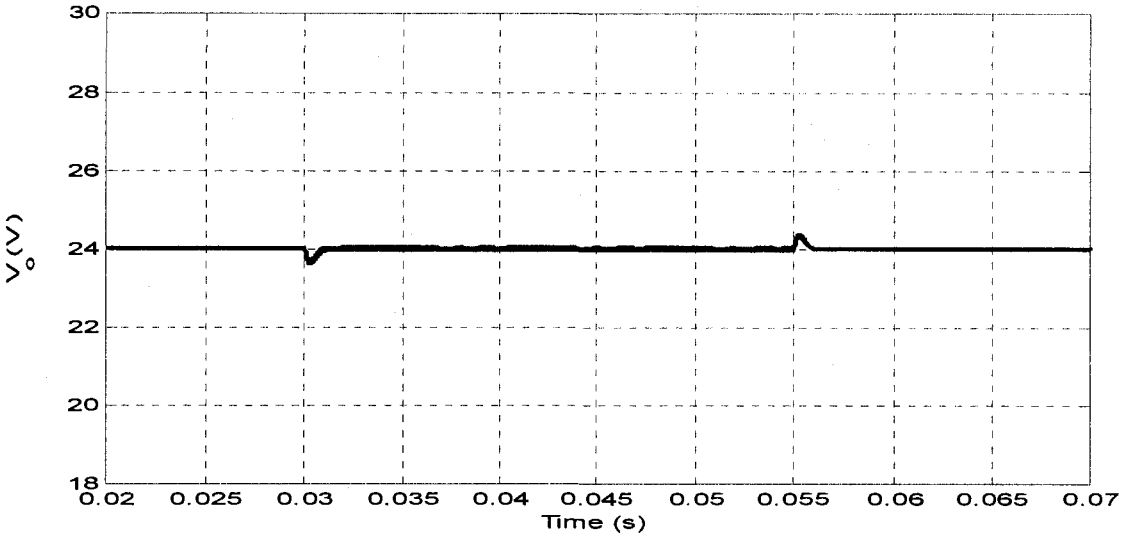
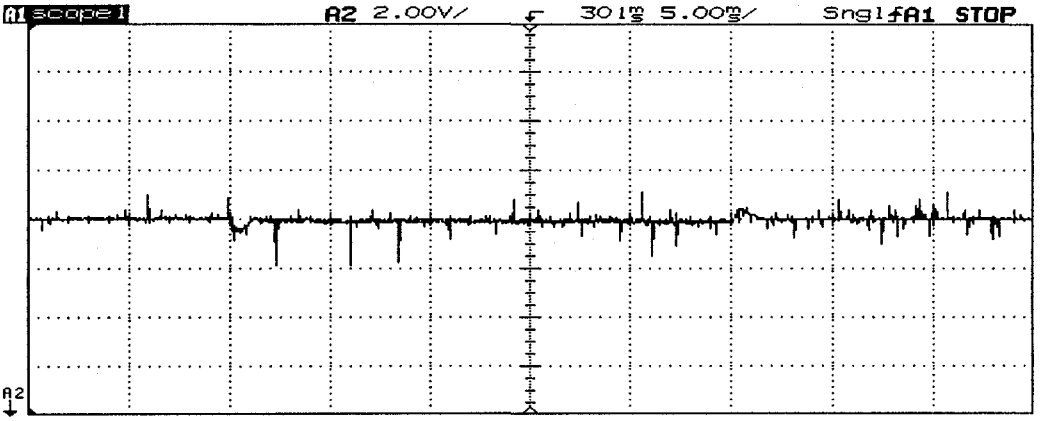


Figure 4-5: Load disturbance experimental setup



(a) Simulated output voltage performance



(b) Experimental output voltage performance

Figure 4-6: Output voltage performance for 100% load disturbances with V_i=12 V

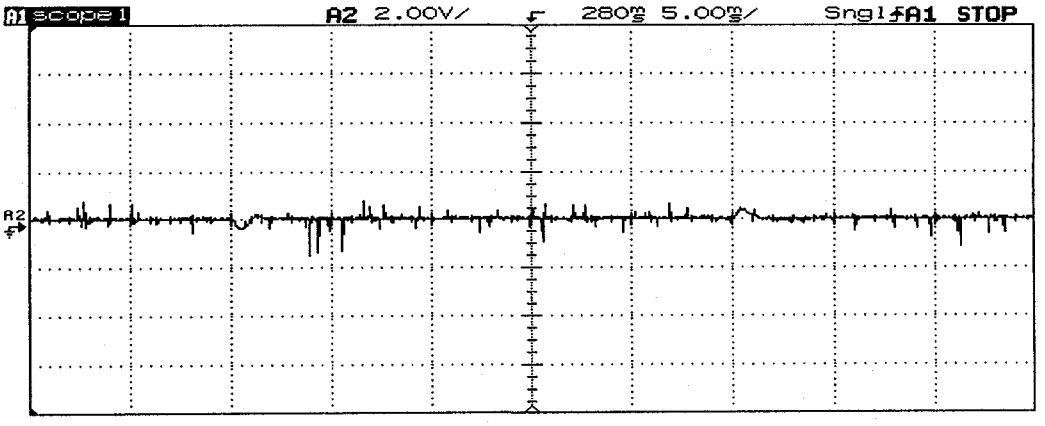
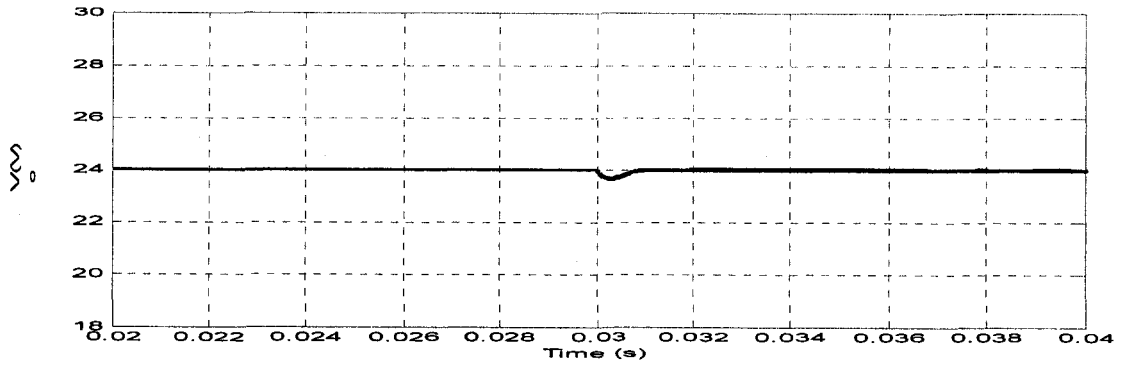
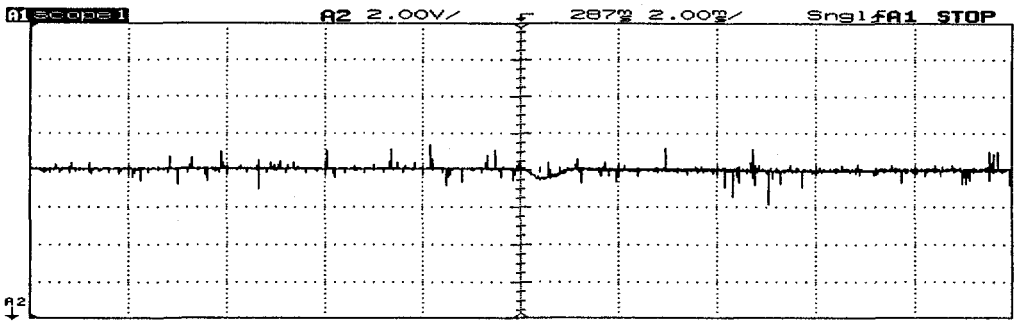


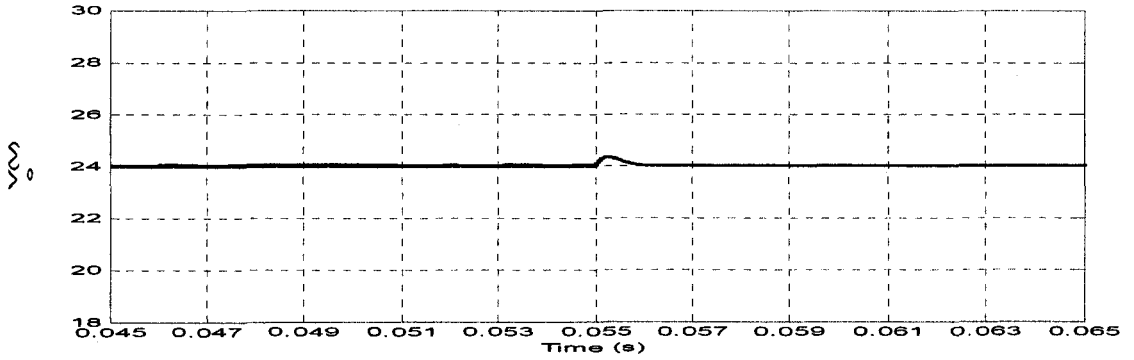
Figure 4-7: Amplified negative error voltage measured at the input of the controller



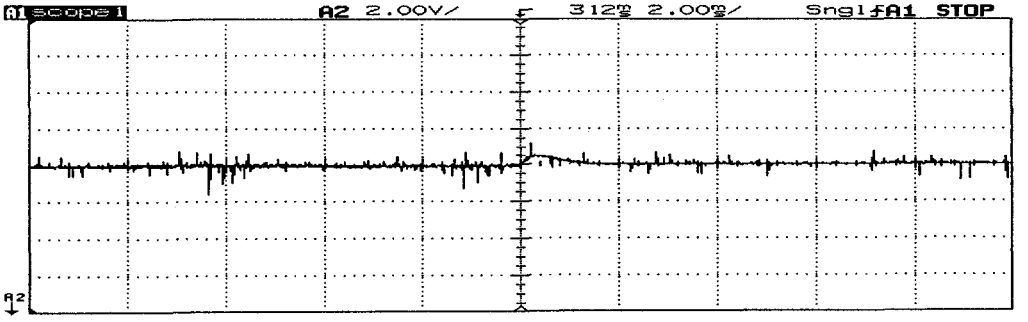
(a) Simulated output performance for positive load disturbance



(b) Experimental output performance for positive load disturbance



(c) Simulated output performance for negative load disturbance



(d) Experimental output response for negative load disturbance

Figure 4-8: Output performance for 100% load disturbances (Magnified)

4-4 Line Voltage Disturbances Experimental Results:

Figure 4-9 shows the experimental setup of the circuit used to apply the line voltage disturbance. When the MOSFET S is turned ON using the isolated driving signal [28], the output voltage will switch to V_{s1} (12) V which turns off the output diode D_s. On the other hand when the MOSFET is turned OFF by the isolated driving signal the diode D_s will turn ON to supply the load current, switching the output voltage from V_{s1} (12V) to V_{s2} – (diode voltage drop). Practically, V_{s2} should be chosen greater than 6V to compensate for the diode voltage drop.

Figure 4-10 illustrate the output voltage V_s of the switching circuit supplying a resistive load (50 Ω) with output voltages V_s of 12V and 6 V.

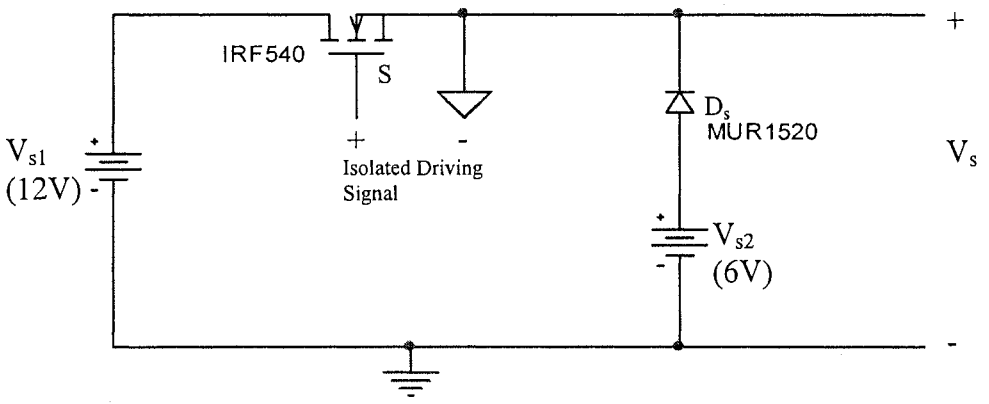


Figure 4-9: Circuit setup used to apply voltage disturbances

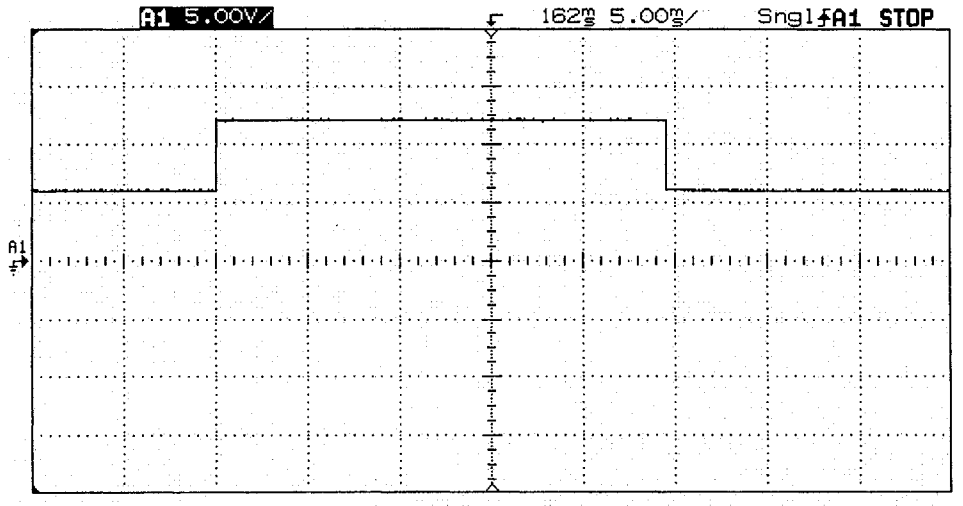


Figure 4-10: Output voltage (V_s) with a low resistive load

However, when this circuit is used to supply the boost converter, the effect of the input capacitor C_{in} of the boost converter will change the output behavior of the designed circuit significantly as illustrated in Figure 4-11. In Figure 4-11 C_{in}=470μF is used instead of C_{in}=2200 μF shown in Figure 4-5. The behavior exhibited in Figure 4-11 can be explained as follows:

Mode 0 **($t=t_0$):** At $t=t_0$ the switch S is turned ON and the C_{in} starts to charge from V_{s2} (6V) to V_{s1} (12V) with a small time constant determined by the $r_{DS(ON)}$ and C_{in} which results in a relatively sharp step in V_s .

Mode 1 **($t_o < t \leq t_1$):** During this mode the switch S is ON and the diode D_s is OFF charging the boost converter input capacitor (C_{in}) to $V_s=V_{s1}$.

Mode 2 **($t_1 \leq t < t_2$):** At $t=t_1$ the switch S is turned OFF and C_{in} starts to discharge, with a time constant determined by the boost converter component values and C_{in}, supplying the current required by the boost converter. During this mode D_s is OFF too because $V_s > V_{s2}$.

Mode 3 **($t_2 \leq t < T$):** By the time $t=t_2$ C_{in} will be discharged to 6 V and diode D_s starts to conduct supplying the boost converter with the required current.

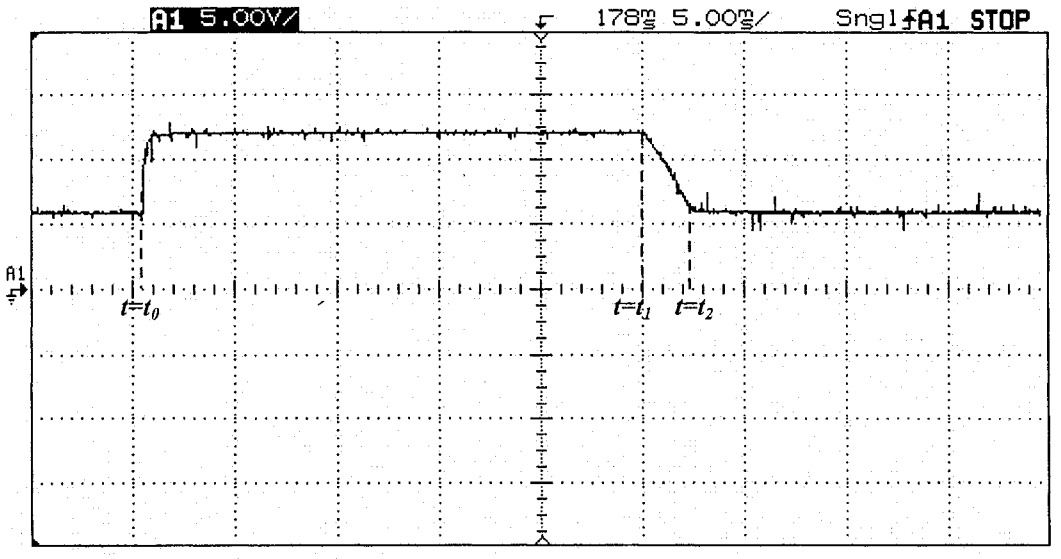
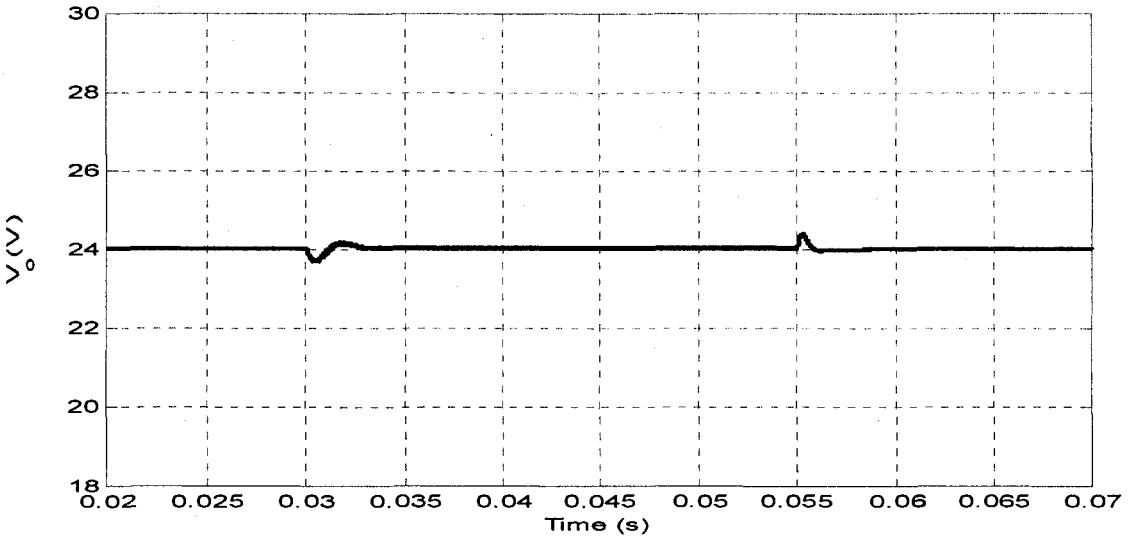


Figure 4-11: V_s performance with C_{in}=470 μF

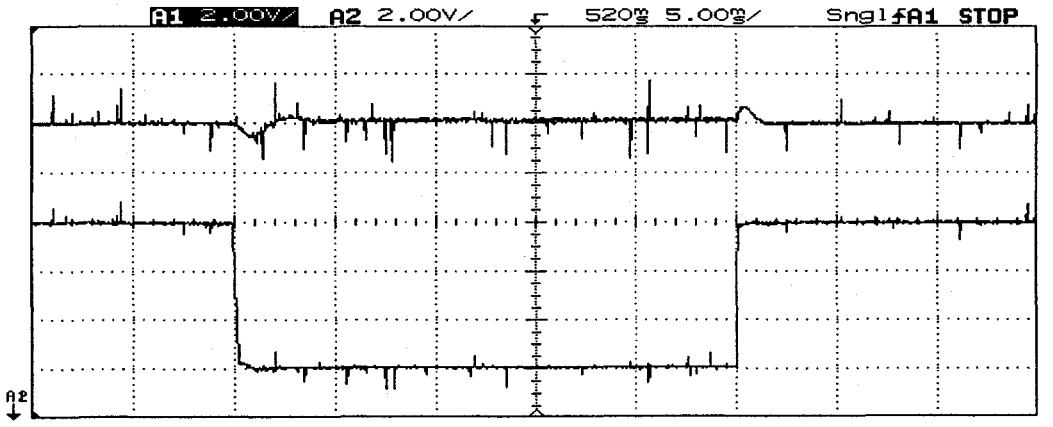
Hence, a C_{in} with smaller capacitance is used to obtain a sharper change from 12V to 6V. A value of 60 μF suffices for this purpose. Figure 4-12(a) shows the simulated output voltage response to 50% change in line voltage from 12V to 6V at t=0.3s and then from 6V to 12V at t=0.55 s. Experimental output performance, using C_{in} =60μF, along with the boost converter line voltage change is presented in Figure 4-12(b). Figure 4-13 presents the amplified filtered negative error voltage, measured at the input of the controller, along with V_i waveform.

Figure 4-12 illustrates a good match between the simulated and the experimental output responses with a slightly larger undershoot in response to the negative V_i disturbance. This slight deviation from the simulation results is due to the ringing of V_i and V_{s2} at the beginning of *Mode 3* (pg. 79) when diode D_s starts to conduct. This ringing behavior is a result of the sudden step change in the output current of the power supply V_{s2} from 0A to a steady state current of larger than 2 A. This current builds up with a dynamic behavior (ringing) determined by the output impedance of V_{s2}, stray inductance of wires, Diode D_s resistance, and by the dynamics of the boost converter system. Figure 4-14 shows the detail of V_i falling edge ringing along with the experimental output voltage response. The dynamic responses of the power supply V_{s2} and V_i waveform are illustrated in Figure 4-15. The dynamic effect of the supply V_{s2} on V_i waveform and on the output voltage performance are clearly demonstrated in these figures. On the other hand, for V_i rising edge, V_{s1} will apply a voltage difference of 6V on the capacitor C_{in} which will charge to 12V relatively fast through the MOSFET S in Figure 4-8.

Figure 4-16 shows the detail of the simulated and the experimental output voltage performance for the negative and the positive voltage disturbances, individually.



(a) Simulated output voltage performance



(b) Experimental output voltage performance and V_i

Figure 4-12: Output voltage performance for 50% voltage disturbance disturbances

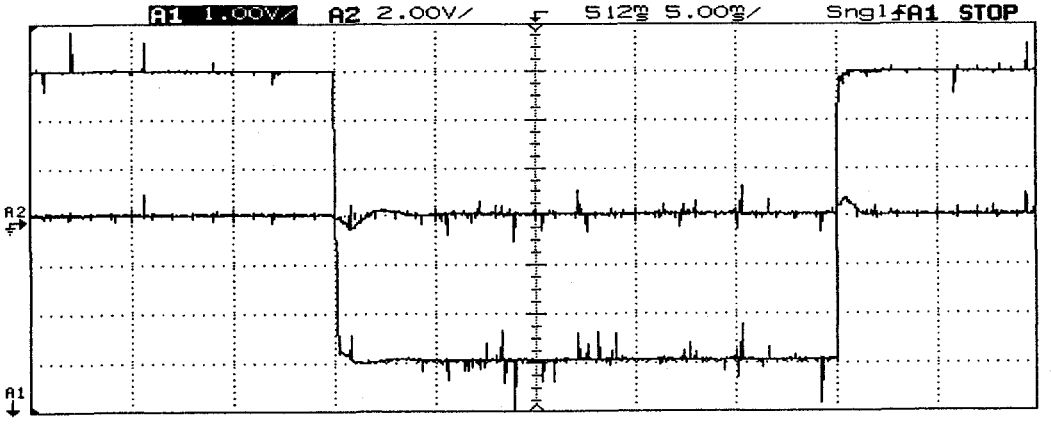


Figure 4-13: Amplified negative error voltage measured at the input of the controller

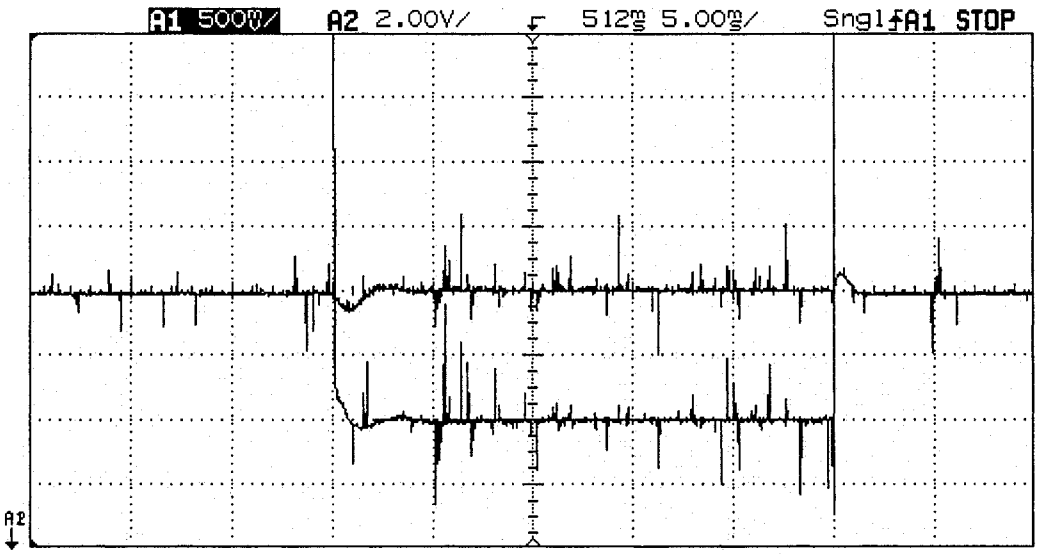


Figure 4-14: V_i Falling edge along with the output voltage performance

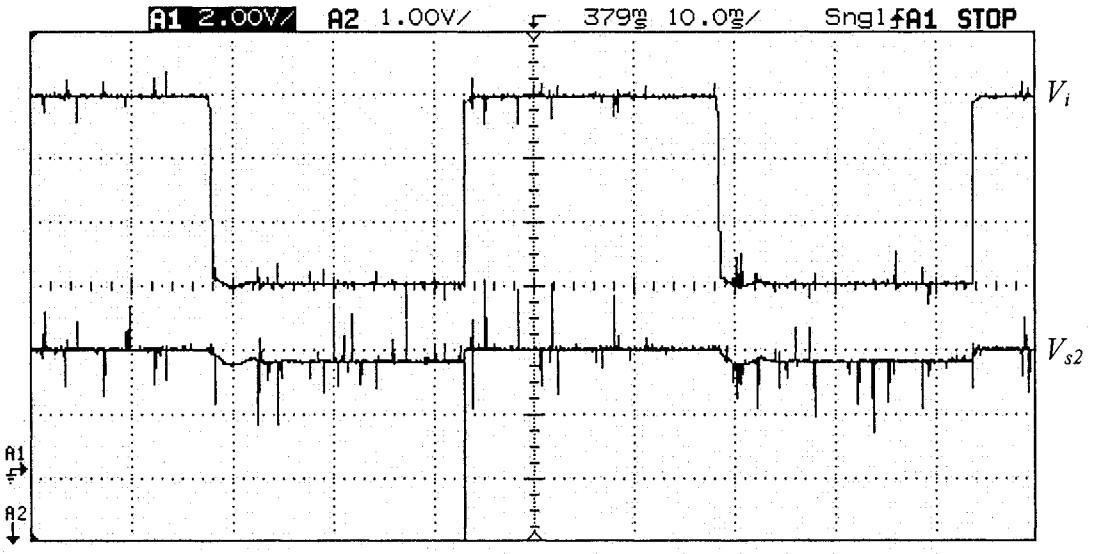
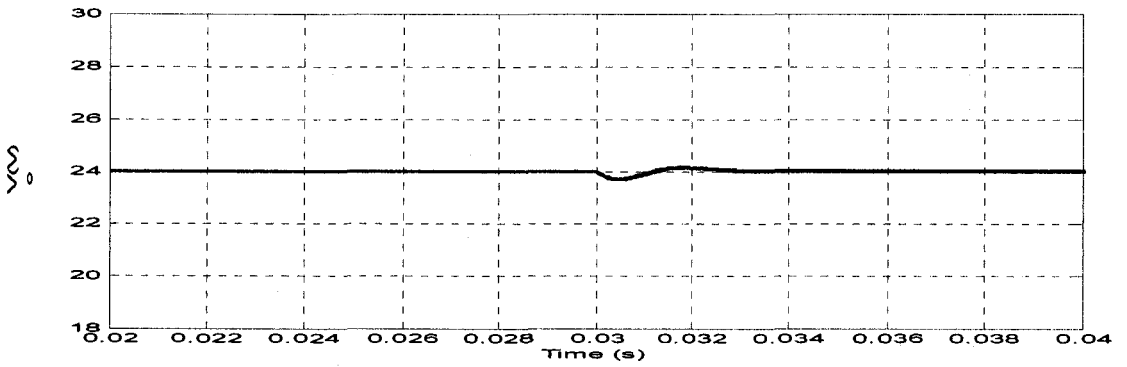
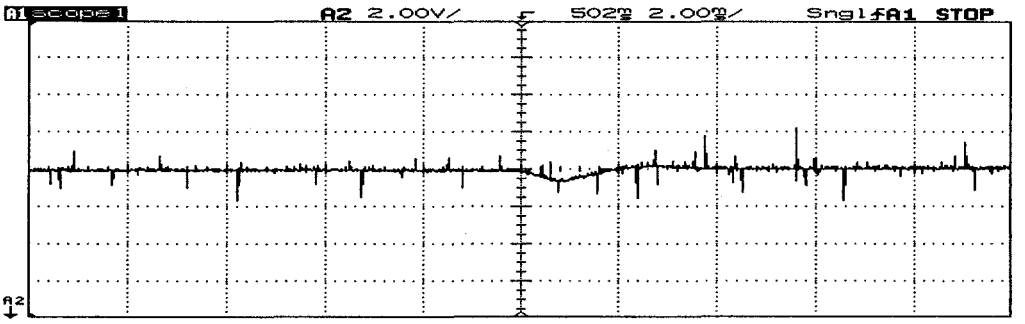


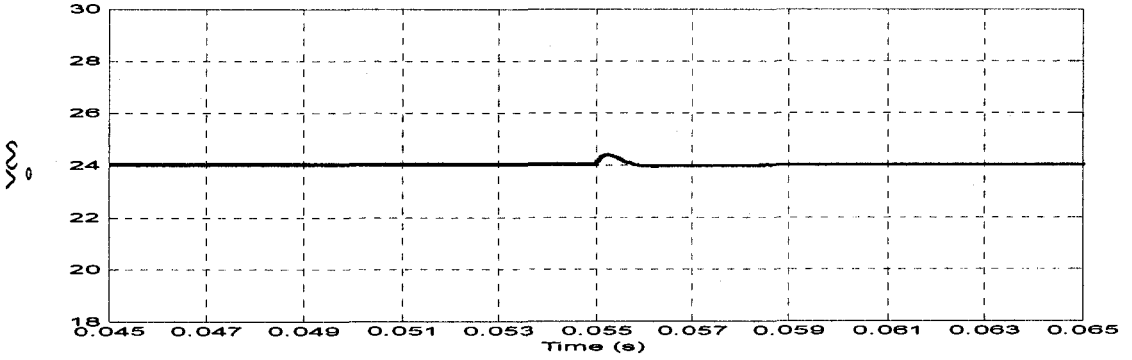
Figure 4-15: V_{s2} dynamic response and V_i waveform



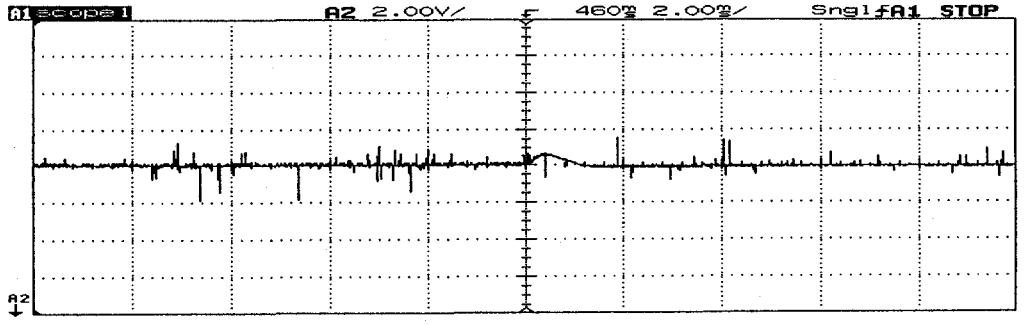
(a) Simulated output performance for negative line voltage disturbance



(b) Experimental output performance for negative line voltage disturbance



(c) Simulated output performance for positive line voltage disturbance

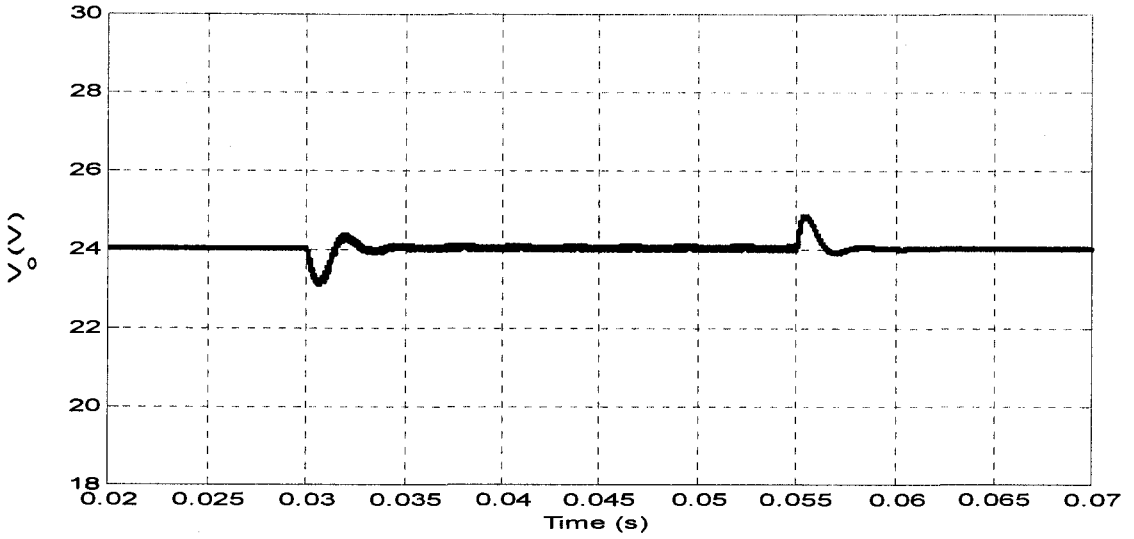


(d) Experimental output performance for positive line voltage disturbance

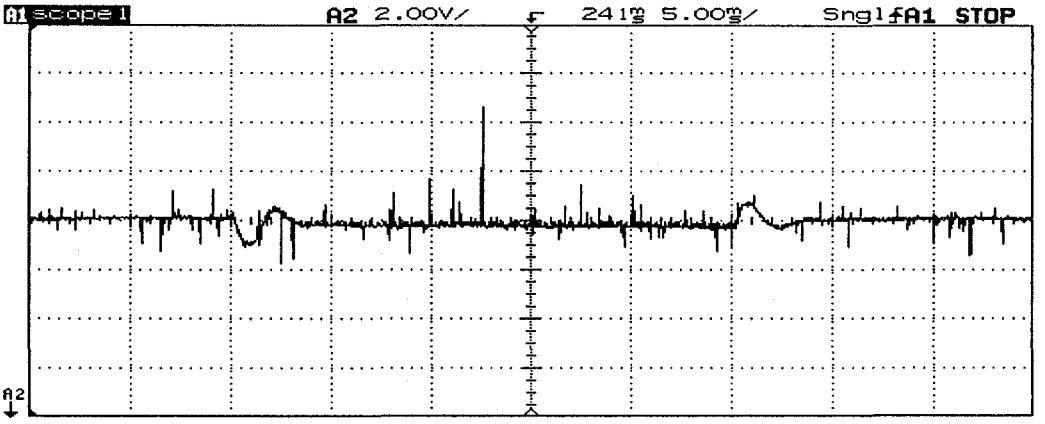
Figure 4-16: Output performance for 50% line voltage disturbances (Magnified)

4-5 Worst Case Disturbances Experimental Results

The control system is tested for worst case disturbances by applying 100% load step to the boost converter operating with a line voltage of 6V. Experimental setup is shown in Figure 4-5 with V_i=6V. Figure 4-17(a) shows the simulated performance of the output voltage for a 100% load disturbance applied as R_{load} step change from 50Ω to 25 Ω at t=0.03 s and then from 25 Ω to 50 Ω at t=0.055 s. The line voltage used throughout this experiment is 6V. The experimental performance of the output voltage for the same disturbances and line voltage is shown in Figure 4-17(b). Figure 4-18 presents the amplified filtered negative error voltage measured at the input of the controller. Figure 4-19 illustrates the detail of the output voltage performance for negative and positive disturbances individually. A good match between the simulated and experimental output response can be noticed from Figure 4-17and Figure 4-19.



(a) Simulated output voltage performance



(b) Experimental output voltage performance

Figure 4-17: Output voltage performance for worst case disturbances

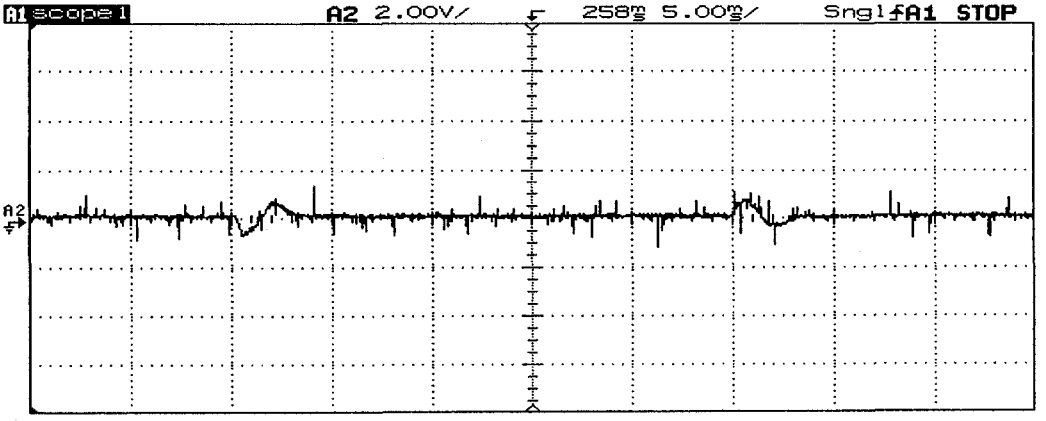
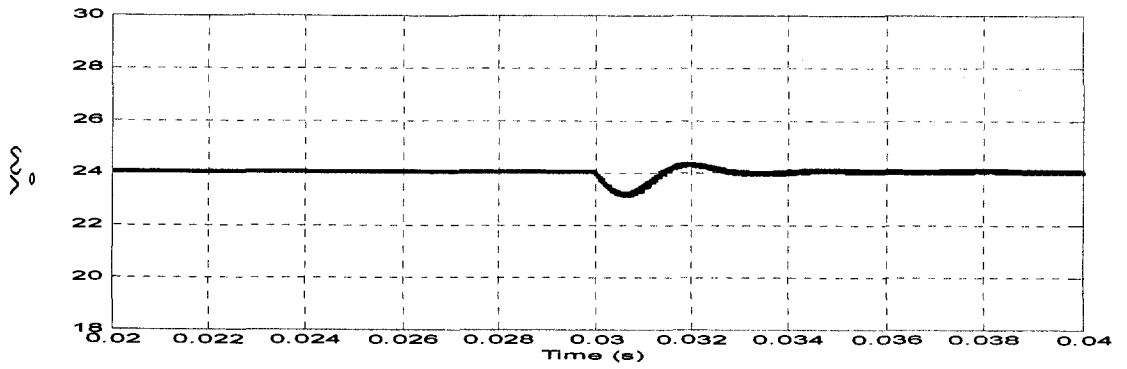
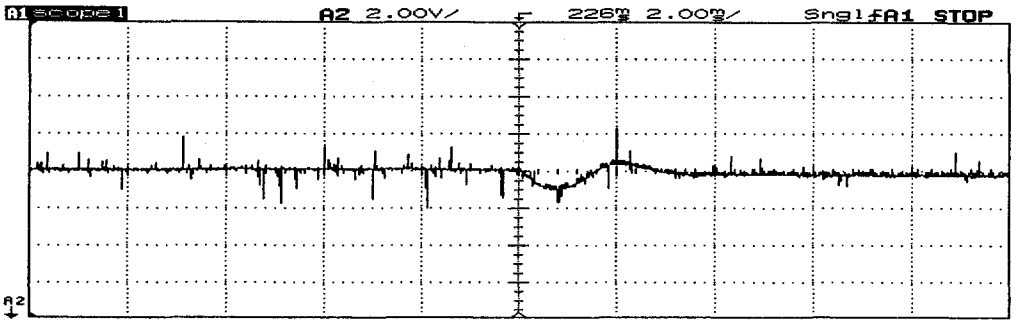


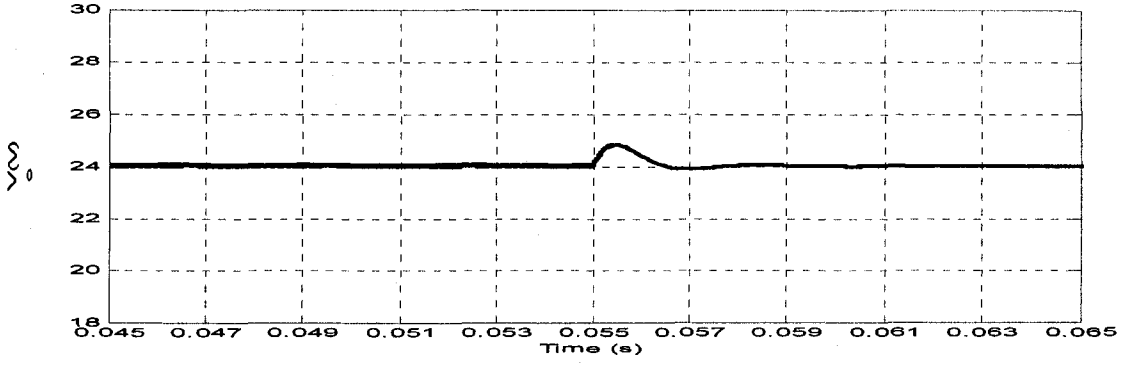
Figure 4-18: Amplified negative error voltage measured at the input of the controller



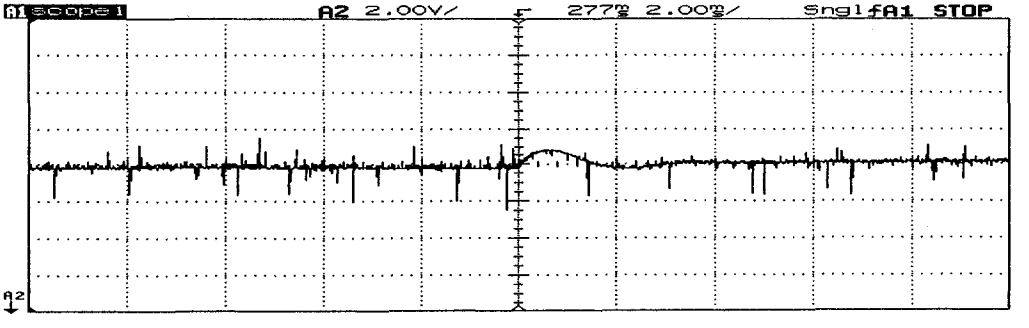
(a) Simulated output performance for positive 100% load disturbance (V_i=6V)



(b) Experimental output performance for positive100% load disturbance (V_i=6V)



(c) Simulated output performance for 100% negative load disturbance (V_i=6V)



(d) Experimental output performance for 100% negative load disturbance (V_i=6V)

Figure 4-19: Output performance for worst case disturbances (Magnified)

Chapter 5

Future Work and Conclusions

5-1 Future Work:

A simple linear controller for the DC-DC boost converter designed using the classical frequency response design method is proposed in this thesis. This controller achieves a superior performance to that of the H_∞, μ synthesis and passivity based integral control. New non-iterative formula have been derived to calculate the voltage collapse point and the operating regions for any given boost converter. The proposed controller and the derived formula have promising applications in isolated switch-mode converters especially the flyback converter. Flyback converter is derived from the buck-boost topology which has a similar non-minimum phase dynamic nature and, also, static characteristics of the boost converter with wider range of practical application in industry. However, for flyback converter, the transformer leakage inductance, magnetizing inductance and transformer losses should be taken into account in the modeling of the converter and the design of the controller. Moreover, the formulae derived in this thesis to calculate the static characteristics and voltage collapse point should be extended for the flyback topology to incorporate the transformer parasitic parameters and the snubber circuit resistive parameters. The extended formulae will be very valuable in choosing the flyback converter component values and in the design of the transformer and the snubber circuit to avoid the voltage collapse and guarantee the required stable operating region corresponding to the expected disturbances.

5-2 Conclusions:

The main achievements and conclusions of this thesis can be summarized as follows:

1. Simple and robust controller is proposed.
2. Simple and easy-to-use design procedure is developed using classical frequency response approach.
3. For small disturbances, simulation shows that the proposed controller is better than the most recognized H_∞ controller in literature.
4. For large disturbances, the proposed controller achieves excellent performance compared with passivity based integral control.
5. Boost converter parameter deviations, disturbances (magnitude and polarity) that can lead to worst case stability frequency response have been investigated. This can be used in the robust design of the boost converter controller instead of the unstructured uncertainty used currently in the literature which leads to conservative results.
6. Non-iterative formulae for static nonlinear characteristic curves and voltage collapse point of the boost converter considering parasitic parameters have been derived.
7. It is shown that there is a limited stable range for duty cycle beyond which the converter exhibits unstable operating points.
8. Small signal analysis does not reveal the instabilities due to transient controller excursions into the unstable operating regions and often reveals adequate gain and phase margins.
9. For a given boost converter, the load limit and the line disturbance limit corresponding to a given operating point have been delineated and no normal controller can avoid instability beyond these limits.
10. Consequently, the term "large disturbance" must be scaled for each converter.
11. Disturbances applied to the converter in the literature cited for testing the designed controllers are often inappropriate from this point of view
12. It is impossible to achieve global stability with regulated output voltage for a boost converter.

13. The static characteristic curves and the corresponding equations obtained through the analysis of this thesis enables choosing of the boost components in the design phase taking into account the range of disturbances, and leads to good choice of operating point for the converter.
14. It is shown that a controller in combination with a saturation limit on the maximum duty cycle derived in this thesis provides robust performance in the face of appropriate disturbances.
15. The static characteristic formula of the boost converter and the proposed controller are experimentally verified.

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Appendix A

Experimental Setup

Experimental circuit diagrams are given in this appendix. Figure A-1 illustrates the boost converter circuit along with the driving circuit and the synchronization circuit. Synchronization circuit is used to generate the driving signals for MOSFETs S_1 and S_2. Figure A-2 shows the circuit diagram of the controller. Duty cycle saturating circuit is shown in Figure A-3

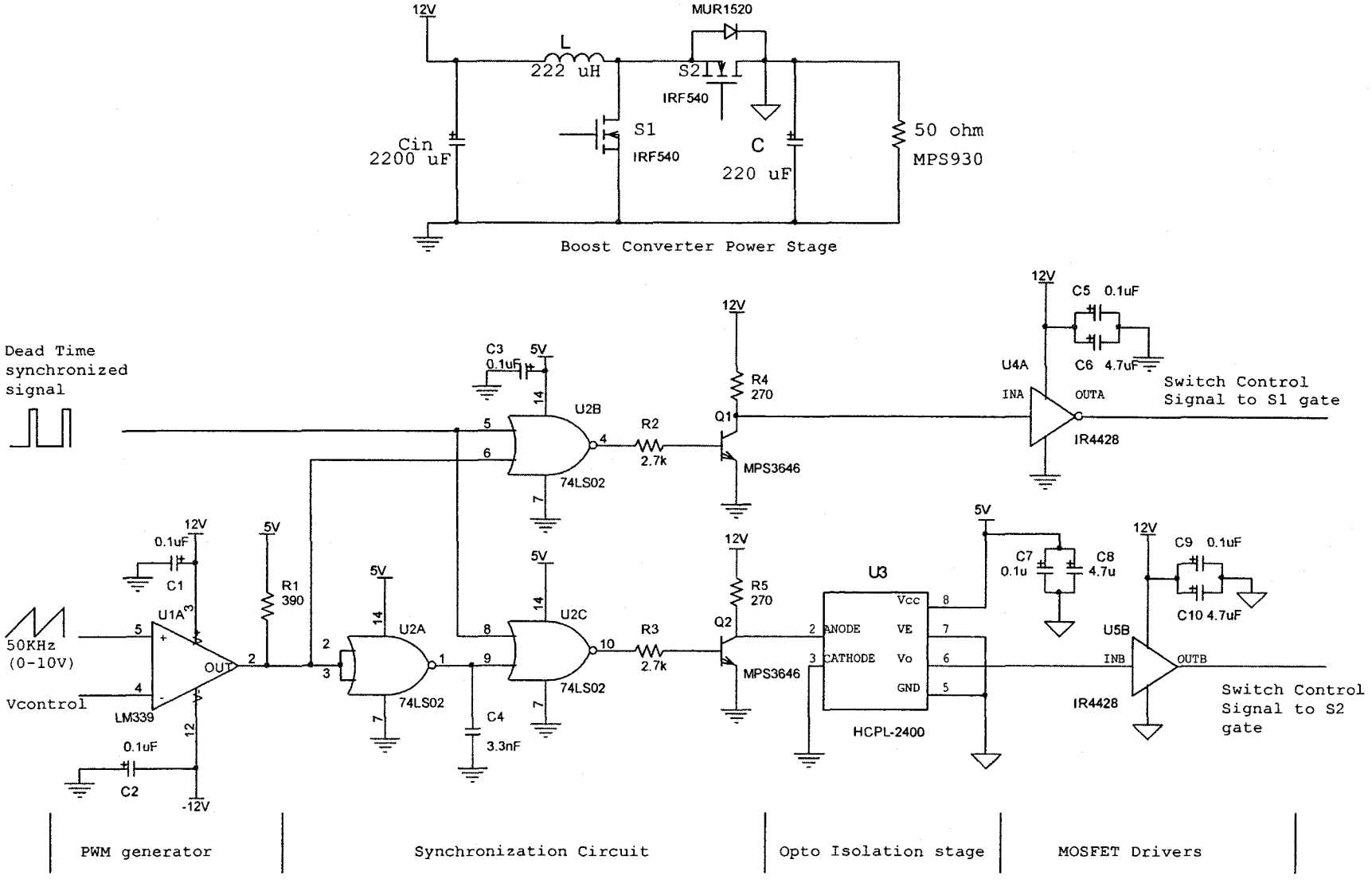

Figure A-1: Boost Converter Driver Circuits

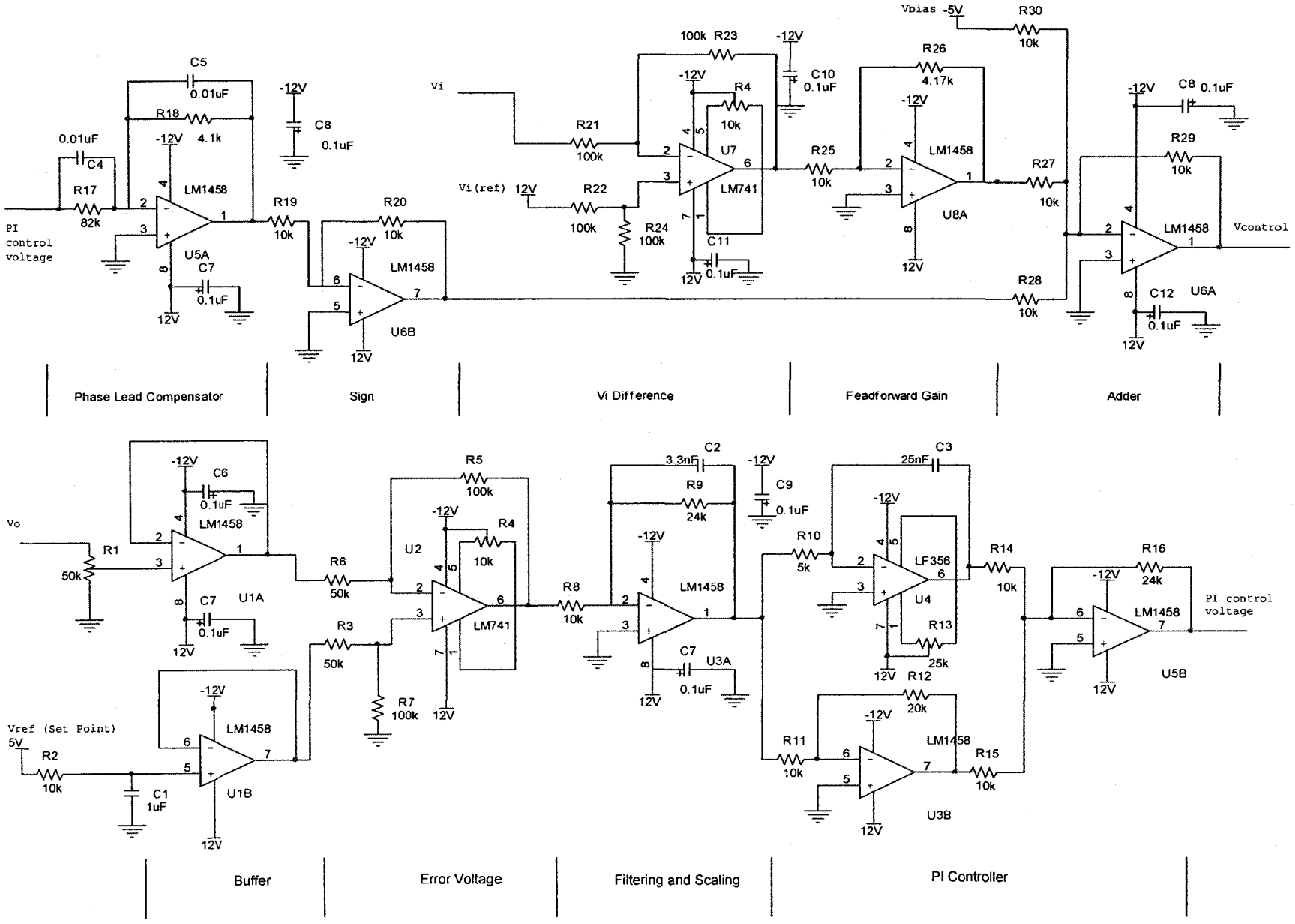

Figure A-2: Experimental Controller Setup

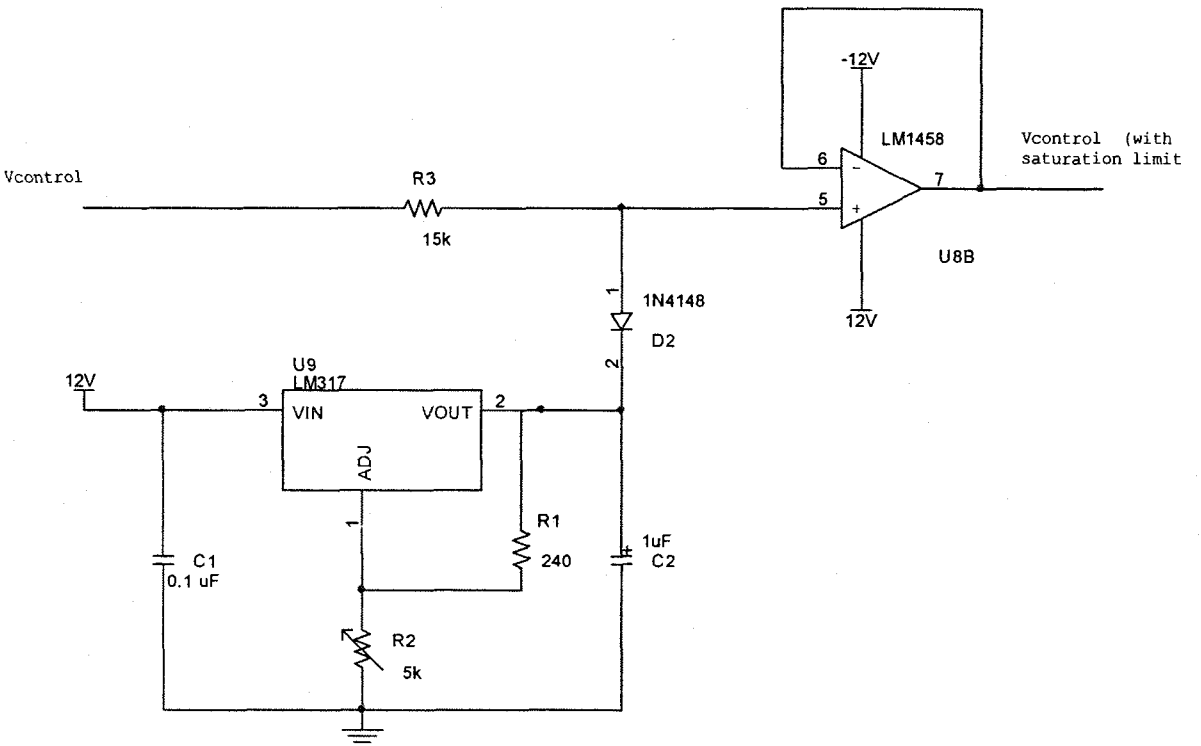

Figure A-3: Duty cycle saturating circuit