LOW-POWER MULTI-BAND INJECTION-LOCKED WIRELESS RECEIVER

by

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A Thesis

Presented to Lakehead University

in Partial Fulfillment of the Requirement for the Degree of

Master of Science

in

Electrical and Computer Engineering

Thunder Bay, Ontario, Canada, 2019

AUTHOR'S DECLARATION FOR ELECTRONIC SUBMISSION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

ABSTRACT

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The demand for low-power high-performance wireless receivers has dramatically increased with the emerging deployment of wireless sensor networks (WSNs). Among the demodulation schemes, non-coherent receivers consume less power in comparison with its counterpart, e.g. the coherent receiver, attributed to its simple architecture and fewer components. The injection-locking based envelope detection design, consisting of a low-noise amplifier (LNA), injection-locked oscillator, and an envelope detector, has drawn a lot more attention in recent years for low-power non-coherent demodulation. However, the utilization of the injection-locked oscillator, providing flexibility and high performance, remains quite challenging.

This thesis describes both the circuit level and mathematical model of injection-locking, allowing for the implementation of a CMOS receiver offering low-power, high performance and the ability to support multiple radio frequency bands. By leveraging both fundamental and superharmonic injection-locking, the receiver is capable of operating at five frequency bands, e.g., 433 MHz, 863 MHz, 915 MHz, 950 MHz, and 2.4 GHz, used for WSN applications.

One of the challenges of making use of superharmonic injection-locking is the narrow lock range that is insufficient for the oscillator to implement frequency-to-amplitude conversion under the locked-in status while maintaining low-power performance. A mathematical model developed in this work reveals the relationship between the lock range of superharmonic injection-locking and the third-order coefficient of the nonlinearity. An examination of the injection transistor operating in the weak and strong inversion region leads to the discovery of an optimal biasing point in the subthreshold region where the maximum lock

range can be attained. Moreover, a further investigation of the dependence of the third-order coefficient of the nonlinearity and the lock range is demonstrated. As a consequence, a technique to additionally extend the lock range via body biasing and p-well injection using a triple-well NFET device is presented.

The receiver was designed in GF 130 nm CMOS technology with a 0.7 V supply voltage. Based on the simulation results, the design achieves a data rate of 5 Mbps for four of the frequency bands and 4 Mbps for the 433 MHz band for both FSK and OOK signals. With two modes of operation, the receiver consumes 770 μW and 685 μW of static power, while achieving a sensitivity of -85 dBm and -75 dBm. The FOM for each mode are 155 pJ/b and 137 pJ/b.

The linearity properties, e.g., 1-dB compression point (P_{1dB}), third-order intercept (IIP3) of LNAs, suffers significantly in ultra-low-power (ULP) applications attributed to the biasing condition of the main transistor. To alleviate this issue, there is typically a trade-off with voltage gain and power performance, degrading the overall design. Based on the investigation of the relationship of the biasing point and the nonlinearity of the transistor, a complementary common-source (CS) LNA was designed in GF 130 CMOS process for optimal voltage gain, power consumption and linearity. By using the symmetrical properties of the NFET/PFET pair, the linearity of the LNA is enhanced. As a result, the simulated voltage gain, IIP3, P_{1dB}, and NF are 15.7 dB, -6.5 dBm, -17.5 dBm and 5.7 dB respectively. The total power consumption is 35 μW from a 0.7 V supply voltage. The evaluated performance of the design using a classical figure of merit (FOM), achieves the highest known value by a significant margin in comparison with state-of-the-art work.

ACKNOWLEDGMENTS

I would first like to express my sincere gratitude to my supervisor Dr. Yushi Zhou, by initially sparking my interest in the field of analog and RF design through his undergraduate courses and accepting me on as a graduate student, providing me with a great learning experience with his kind support, excellent expertise, and invaluable knowledge throughout our countless discussions. Also encouraging free thinking and confidence in research capabilities and inspiration to continue further.

Secondly, I would like to thank Dr. Carlos Christoffersen for his informative discussions and kind assistance, as well as being able to learn from his excellent teachings in RF design. I would also like to thank Dr. Natarajan for his kind support and encouragement throughout my studies at Lakehead. Thank you to Dr. Qiang Wei for acting as one of my committee members, providing useful comments on this work. Thank you to Dr. Fei Yuan from Ryerson University for his contributions in my research.

On a personal note, I would most importantly like to thank my parents for showing me the value of education, discipline, and hard work and also providing me with their unconditional love, care, and support. I would also like to thank Jema for always being by my side throughout our thesis work, making this a joyful experience. Also, thank you to my grandparents and sister for their love and support.

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List of Symbols

AC	Alternating Current
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
ASK	Amplitude-Shift-Keying
$BPSK$	Binary-Phase-Shift-Keying
BW	Bandwidth
CAD	Computer-Aided Design
$CMOS$	Complementary Metal-Oxide Semiconductor
dBm	Decibel power with respect to 1 Milliwatt
DC	Direct Current
DCR	Direct-Conversion Receiver
$DCRO$	Digital Controlled Ring Oscillator

DRO	Digital Ring Oscillator
DSP	Digital Signal Processing
ED	Envelope Detector
FM	Frequency Modulation
FOM	Figure of Merit
FSK	Frequency-Shift Keying
$IEEE$	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
$ILFD$	Injection-Locked Frequency Divider
ILO	Injection-Locked Oscillator
ISM	Industrial Scientific Medical (radio bands)
LC	Inductor-Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MCU	Microcontroller
$MOSFET$	MetalOxideSemiconductor Field-Effect Transistor
NF	Noise Figure
OOK	On-off Keying
PA	Power Amplifier
PLL	Phase-Locked Loop
PVT	Process Voltage Temperature

QAM	Quadrature-Amplitude-Shift-Keying
$QPSK$	Quadrature-Phase-Shift-Keying
RF	Radio Frequency
RLC	Resistor-Inductor-Capacitor
SoC	System-on-Chip
SR	Super-Regenerative
ULP	Ultra-Low-Power
UWB	Ultra-Wide-Band
VCO	Voltage-Controlled Oscillator
WSN	Wireless Sensor Network
$WPAN$	Wireless Personal Area Network
$WBAN$	Wireless Body Area Network

Chapter 1

Introduction

The emerging field of wireless sensor network (WSN) technology enables end-user access to valuable information through the deployment of spatially dispersed remote wireless sensor nodes, performing a collaborative measurement process. These wireless sensors are complex integrated chips, termed the name "system-on-chip" (SoC) as they combine analog, digital and RF communication functional blocks on a single substrate and are used in a wide variety of applications. Examples include but are not limited to, environmental monitoring for irrigation control and forest fire detection, home automation for security and surveillance, patient health monitoring and diagnosis, sustainable energy systems for smart cities, intelligent transportation services, industrial control, and structural health monitoring [1, 2, 3, 4, 5]. The results and overall impact of WSN technology has significantly benefited today's society by providing information and control, improving both the performance and ease of a multitude of areas, e.g., health, commercial, industrial, transportation, etc. Thus enhancing the overall quality of life. Therefore, there is a high market demand for high-performance wireless sensors. However, the rapid scaling of digital CMOS technology has brought a new challenge of lowering the power consumption while maintaining high performance functionality. It is therefore, of importance to introduce innovative and creative solutions to meet the market requirements [6].

The basic process for a WSN to convey end-user information via remote wireless connectivity is established by the incorporation of robust wireless sensor nodes to record and monitor physical properties, e.g., light, temperature, pressure, air; a communication proto-

col to effectively transmit and receive the information; and a base station such as a cellular phone or computer for end-user information display. A key property of WSN applications is maintaining low communication costs. As a result, low data rates and narrowband radio frequency (RF) communication is the standard form of data transfer. Additionally, maintaining low-power operation is a critical concern since a large majority of the sensors are positioned in remote and isolated areas, operating under a limited enery source. Although, medical applications such as implantable devices exhibit higher-data rates [7], in general reducing power consumption is a major factor. With these observations in mind, the selection of the communication protocol and design of the wireless sensor node require special attention as they dictate the overall outcome in the performance of the WSN.

The IEEE 802.15.4 and IEEE 802.15.6 standards are the favourable choices for the communication protocol when implementing a WSN since they both target low-cost and low-power applications. The 802.15.4 standard physical (PHY) layer allocates the 433 MHz, 868 MHz, 900 MHz, and 2.4 GHz industrial, scientific, and medical (ISM) frequency bands for low-cost and low-power wireless personal area networks (WPANs), with a maximum data rate of 250 kbps for a 10-meter communication range [8]. Similarly, the PHY layer for the 802.15.6 standard defines the 402 MHz, 868 MHz, 915 MHz, 950 MHz, and 2.4 GHz frequency bands for low-cost and low-power wireless body area networks (WBANs) dedicated for wearable and implantable medical devices. The data rates range from 0.5 Mbps to a maximum of 10 Mbps with a communication range of 5-meters [9]. Alternatively, the Zigbee and Bluetooth protocols, which are based on the IEEE 802.15.4 and IEEE 802.15.1 specifications respectively are optional choices as they both target short-range, low-power and low-cost applications [10]. Typically, technologies such as Wi-Fi and UWB are avoided due to the high communication costs and data rates. Wi-Fi, for example, has a maximum signal rate of 54 Mbps [11], which is not necessary for WSN applications. Nevertheless, WSNs contain a variety of readily available communication protocols and technologies to meet both low-cost and low-power requirements.

The wireless sensor node is usually comprised of four main modules: front-end transceiver, processor, transducer or sensor, and power supply. The front-end transceiver provides the

medium for wireless information transfer and communicates with adjacent sensor nodes or the base station. Within this block, the analog signal processing performed consumes large amounts of power. The processor is responsible for performing the signal processing from the transducer, as well as storing information. The microprocessor dealing with the digital signal processing (DSP) usually includes analog-to-digital converter (ADC), microcontroller (MCU) and a memory block. The transducer or sensing unit is the component required to convert the measured physical property into an electrical signal. The power supply consists of a battery or energy source and a DC-DC converter [12]. Furtheremore, the structure of the wireless sensor node is small in physical size and volume, with dimensions typically in the range of 1 cm^3 and are built to function in harsh environments and under extreme climate conditions. Unfortunately, due to limited structure and resources allocated towards the device, maintaining low-power and high-performance operation has proven to be a difficult task. To illustrate the preceding point, most applications place the sensor node in remote and isolated locations, where the sensor is required to operate for extended periods, with shelf-lives ranging up to 5 years [13]. This proves challenging since it is isolated from the main grid and powered by a limited energy source. An example of a traditional energy source used in powering the device is lithium coin cell batteries due to their small size and low-cost production [14]. However, these batteries have a very limited lifetime and since the battery life is entirely dependent on the current drawn from it, the sensor device must be energy-efficient to operate for extended periods. A cost-effective alternative approach to powering the device is through RF ambient energy harvesting, which utilizes an RF power antenna tuned to a broadcast station and an integrated RF-DC rectifier to convert the transmitted power down to consumable power [15]. The drawback with this method is the power drawn has an inversely proportional relationship to the distance of the transmitted signal. Hence, at longer distances, this technique may not be viable. The outcome of these conventional energy sources used in powering the sensor node imposes a stringent power budget, demanding solutions to address this problem. Another technical impediment is attributed to the sensitivity limitation and communication range of the wireless sensor. In general, for the transmitter to generate a high powered RF signal, and for the receiver to achieve a low sensitivity, comes at the expense of power consumption. To mitigate the communication

requirements of the transceiver, the sensors can operate in a multi-hop fashion, i.e., communicate with nearby sensors. Unfortunately, applications may require thousands of sensors to work in unison by creating a transmit-and-receive medium back to the base station.

In summary, these design challenges demonstrate the importance of reducing the power dissipation emitted from the sensor node and enhancing system performance as it directly correlates to the application cost of the WSN. As a result, there is a high-demand for energy-efficient, high-performance and long-lasting wireless sensor devices.

1.1 Motivation and Objectives

To improve energy efficiency and extend the lifetime of the sensor device, the power dissipation from the front-end transceiver has to be addressed. The transceiver requires an additional demand of the available power budget in comparison to the remaining modules in response to the power-hungry analog CMOS circuit blocks, e.g., power amplifier, RF gain stage, low-noise amplifier (LNA). However, reducing the power dissipation and maintaining high-performance operation has demonstrated to be a difficult task, resulting in active research in low-power wireless receiver designs for WSN applications [16, 17, 18, 19, 20]. In general, the work involved in the development of sensor node transceivers reduces the overall complexity of the architecture and trades bandwidth (BW) efficiency for energy efficiency. As a result, modulation schemes based on non-coherent detection have been the popular choices for data extraction. Therefore, traditional wireless receivers that employ high-accuracy frequency conversion architectures are avoided since they adopt power hungry frequency synthesizer blocks required for local-oscillator (LO) generation and I/Q signal paths needed for data recovery. Prominent examples of receiver architectures utilized for low-power applications that can maintain sub-mW power and achieve excellent performance include the tuned RF (TRF), uncertain-IF, and the super-regenerative on-off-keying (OOK) based designs [16, 17, 18]. An alternative structure, known as the injection-locked oscillator (ILO) based envelope detection receiver offers a simplified architecture, demonstrating superior performance [19, 20]. The ILO receiver adopts a unique natural phenomenon known

as injection-locking, where an oscillator, when perturbed or injected by a sufficiently large periodic signal at a nearby frequency will shift the oscillator to the frequency of the injection signal. This frequency shift is referred to as fundamental injection-locking. Similarly, if the injected signal is operating at a harmonic frequency relative to the free-running frequency of the oscillator, the ILO can perform either frequency multiplication or division. These frequency operations are known as subharmonic and superharmonic injection-locking respectively [21] and have numerous application use. Examples include suppressing jitter accumulation in digital controlled ring oscillators (DRCOs), low-noise clock distribution networks, frequency prescalers in phase-locked loops (PLLs), robust process, voltage, and temperature (PVT) local oscillator (LO) generators, etc [22, 23, 24, 25]. One of the most important metrics to measure the performance of the ILO, is the lock range. The lock range refers to the range of frequencies that satisfy the locking condition of the oscillator which in general depends on the properties of the incident signal and the oscillator itself, e.g., quality factor, resonant frequency, output voltage, etc. It is critical to ensure that the lock range is large, as it enables the receiver to capture and lock to a wide range of frequencies.

In an ILO based receiver design, it is common to implement the oscillator of a differential LC type or ring oscillator topology. The LC topology exhibits superior phase noise performance in comparison with a ring oscillator. However, the ring oscillator reduces the silicon area by eliminating the need for large passive inductors [26]. Usually, the former is preferred and chip size requirements are relaxed since the ring oscillator suffers from severe frequency drift requiring calibration techniques. Due to the narrowband characteristics from the high Q properties of the resonator in an LC oscillator, the magnitude of the lock range is small. To compensate, the injection power applied to the oscillator has to be increased but that typically requires additional power consumption from the amplification stage. Alternatively, a technique known as inductive shunt-peaking [27] can be used to enhance the injection power by implementing an inductor to resonate out unwanted parasitic capacitance. Unfortunately, the chip size becomes significantly large and is not desirable in an LC configuration. Active-inductors can be used to eliminate the large passive components which have demonstrated effective performance in injection-locking systems to achieve an extended lock range [28, 29]. A drawback with the active-inductor approach in sub-GHz

and GHz frequency applications is the value of the inductance has an inversely proportional relationship to the transconductance of the transistor. Meaning, for a reasonable value of inductance, the transistor has to obtain a high transconductance when targeting higher frequencies, thus requiring larger drain currents and increasing the overall power consumption. In general, a majority of the work investigating techniques to extend the lock range adopt passive inductors or complex high-order filters to couple the superharmonic and fundamental lock ranges which have not been demonstrated practical for use in narrow RF applications [30, 31, 32, 33, 34, 35, 36]. Therefore, newer solutions are necessary to enhance the lock range that can be employed for WSN applications.

In addition, previous work adopting the ILO based receiver have only utilized a single form of injection-locking to target a single frequency band. Also, the superharmonic injection that performs divide-by-4 frequency division has not yet been explored for receiver purposes. Therefore, motivated to apply multiple types of injection-locking to capture a wide range of frequency bands, correctly utilize divide-by-4 injection, explore lock range enhancement techniques to improve performance and driven to meet the growing demand in energy-efficient and high-performance wireless sensor node devices, the objective of this work is to design a low-power ILO based multi-band wireless receiver that targets WSN frequency bands within the 400 MHz - 2.4 GHz spectrum and further investigate new techniques to enhance the lock range of ILO to improve system performance and mitigate power consumption.

1.2 Contributions

In this section, the contributions of this work are summarized.

1.2.1 Low-Power Receiver

The main contribution of this work is the design of a sub-mW multi-band CMOS wireless receiver that covers a total of 5 frequency bands within the 400 MHz - 2.4 GHz spectrum and can utilize both OOK and FSK demodulation. This is accomplished by adopting fundamental, divide-by-2 and divide-by-4 injection, in which the oscillator of the receiver is tuned

such that it can lock to the desired frequency band, making it attractive for WSN applications. The receiver incorporates three main blocks: LNA, ILO, and an envelope detector. A thorough analysis and implementation process of each block are presented and simulations are performed to demonstrate the overall functionality of the receiver. The receiver is compared with state-of-the-art work, resulting in a high-performance design.

1.2.2 Injection-Locked Oscillators

This work provides a detailed analysis and description of how to increase and optimize the lock range for divide-by-2 and divide-by-4 superharmonic injection. This is achieved by modelling the phenomena using the super-regenerative frequency divide-model, in which the injection transistor is treated as a harmonic mixer, composed of a nonlinear block and a pure-multiplier. As a result, the intrinsic relationship between a given lock range and their corresponding nonlinear coefficients is established. In the case of the divide-by-4, the lock range is proportional to the third-order nonlinear coefficient, which leads to the discovering of an optimal biasing point for the injection transistor to maximize the lock range. Additionally, this work expands on the third-order nonlinear relationship by exploring techniques to increase the magnitude of the coefficient, demonstrating a body-bias and p-substrate injection technique by use of a triple-well CMOS process further enhancing the lock range. A comparative study is also presented when the injection transistor is biased in the weak inversion and strong inversion region, obtaining a relationship between the region of operations and the lock range. Simulations are performed to measure the results of this work and demonstrate the findings.

1.2.3 Ultra-Low-Power LNAs

The design of a linearized ultra-low-power (ULP) LNA is proposed for WSN applications targeting the 902-928 MHz ISM band. The LNA adopts a common-source (CS) with a PFET active load topology utilizing complimentary derivative superposition (DS) for linearization. Optimal biasing metrics are studied and compared with the linearity properties of the main transistor (MT) of the LNA. The circuit uses an NFET which is biased

to optimize the LNA for voltage gain, power, and bandwidth efficiency. Then by exploring the third-order nonlinear relationship between the NFET and the self-biased PFET transistor pair, it is shown that an accurately sized device that exhibits an equal and opposite third-order nonlinear coefficient to one another, can reduce the overall nonlinear effects of the LNA. As a result, the LNA achieves a high third-order intercept point (IIP3) attributed to the compensated third-order nonlinearity around its operating point without the need for auxiliary components. Simulations are performed and compared with state-of-the-art work, in which the proposed design achieves the highest classical FOM.

1.3 Publications

1.3.1 Conference Papers

- **Jared Mercier** and Yushi Zhou *"35 μW Linearized LNA for WSN Applications"* in IEEE International Midwest Symposium on Circuits and Systems, 2019.

- Yushi Zhou and **Jared Mercier** and Fei Yuan, *"A Comparative Study of Injection-Locked Frequency Divider Using Harmonic Mixer in Weak and Strong Inversion"* in IEEE International Midwest Symposium on Circuits and Systems, 2018.

1.3.2 Journal Papers

- **Jared Mercier** and Yushi Zhou *"Low-Power Multi-Band Injection-Locked Wireless Receiver"* in IET Circuits, Devices and Systems, 2019 (To be submitted).

1.4 Thesis Organization

The remaining work of this thesis is organized as follows:

- Chapter 2 presents a discussion on non-coherent and coherent demodulation schemes, investigating the trade-offs for low-power applications. In addition, an overview of

state-of-the-art low-power receiver architectures is explored to investigate the advantages and disadvantages to meet the design criteria. The chapter concludes with the selected receiver design.

- Chapter 3 presents a detailed study on the theory of injection-locking in LC oscillators as well as the frequency-to-amplitude conversion property. A mathematical analysis of superharmonic injection-locking is demonstrated using the regenerative frequency divide-model to establish a relationship between the nonlinear coefficients and the lock range. Presenting the discovering of a lock range enhancement technique for divide-by-4 injection based on the third-order nonlinear relationship of injection transistor.

- Chapter 4 presents the design of the ultra-low-power LNA. This involves a discussion of optimal biasing and complementary derivative superposition to enhance the performance of the design. In addition, simulation results are demonstrated followed with a comparison of state-of-the-art work.

- Chapter 5 presents the design of the receiver. A thorough analysis of each circuit block within the receiver is presented, and the performance of the blocks and overall receiver operation is demonstrated through simulations.

- Chapter 6 concludes this work and provides future suggestions to improve the design as well as new areas to investigate for lock range enhancement.

Chapter 2

Receiver Architecture

This chapter presents an overview of receiver architectures applicable to meet the stringent power requirements and achieve an energy-efficient, low-voltage design. It begins with a discussion of coherent and non-coherent based demodulation techniques, by emphasizing the trade-offs between bandwidth and energy efficiency. Next, presenting basic circuit techniques to demodulate carrier signals for baseband processing. In addition, an examination and comparison of both modern and state-of-the-art receiver architectures is presented to illustrate possible candidates to meet the design criteria for the sub-mW multi-band wireless receiver. Concluding with a performance summary of recent low-power receiver designs from previous literature. Section 2.1 discusses the demodulation schemes regarding coherent and non-coherent schemes with various circuit techniques for data recovery. In section 2.2, a general overview of receiver architectures is discussed, concluding with a detailed examination of the injection-locked based architecture. Lastly, section 2.3 summarizes the chapter.

2.1 Demodulation Scheme

The choice of the demodulation scheme plays a significant role in dictating the overall power consumption of the receiver. The type of demodulation scheme can be categorized as either coherent or non-coherent detection, both having their own merits. Useful metrics to distinguish the differences between the two categories are spectral efficiency and energy efficiency. The former is defined as the throughput per unit bandwidth and the latter is

defined as the number of bits per unit energy consumption [37]. In general, the schemes that support higher data rates come at the expense of additional complexity in the receiver structure, resulting in a supplementary power budget. These usually apply to coherent based demodulation schemes. Similarly, the non-coherent schemes normally achieve high energy efficiency in the receiver at the expense of bandwidth performance. This section discusses the reasons for these trade offs and benefits of a non-coherent based design.

2.1.1 Coherent Detection

Coherent detection focuses on tracking the phase information of the received carrier signal to interpret the transmitted data. Examples of utilized coherent based demodulation schemes employed in receivers are binary-phase-shift-keying (BPSK), quadrature-phase-shift-keying (QPSK) and alternative forms of quadrature-amplitude-modulation (QAM). A BPSK waveform can expressed as [38]

$$x_{PSK}(t) = \sqrt{\frac{2E_b}{T_b}} cos(\omega_c t + \theta), \tag{2.1}$$

where E_b is the energy per bit, T_b is the bit duration, ω_c is the carrier frequency and θ is the phase. As a result, the transmitter modulates the phase θ from 0 to π corresponding to a bit of "1" or "0." The latter two demodulation schemes transmit a relatively more complex waveform to provide additional information throughput by modifying the amplitude of the carrier in conjunction with the phase θ. However, the general principle is the same. The receiver must then deconstruct and interpret the phase variations of the carrier for information processing.

The most fundamental approach to deconstruct a coherent based carrier signal is achieved by implementing an I/Q signal path, referred to as quadrature downconversion. The implementation is shown in Fig. 2.1 which consists of a set of mixers, low-pass filters (LPFs) and a highly accurate reference signal produced from a quadrature local oscillator (LO) [39]. The primary property is that the RF signal gets downconverted to two separate copies of itself that are 90° out of phase. The I and Q signals are referred to as the "inphase"

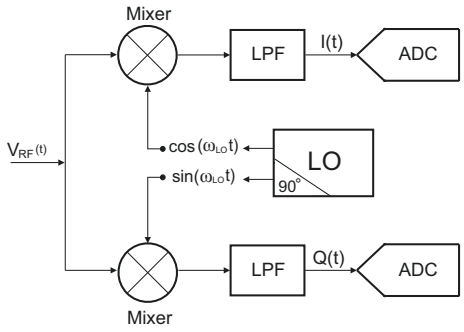


Figure 2.1: I/Q Signal Path.

and "quadrature" components that are formed by the RF carrier mixing with the LO signal in each path which is then applied to a LPF. The signals are then converted to digital form using an ADC for baseband processing. This technique is widely utilized in receivers, e.g., direct-conversion, modern Heterodyne, for achieving high spectral efficiency since the data is impressed on a complex two-dimensional plane, known as a constellation diagram [40]. However, this is at the expense of energy efficiency since producing an accurate reference signal from the LO generator results in additional power consumption and is one of the key elements to distinguish the difference in the circuit requirements for coherent and non-coherent based designs.

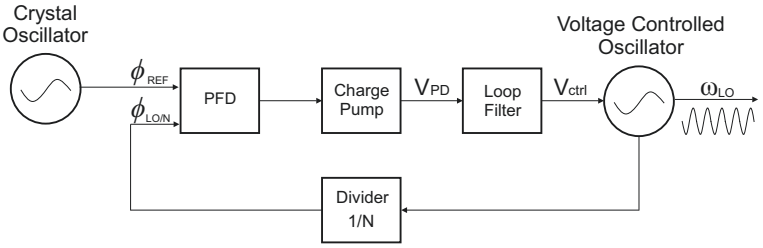


Figure 2.2: Phase-locked-loop.

Shown in Fig. 2.2 depicts a simplified PLL diagram to produce a clean LO signal with minimal phase noise. This is a widely adopted design technique when a highly accurate reference signal is desired. The PLL consists of a reference crystal oscillator, dividers, phase/frequency detector implemented using D flip-flops, charge pump and a voltage-

controlled oscillator (VCO) [41]. The PLL acts as a control system using the phase properties of the VCO as feedback to ensure that the generated output signal ω_{LO} is constant with minimal frequency drift. It is accomplished by comparing the phase and frequency differences of a crystal oscillator and a fractional version of ω_{LO}. If there is any phase variation between the two signals, the PFD and charge pump produce a voltage V_{PD} that is proportional to the difference of the phases. The control voltage is then filtered by the loop-filter and then is applied to the VCO for frequency adjustment. As a result, the LO maintains the accuracy required for the mixing operation in the I/Q path. Unfortunately, there is a considerable amount of circuit elements within the loop, which can be a difficult task to reduce the power dissipation while also maintaining high-performance. In addition, the target receiver design must cover the WSN frequency bands within the 400 MHz - 2.4 GHz spectrum, further increasing the complexity of the PLL requirements since obtaining such a wide-frequency range is not feasible under a single VCO. Because of these factors, coherent detection based schemes which rely on accurate reference signals, knowledge of the carrier phase information and additional circuit resources are avoided in low-power applications.

2.1.2 Non-Coherent Detection

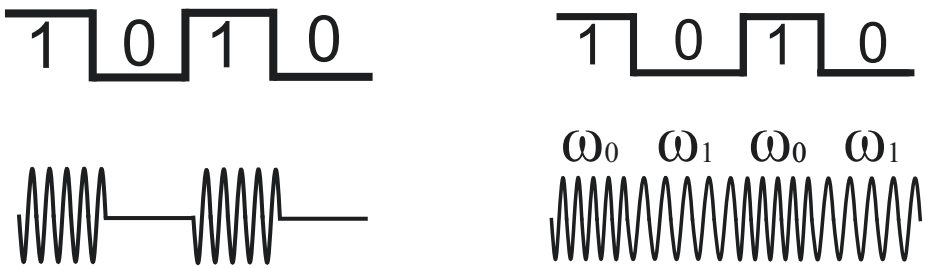
Non-coherent detection ignores the phase information of the carrier signal and uses techniques such as square law devices or matched filters to interpret the transmitted data. The most commonly used non-coherent demodulation schemes employed in low-power receiver applications are on-off-keying (OOK) and frequency-shift-keying (FSK). In terms of energy efficiency, OOK is more effective compared to FSK since various half-cycles of operation the receiver can function in a free-running or relaxed state. However, OOK increases the linearity requirements of the power amplifier (PA) to transmit an amplitude-modulated signal. On the contrary, FSK relaxes the linearity requirements of the PA and additionally improves spectral efficiency as it enhances the overall signal bandwidth. Regardless, both have excellent functionality with minimal complexity as opposed to the receiver requirements for a coherent based demodulation scheme. The waveform representing an OOK signal can be expressed as

$$x_{OOK}(t) = a_n cos(\omega_c t) \tag{2.2}$$

where the amplitude of the signal a_n switches states from 0 to 1 and reflects the digital information, i.e., "1" or "0." Similarly, a FSK carrier signal can be expressed as

$$x_{FSK}(t) = a_1 cos(\omega_0 t) + a_2 cos(\omega_1 t) \tag{2.3}$$

where the amplitudes $[a_1, a_2]$ are given by $[1, 0]$ or $[0, 1]$, corresponding to bits "1" or "0." Shown in Fig. 2.3(a) and Fig. 2.3(b) is an illustration of these types of waveforms and their converted digital outputs after baseband processing.



(a) OOK signal. **(b)** FSK signal.

Figure 2.3: Non-coherent signals.

The most popular circuit to perform baseband conversion for non-coherent schemes is an envelope detector (ED). An ED takes the voltage amplitude of a high-frequency signal and rectifies it using diodes or transistor devices, and a LPF to translate the frequency down to a lower value to produce a constant voltage. The original waveform will contain variations in the amplitude in which the diode or transistor converts the voltage of the carrier signal to a current, then back to voltage across the LPF. The converted current is injected through a LPF, to block out the high-frequency component, and the capacitor starts charging and discharging according to the amplitude transition of the applied signal. As a result, the ED produces an output voltage that captures the peak voltage variations of the

original carrier waveform. The basic output response of this operation is shown in Fig. 2.4, where the applied signal is amplitude modulated. During the period of the larger voltage peak, the capacitor will charge and remain at a constant voltage. As the signal decreases in magnitude, the capacitor discharges current through the resistor, decreasing the output voltage and establishes a new constant value. Thus, the ED can distinguish variations in signal amplitude necessary for baseband processing.

One of the challenges when designing an ED, is to ensure that the output voltage that represents alternative bits obtains a sufficiently large difference after detecting slight variations in amplitude from the high-frequency signal. MOSFET devices perform excellently for this requirement and are typically chosen as opposed to diodes.

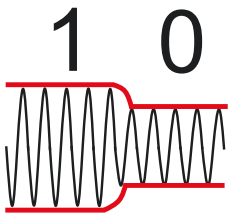
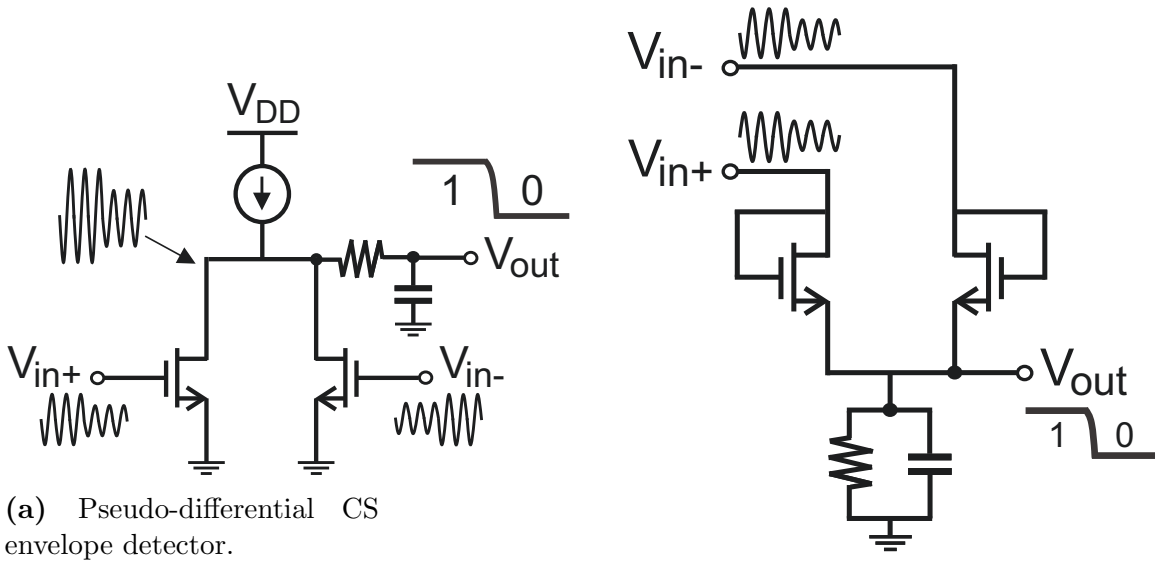


Figure 2.4: Envelope detector output.

The implementation of a MOSFET ED in a low-power receiver has many possible configurations. Shown in Fig. 2.5(a) and Fig. 2.5(b) are the pseudo-differential common-source (CS) and the diode-connected configurations commonly used. The former produces an output voltage that decreases as the input voltage V_{in} applied to the gate increases. The signal is then passed through a LPF for baseband conversion. Similarly, as the AC voltage across the diode-connected configuration varies, the drain current injected into the LPF varies. The high-frequency component is then filtered by the LPF and is converted to a baseband signal at the source node. In common receiver configuration, the signal entering the ED circuit is in a differential form, which is then converted to a single-ended output. Nonetheless, the design is simple as the ED only requires a sufficient AC voltage variation ($\sim$ 10 mVp) applied to the gate of the transistor for proper functionality. Moreover, the transistors can be biased in the sub-threshold region to exhibit nonlinear characteristics, improving signal

conversion and most importantly, operate at extremely low-powers, typically less than 10 μW [42, 43, 44]. Therefore, the ED is the most suitable and practical circuit for the receiver.



(a) Pseudo-differential CS envelope detector.

(b) Diode-connected envelope detector.

Figure 2.5: MOSFET envelope detectors.

However, an ED cannot recover data from an FSK waveform since the signal has an ideally constant amplitude and only contains frequency variations. Mixers can be implemented for frequency translation, similar to coherent demodulators. Unfortunately, the issue arises in regards to power consumption when an accurate LO signal is required through a PLL. In [45], a FSK receiver is demonstrated using quadrature downconversion, achieving low-power performance but the LO generation circuit is implemented using a ring-oscillator, suffering from severe phase noise and subsequently affecting the overall performance. An alternative technique presented in [46], uses matched filters implemented by parallel LC tank circuits prior to the ED. The filters are tuned at different resonant frequencies ω_1 and ω_2 according to the FSK signal. Depending on the transmitted bit, one of the filters will pass the RF carrier towards a particular ED. The comparator can then determine which bit was transmitted based on the response of the EDs. This simplified demodulation circuit architecture is depicted in Fig. 2.6.

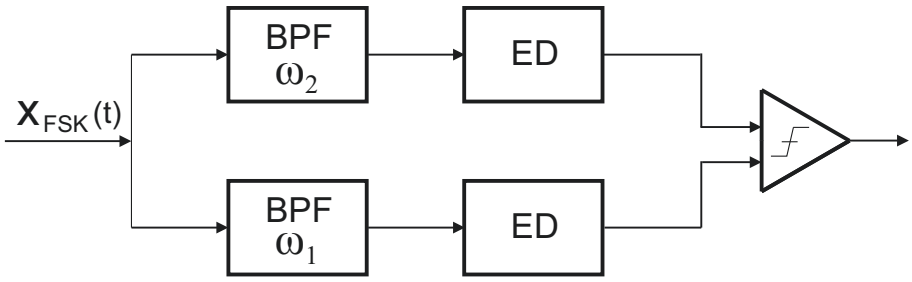


Figure 2.6: FSK demodulator using matched filters.

The issue with this approach when targeting multiple frequency bands is the amount of required silicon area attributed to the large passive inductors, which is not practical for a fully-integrated design. Additionally, the carrier frequencies would have to be spaced at relatively large distances due to the limitations of the quality factor of integrated LC tank circuits. A more practical approach to demodulate an FSK signal can be achieved by periodically adjusting the center frequency of the main oscillator [47] and injecting the FSK signal such that the output voltage contains variations in amplitude. This technique does not require additional silicon area as the tuning is all performed through digital CMOS circuits. The main point from these techniques is that in order to demodulate a FSK signal by making use of the ED, the frequency modulated signal must be converted to an amplitude modulated signal.

In summary, non-coherent detection adopts energy-efficient low-power circuit techniques with minimal complexity at the expense of spectral efficiency since the carrier phase information is neglected. In addition, most receivers targeting sub-mW operation adopt OOK demodulation since the ED operates at ultra-low-powers, with ease of integration.

2.2 Architecture Overview

In this section, an overview of low-power non-coherent based receiver architectures is presented, as well as traditional coherent receiver design.

2.2.1 Direct-Conversion

One of the most common architectures for a variety of RF applications is the direct-conversion receiver (DCR), also referred to as zero-IF or homodyne. The DRC is shown in Fig. 2.7, which incorporates a LNA, quadrature downconversion stage, followed by baseband circuits. The unique property of this configuration is the LO signal is tuned to the exact same frequency as the incoming RF signal. Thus, after mixing, the signal is translated down to a zero frequency. The advantage of this approach eliminates the problem of imaging. Imaging occurs when the frequency spacing between an RF and image signal is equal and opposite in magnitude relative to the LO signal. As a result, the resultant IF frequency after mixing becomes corrupted. However, the DRC eliminates the need for an IF frequency since the RF signal is directly converted down to DC.

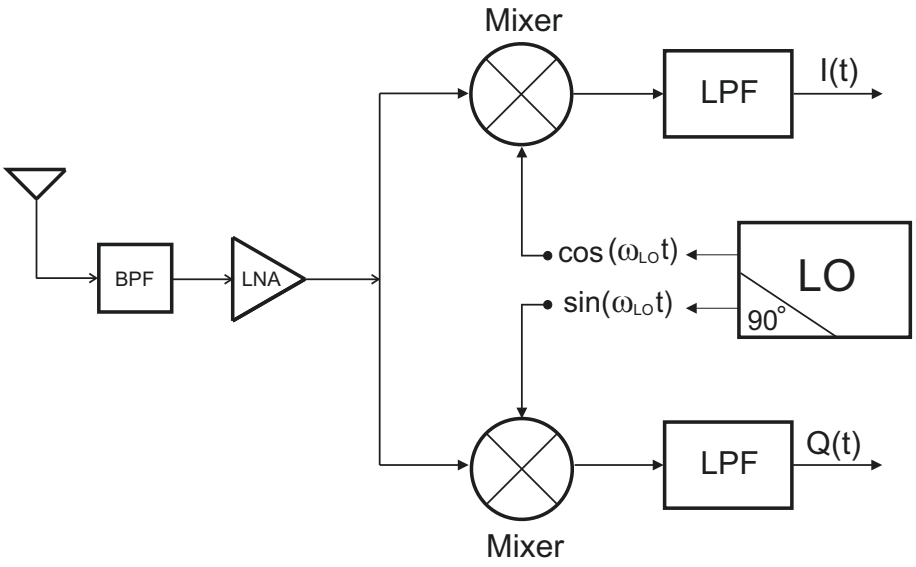


Figure 2.7: Direct-conversion receiver architecture.

Presented in [48], a DRC receiver is designed for WSNs targeting the IEEE 802.15.4 WPAN applications. Attributed to the frequency-synthesizers required for LO generation in the I/Q path, the power consumption is considerably above the sub-mW design requirement.

Similarly, demonstrated in [49], a DRC receiver is designed but the power consumption is relatively high attributed to the complex and power hungry clock generators.

In addition, the DRC is prone to high-flicker noise from the MOSFETs since the carrier is translated down to DC, as well as issues including LO leakage and DC offsets [39]. Therefore, the DRC is not an ideal architecture to achieve low-power performance mainly since it adopts the power-hungry quadrature downconversion property.

2.2.2 Uncertain-IF

The uncertain-IF architecture proposed in [50], eliminates the need of a highly accurate RF oscillator to meet the stringent phase noise requirements by utilizing a digital-control oscillator (DCO) connected in a feedback loop with an off-chip calibration circuit. The front-end architecture is shown in Fig. 2.8, which consists of a bulk acoustic wave (SAW) filter for precise selectivity and input matching, mixer, DCO, IF amplifiers and an ED. The DCO is implemented using a ring-oscillator configuration for low-power performance which is calibrated with an off-chip frequency calibration circuit. The off-chip circuit is not physically integrated on the receiver substrate which reduces the integration properties.

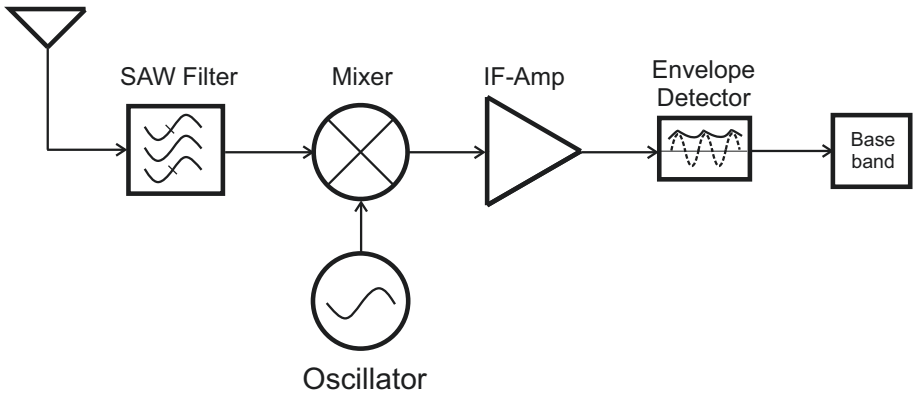


Figure 2.8: Uncertain-IF receiver architecture.

The RF signal directly mixes with the LO signal for IF conversion and is passed through the IF stage for amplification and demodulated using an ED. The advantage is that the amplification is performed at lower frequencies, achieving relatively high sensitivity performance. The functionality of this topology has also demonstrated excellent power performance, ranging less than 100 μW and have found application use for wake-up receivers [51, 17]. However, since the DCO requires external calibration due to the high-frequency drift characteristics of a ring-oscillator, this results in off-line calibration, increasing the overall system cost. Additionally, the number of SAW filters required for the selectivity requirements of covering the 400 MHz - 2.4 GHz frequency bands is not practical. Therefore, this architecture is not an effective choice to meet the design criteria, mainly due to system cost and the integration properties.

2.2.3 Tuned-RF

The RF envelope detection based architecture or tuned-RF, follows a similar approach to the uncertain-IF architecture. However, it eliminates the oscillator stage and consists of parallel RF amplification stages cascaded with an ED circuit. The power performance properties are excellent since the oscillator block is removed [52, 53].

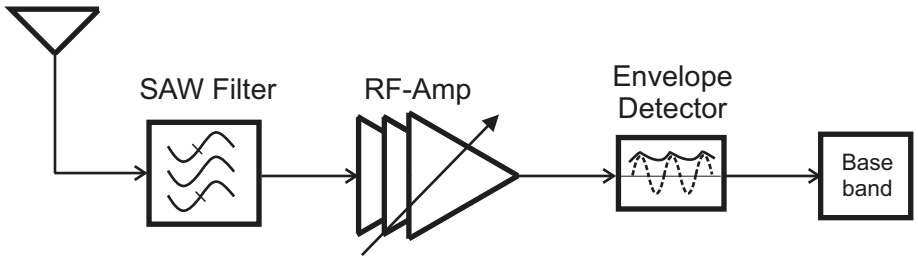


Figure 2.9: Tuned-RF receiver architecture.

The unfortunate drawbacks arise from the fact that the signal amplification is performed at RF frequencies, resulting in poor sensitivity performance. Additionally, the selectivity re-

quirements for channel selection increases system cost and reduces integration when targeting multiple frequency bands since the architecture relies on off-chip SAW filters. Moreover, the design can only demodulate OOK signals, increasing the linear requirements of the power amplifier (PA) on the transmitter side. Therefore, the tuned-RF is more ideal for wake-up receivers that do not require high sensitivities and target single frequency operation.

2.2.4 Super-Regenerative

The super-regenerative architecture has also demonstrated effective performance for low-power energy-efficient receiver designs [54, 55, 56, 57]. The block diagram is shown in Fig. 2.10, which consists of an LNA, quench controlled oscillator, ED, and baseband circuits. The basic principle in a regenerative system is that they do not contain a constant free-running oscillator and utilize an external signal to control the functionality of the clock. The external signal is referred to as a quench signal which controls the power up and down conditions of an oscillator in synchrony with an injected signal detected and amplified from the LNA. For signal detection, the receiver measures the startup time conditions of the oscillator as the quench signal is applied in conjunction with the transmitted OOK carrier wave. If the OOK signal transmitted is a "1," the oscillator produces a faster startup time as opposed to when a "0" is transmitted. This is based on the result of the natural response of the output voltage which has a dependency on the injected signal [58]. As a result, the output of the oscillator exhibits time variations in magnitude which is then applied to an ED and comparator for data recovery. It can also be considered as a system that samples the RF carrier signal with a sampling frequency equal to the frequency of the quench signal.

The receiver can achieve extremely high sensitivities since the amplitude of the injected signal is only required to vary the output voltage time response at sufficient lengths compared to the alternative of an absent signal. However, drawbacks include the complexity of the design when FSK demodulation is of interest for higher information throughput, requiring additional circuit elements, e.g., PLL, reference oscillator, etc. Moreover, the maximum attainable data rates are relatively low since the system requires a sampling period to establish the startup time condition of the oscillator based on the quench signal and re-

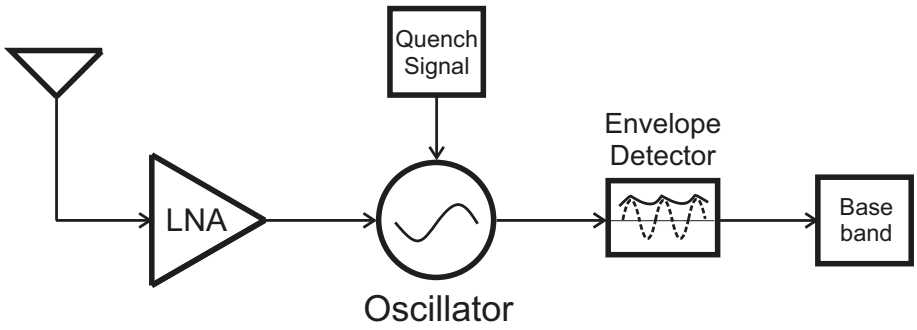


Figure 2.10: Super-regenerative receiver architecture.

ceived carrier waveform. In addition, the system requires an accurate constant quench signal with minimal phase noise. As a result, the complexity and power dissipation of the design increases. Thus, an alternative receiver architecture is of interest to meet the design criteria.

2.2.5 Injection-Locked

One of the most high-performance receiver architectures for low-power applications is the injection-locked based envelope detection design [59, 60, 61, 62, 63]. The architecture is shown in Fig. 2.11, which consists of an LNA, ILO, and an ED followed by baseband circuits.

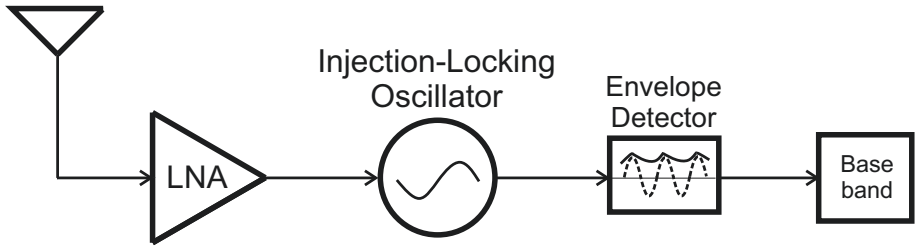


Figure 2.11: Injection-locking envelope detection based architecture.

To illustrate the functionality of the receiver, suppose that the LNA detects an OOK waveform representing a transmitted bit of "1" that has a sufficient amplitude operating a frequency nearby the free-running frequency of the ILO. The ILO will lock to the injected

signal and simultaneously alter the output voltage. Similarly, if the transmitted bit of "0" is detected by the receiver in which the carrier waveform has a zero magnitude, the oscillator returns to its free-running state and the output voltage reestablishes its original value. As a result, the ILO can detect a time varying voltage necessary for the ED to perform demodulation. Additionally, the ILO operates on a FSK signal in a similar fashion. However, instead of returning back to the free-running state, the ILO locks to frequency representing the transmitted bit of "0." Therefore, the output voltage is a function of the injected frequency within the lock range of the ILO. This relationship is depicted in Fig. 2.12, where the ILO produces an output voltage V_{out}, for a particular injection frequency ω_{inj}, that is valid within the bounds of lock range $(\omega_o - \omega_L)$ - $(\omega_o + \omega_L)$. Noting that Fig. 2.12 is an ideal representation since the lock range is usually not symmetrical around the oscillator's free-running frequency ω_o and the voltage does not approach zero as the incident frequency is near the edge. Still, the receiver maintains a simplified architecture design that can achieve dual FSK and OOK demodulation.

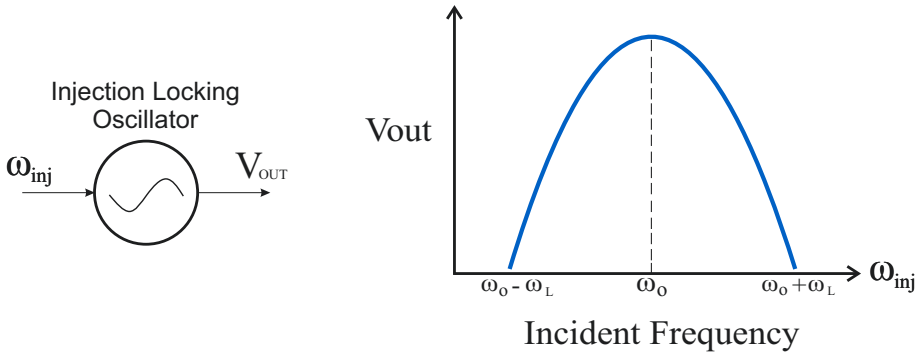


Figure 2.12: Frequency-to-Amplitude.

Furthermore, the time it takes for the oscillator to lock to the frequency of the incident signal is incredibly fast since the locking process is a form of phase modulation, allowing the receiver to achieve high data rates. In addition, with the ILO implemented using an LC-based topology, the phase noise performance is enhanced due to both the high Q properties

of the tank circuit and the injection-locking phenomena. In the latter case, as the ILO locks to an injected frequency, the phase noise decreases substantially, generating a clean signal. Also, the harmonic components of the ILO can mix with incoming frequencies. Thus, it is not imperative for a PLL and mixer for frequency operations since the ILO can perform sub and superharmonic injection, i.e., frequency multiplication and division. Suggesting that to target the desirable 400 MHz - 2.4 GHz frequency bands, the ILO has to be tuned such that it can utilize multiple forms of injection-locking within a reasonable tuning range. This will also improve dynamic power consumption since the main clock is operating at a lower frequency.

The main design challenge arises from the small lock range of the LC oscillator attributed to the narrow-band characteristics, resulting in limited sensitivity performance. Common techniques to compensate for the minimal the lock range, e.g., passive inductors, signal amplification, comes at the expense of silicon area and power consumption respectively, resulting in additional system cost. Another design consideration is to optimize the energy efficiency. This can be captured using the "energy per bit" metric, in which lowering the value is more desirable. The expression is defined by the following

$$E_b = \frac{I_{DD} * V_{DD}}{f_b}, \tag{2.4}$$

where f_b is the data rate, I_{dd} is the total current from the supply voltage V_{dd}, with units of J per bit. Observing that a receiver that can process higher data while reducing the energy or work required is more effective. In [63], the authors present an ILO FSK divide-by-2 receiver targeting the 915 MHz frequency band operating under a 0.7 V supply, achieving one of the best E_b with a value of 84 pJ/b. With inductive-shunt peaking used to enhance the lock range, and with the LNA providing a gain of 40 dB, the sensitivity was approximately -75 dBm. A similar design was proposed in [61], operating under a 1.2 V supply voltage, obtaining excellent performance with an E_b of 80 pJ/b. However, both designs only target a single frequency band, limiting the application use of the receiver. Additionally, the former design uses all inductive components implemented off-chip, reducing the overall integration

properties of the receiver. In the latter design, the supply voltage is relatively high, which does not scale well with present day technology. Therefore, additional work is required to improve the performance for low-voltage ILO receivers that can also obtain an enhanced lock range that provides ease of integration and reduces system cost.

2.3 Summary

This chapter demonstrated the advantages of non-coherent based demodulation schemes owing to ease of circuit design and low-power consumption. Coherent demodulation demands complex circuity and accurate reference signals, increasing power dissipation, which is avoided for WSN applications. In addition, an overview of state-of-the-art low-power receiver architectures was presented to explore the optimal receiver choice.

Table 2.1: State-of-the-art work low-power receivers.

Ref.	Arch.	Power (μW)	Data Rate (Mbps)	Sensitivity (dBm)	Scheme	Energy/Bit (pJ/b)	Tech. (nm)	Year
[50]	UIF	52	0.1	-72	OOK	520	90	2009
[51]	UIF	100	0.05	-55	OOK	2000	180	2013
[52]	TRF	500	1	-37	OOK	500	180	2007
[53]	TRF	65	0.1	-56	OOK	650	90	2007
[54]	SR	400	2	-95	OOK	200	180	2010
[55]	SR	320	1	-87	OOK	320	40	2016
[56]	SR	400	0.005	-100	OOK	80000	-	2005
[57]	SR	2800	0.5	-90	OOK	5600	130	2007
[59]	ILO	45	0.312	-62	FSK	145	180	2015
[60]	ILO	39	0.2	-55	FSK	195	130	2012
[61]	ILO	639	8	-78	FSK	80	130	2015
[62]	ILO	54	0.2	-80	OOK/FSK	270	180	2016
[63]	ILO	420	5	-73	FSK	84	180	2011

Table 2.1 summarizes state-of-the-art work of non-coherent low-power receiver architectures. Observing that the uncertain-IF (UIF) and tuned-RF (TRF) are limited in

sensitivity and data rates. On the contrary, the super-regenerative (SR) and the injection-locked based (ILO) receivers attain excellent performance, with the latter achieving enhanced energy-efficieny with minimal E_b. Also, the ILO receiver enables dual OOK and FSK demodulation, enabling further functionality. The main challenge however of the ILO based receiver is the narrow lock range, demanding further investigation to improve sensitivity performance. Nonetheless, the ILO architecture is the strongest choice to design the sub-mW multi-band receiver.

Chapter 3

Injection-Locked LC Oscillator

In this chapter a comprehensive analysis of injection-locking in LC oscillators is presented. It begins with a discussion on the fundamentals of LC oscillators, followed by mathematical descriptions describing the lock range. Also, the relationship between an incident frequency applied to the injection-locked oscillator and its corresponding output voltage is presented to illustrate the frequency-to-amplitude conversion property. Next, a model to gain insight into the relationship between the nonlinear coefficients of the injection transistor and the lock range regarding superharmonic injection is demonstrated. Following is a discussion of transistors operating in the weak and strong inversion region to demonstrate through simulations the optimal biasing point to attain a wide lock range for divide-by-4 superharmonic injection. Lastly, the chapter is summarized. Section 3.1 discusses LC cross-coupled oscillators. Section 3.2 discusses injection-locking oscillators. Next, section 3.3 discusses superharmonic injection-locking. In section 3.4, transistors operating in the weak and strong inversion region are discussed. In section 3.5, simulations are demonstrated. Lastly, section 3.6 summarizes this chapter.

3.1 LC Cross-Coupled Oscillators

An oscillator generates a continuous periodic signal without the need of an external input. This is accomplished based on positive-feedback, in which the oscillating loop operates in a regenerative manner, experiencing sustained growth. To initialize indefinite growth, the

oscillator requires a set of startup conditions which can be acquired using a linear negative-feedback model as shown from Fig. 3.1. With the closed-loop transfer function given as

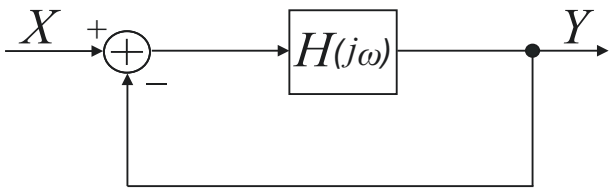


Figure 3.1: Feedback view of oscillator.

$$\frac{Y}{X}(j\omega) = \frac{H(j\omega)}{1 + H(j\omega)}, \tag{3.1}$$

the phase and loop gain requirements for sustained oscillation can be determined. Consider that when a frequency at ω_{osc} causes $H(s = j\omega_{osc})$ to equal -1, the signal passing through $H(j\omega)$ experiences a 180° phase shift and the loop gain goes to infinity causing the circuit to amplify its own noise component at ω_{osc}. Therefore, as the signal returns back to the input of the subtractor, the resulting waveform is given as the sum of the original waveform and an inverted copy, thus growing in amplitude. The oscillator continues growth until it experiences limitations imposed by circuit nonlinearities. These conditions for oscillation are known as the "Barkhausen criteria" and are given as

$$\begin{aligned} |H(j\omega_{osc})| &\geq 1 \\ \angle H(j\omega_{osc}) &= 180^\circ. \end{aligned} \tag{3.2}$$

Since the subtractor produces an additional 180° to the signal, it can also be stated that the total phase shift around the loop must be an integer multiple of 2π. In addition, attributed to circuit PVT, the loop gain is chosen greater than 1.

An ideal LC oscillator consists of a parallel connection between an inductor and capacitor which exchanges energy in the form of an electric and magnetic field to produce

a continuous periodic signal. However, practical components exhibit unwanted parasitics, dissipating energy in the form of heat, causing a decaying signal. Therefore, an active element is required to replenish the signal. This can be realized from the simplified one-port view of a LC oscillator as shown in Fig. 3.2. The loss resistance R_p models all unwanted parasitic resistances from L and C, and an active transconductor $-G_m$ is inserted which contains negative conductance to cancel out the loss effects from R_p. The resonant frequency is determined when the impedance of L and C are equivalent, $\omega_{osc}C = \frac{1}{\omega_{osc}L}$, and hence $\omega_{osc} = 1/\sqrt{LC}$. As a result, the reactive components *look* like an open circuit and the oscillator produces a continuous voltage V_{osc}.

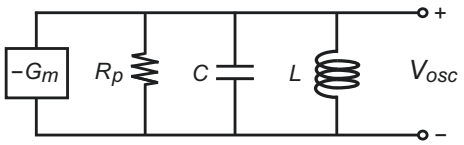


Figure 3.2: One-port view of LC oscillator.

The most popular circuit to realize the model of Fig. 3.2 using MOSFET devices for RF applications is the cross-coupled oscillator as shown in Fig. 3.3, mainly attributed to its excellent phase noise properties.

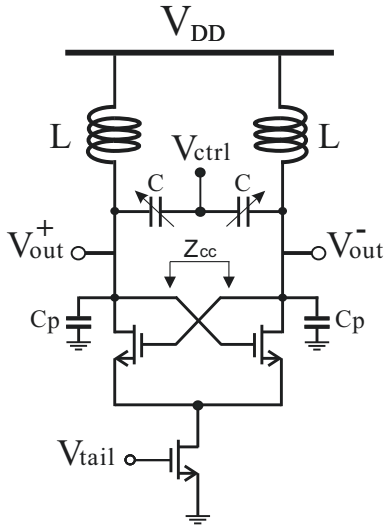


Figure 3.3: Cross-coupled oscillator.

The cross-coupled transistor pair forms the active transconductor with an impedance Z_{cc} of approximately equal to $-\frac{2}{g_m}$ compensating the loss resistance R_p from the LC tank. The tail transistor is used to supply and set the DC biasing current. The resonance frequency is given as $\omega_{osc} = \frac{1}{\sqrt{L(C+C_p)}}$, where L is the inductance, C_p is the transistors parasitic capacitance and C is the capacitance from the varactor diode. The varactor diode is used to tune the center frequency of the oscillator, in which the differential output voltages can be expressed as a frequency-modulated signal, given as [64]

$$V_{out}(t) = A(t)\sin(\omega_o t + k_{VCO}\int_0^t V_{ctrl}(\tau)d\tau), \tag{3.3}$$

where A is the peak amplitude of the output voltage, V_{ctrl} is the control voltage, k_{VCO} is the tuning gain or sensitivity equal to $\frac{dV_{ctrl}}{d\omega}$, and ω_o is the center frequency. To determine the transfer function between nodes V_{out}^+ and V_{out}^-, consider removing the connection between one of the gate to drain nodes and observing that the cross-coupled oscillator can be realized as two cascaded LC tuned stages. The voltage gain of the first stage can be expressed as

$$G_1(j\omega) = -g_{m1}Z_{out} = -g_{m1}\big[\frac{1}{\frac{1}{R_p} + j\omega C - \frac{j}{\omega L}}\big]. \tag{3.4}$$

Similarly, the voltage gain between the second stage is expressed as

$$G_2(j\omega) = -g_{m2}Z_{out} = -g_{m2}\big[\frac{1}{\frac{1}{R_p} + j\omega C - \frac{j}{\omega L}}\big]. \tag{3.5}$$

With the cross-coupled transistor pair equivalent in size, $g_{m1} = g_{m2} = g_m$. We now have

$$G(j\omega) = G_1(j\omega)G_2(j\omega) = \big[\frac{-g_m}{\frac{1}{R_p} + j\omega C - \frac{j}{\omega L}}\big]^2. \tag{3.6}$$

Recognizing that at resonance, $\omega C = \frac{1}{\omega L}$, Eq. (3.6) simplifies to

$$G(j\omega) = (g_m R_p)^2. \tag{3.7}$$

Thus, $(g_m R_p)^2$ must be greater than or equal to 1 to satisfy the loop gain requirement of the Barkhausen criteria for sustained oscillation. The phase condition is met by the cross-coupled transistor pair both producing a 180° phase shift due to the signal inversion property between the gate and drain, creating a total phase shift of 360° around the loop.

3.2 Injection-Locking Techniques

Injection-locking is a natural phenomenon that occurs when a free-running oscillator is perturbed by a periodic signal at a nearby frequency, causing the free-running frequency of the oscillator to shift to the frequency of the incident signal. The incident signal is termed as the injection signal and the associated frequency is defined as the injection frequency. In the following, we will use the LC cross-coupled oscillator to demonstrate and analyze the injection-locking behaviour. First, consider the magnitude and phase response of RLC tank circuit as shown in Fig. 3.4.

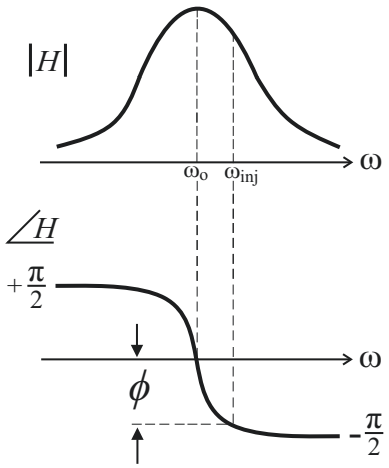


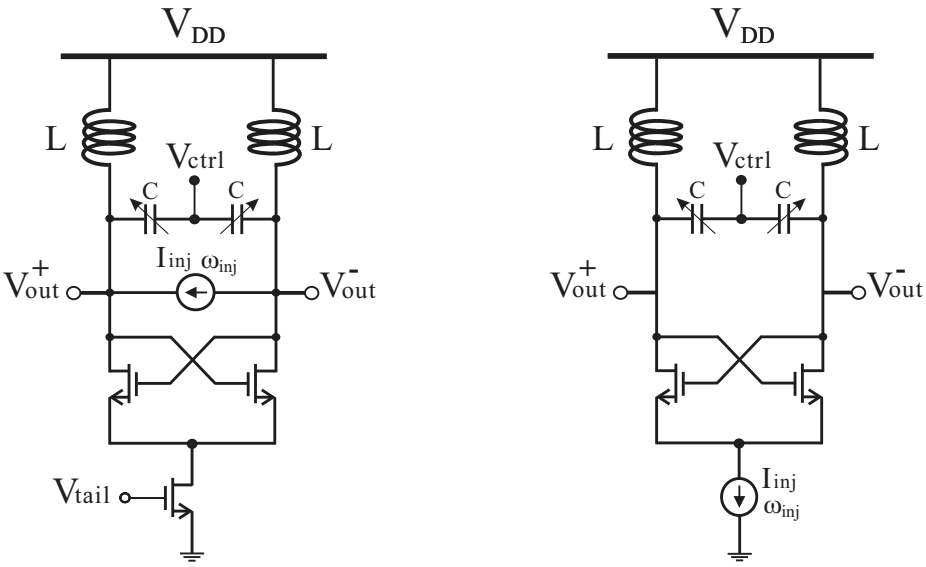
Figure 3.4: Tank circuit magnitude and phase response under injection.

The tank circuit is initially oscillating at a frequency of ω_o and the total phase shift around the loop is 0° or 360°, satisfying the Barkhausen criteria. Now, suppose that the oscillator is perturbed by an incident signal operating at an alternative frequency denoted as ω_{inj}. The incident signal will induce an additional phase shift of ϕ within the loop, causing the

oscillator to no longer oscillate at ω_o since the phase shift deviates away from 360°, failing to meet the Barkhausen criteria. If the tank circuit can compensate the additional phase shift of ϕ such that the Barkhausen criteria is satisfied, the oscillator shifts the free-running frequency to ω_{inj} and injection-locking is achieved. The range of frequencies relative to the free-running frequency that satisfies the injection-locking condition, fall into what is referred to as the lock range, e.g., $\omega_o \pm \omega_L$. In addition to frequencies nearby the free-running frequency, harmonic signals with frequencies of integer N multiples of ω_o can also achieve injection-locking. Superharmonic injection-locking occurs when the frequency of the incident signal is operating at $N\omega_o$, where N = 2, 3, 4, etc. As a result, the oscillator performs frequency division. Similarly, subharmonic injection-locking occurs if N = $\frac{1}{2}$, $\frac{1}{3}$, $\frac{1}{4}$, etc, of the free-running frequency, performing frequency multiplication. Alternatively, if the frequency of the incident signal applied to the oscillator is located outside of the lock range, the oscillator experiences an unwanted amplitude modulated effect, referred to as injection-pulling. Injection-pulling is strongly avoided and requires special care to avoid in application use.

Fig. 3.5 illustrates two injection-locking techniques towards the cross-coupled LC oscillator. Fig. 3.5(a) is referred to as direct injection, where an incident current or voltage with a frequency of ω_{inj} is imposed directly in the drain node of the cross-coupled transistor pair. Fig. 3.5(b) demonstrates another possible injection node located at the source node of the cross-coupled pair, referred to as tail injection, commonly adopted in the injection-locked oscillator. However, it is trivial to bring the incident signal through the tail transistor because it imposes a larger load effect to the source of the injection signal and requires special design attention of the drain node of the tail transistor to improve the injection efficiency. On the other hand, direct injection enhances the injection efficiency by directly coupling the incident signal at the same nodes shared with the LC tank circuits. In this thesis, we focus on direct injection to explore the behaviour of the injection locking oscillator and the subsequent design techniques in the wireless receiver.

Also, with the increasing demand for low-power high-reliable transceivers, injection-locked oscillators are becoming increasingly common, utilized for ASK and FSK demodula-



(a) Direct injection. **(b)** Tail injection.

Figure 3.5: Injection techniques.

tion. This is attributed to the oscillator's ability to convert a frequency modulated signal to an amplitude modulated signal and fast locking time. Following this section is an in-depth investigation of frequency-to-amplitude conversion associated with the lock range and other parameters that affect the lock range and consequently the amplitude of the oscillator is exploited. First, the expressions describing the transfer function and phase of a second-order parallel tank circuit are determined as they are necessary for the subsequent analysis required to describe the injection-locking mechanism. The impedance of a parallel RLC tank circuit is given as

$$Z(j\omega) = \frac{1}{\frac{1}{R_p} + \frac{1}{j\omega L} + j\omega C}. \tag{3.8}$$

With $\omega_o = 1/\sqrt{LC}$, we have

$$Z(j\omega) = \frac{1}{\frac{1}{R_p} + \frac{j}{\omega L}(\frac{\omega^2 - \omega_o^2}{\omega_o^2})}. \tag{3.9}$$

Given that $Q = \frac{R_p}{wL}$, we can further simplify to

$$Z(j\omega) = \frac{R_p}{1 + jQ(\frac{\omega^2 - \omega_o^2}{\omega_o^2})}. \tag{3.10}$$

The term $\frac{\omega^2 - \omega_o^2}{\omega_o^2}$ can be linearized around ω_o using a Taylor series expansion. Hence, we find the following expressions

$$f(\omega) \approx f(\omega_o) + \frac{df}{d\omega}(\omega - \omega_o). \tag{3.11}$$

Given that

$$f(\omega_o) = 0, \tag{3.12}$$

and with

$$\frac{df}{d\omega}(\omega - \omega_o) = \frac{d(\frac{w^2 - w_o^2}{w_o^2})}{d\omega}(\omega - \omega_o) = \frac{2}{\omega_o}(\omega - \omega_o), \tag{3.13}$$

we can rewrite the impedance as

$$Z(j\omega) \approx \frac{H_o}{1 + j2Q(\frac{w - w_o}{w_o})}, \tag{3.14}$$

with $H_o = R_p$. Therefore, the transfer function is expressed as

$$H(j\omega) = \frac{V_o}{I_{in}} = Z(j\omega) = \frac{H_o}{1 + j2Q(\frac{w - w_o}{w_o})}. \tag{3.15}$$

Next, the phase shift α can be determined using the relationship that

$$\alpha = \tan^{-1}\left(\frac{\mathrm{Im}(Z(j\omega))}{\mathrm{Re}(Z(j\omega))}\right) = \tan^{-1}\left(\frac{-\frac{2R_pQ(\frac{\omega - \omega_o}{\omega_o})}{1+4Q^2(\frac{\omega-\omega_o}{\omega_o})^2}}{\frac{R_p}{1+4Q^2(\frac{\omega-\omega_o}{\omega_o})^2}}\right). \tag{3.16}$$

Arriving at

$$\alpha = \tan^{-1}\left(\frac{2Q(\omega_o - \omega)}{\omega_o}\right). \tag{3.17}$$

If a phase modulated signal is traveling through a tank circuit, ω can be replaced with $\omega + \frac{d\phi}{dt}$, given as the instantaneous frequency. We now have

$$\alpha = \tan^{-1}\left(\frac{2Q(\omega_o - \omega - \frac{d\phi}{dt})}{\omega_o}\right). \tag{3.18}$$

With the expressions acquired describing the phase and the transfer function of the tank circuit, we now follow the steps from [65] to examine the frequency-to-amplitude conversion property by considering the oscillator under injection, modelled in Fig. 3.6. The goal here is to compute the voltage V_a and apply it to the phase shift of the tank circuit then equate the result to V_{out}. The free-running oscillator is operating at a frequency of ω_{osc}, with a peak voltage of V_{osc}. Now, suppose that an incident signal with a frequency of ω_{inj} and peak voltage of V_{inj} is applied and the oscillator experiences injection locking. With the voltage V_a given as

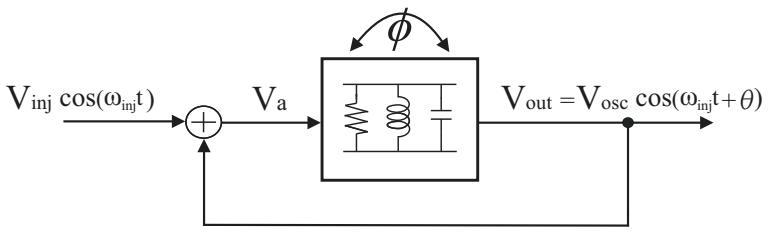


Figure 3.6: *LC* oscillator under injection.

$$V_a = V_{inj}\cos(\omega_{inj}t) + V_{osc}\cos(\omega_{inj}t + \theta). \tag{3.19}$$

This can be expanded as

$$V_a = (V_{inj} + V_{osc}\cos(\theta))\cos(\omega_{inj}t) - V_{osc}(\sin(\omega_{inj}t)\sin(\theta)). \tag{3.20}$$

The signal V_a must be converted into a single sinusoidal before applying it to the phase shift of the tank circuit because superposition theorem does not hold. Therefore, we use the definition of

$$\tan(\phi) = \frac{V_{osc}\sin(\theta)}{V_{inj} + V_{osc}\cos(\theta)}, \tag{3.21}$$

and by factoring $V_{inj} + V_{osc}\cos(\theta)$, we have

$$V_a = \frac{V_{inj} + V_{osc}\cos(\theta)}{\cos(\phi)}\cos(\omega_{inj}t + \phi). \tag{3.22}$$

With $\cos(\phi) = \frac{1}{\sqrt{1+\tan^2(\phi)}}$, V_a can now be converted to a single sinusoidal and be subjected to the phase shift of the tank. Therefore,

$$V_a = \sqrt{V_{inj}^2 + V_{osc}^2 + 2V_{inj}V_{osc}\cos(\theta)}\cos(\omega_{inj}t + \phi). \tag{3.23}$$

Using the phase shift expression in Eq. (3.18) derived earlier, V_{out} is given as

$$V_{out} = A \times \cos(\omega_{inj}t + \phi + \tan^{-1}\big[\frac{2Q}{\omega_{osc}}(\omega_{osc} - \omega_{inj} - \frac{d\phi}{dt})\big]). \tag{3.24}$$

Commenting on Eq. (3.24), the frequency-to-amplitude conversion property is built once the oscillator is under injection. The output voltage after the injection-locking process is established is given as $\sqrt{V_{inj}^2 + V_{osc}^2 + 2V_{inj}V_{osc}\cos(\theta)}$ and is a function of the phase shift of the tank. As a result, the value of the output voltage varies depending on the deviation of the phase shift produced by the tank circuit. A larger deviation between the free-running frequency and injection frequency produces a larger phase shift and consequently a smaller output amplitude. Making use of this property, a frequency modulated signal can be converted to an amplitude modulated signal such that low power can be achieved in the design of

the receiver. In addition, a wider lock range apparently leads to a larger amplitude variation and as a consequence, a smaller signal can be converted.

Completing the analysis above when assuming $V_{inj} << V_{osc}$, V_{out} can be approximated as

$$V_{out} \approx V_{osc} \times \cos(\omega_{inj}t + \phi + \tan^{-1}\big[\frac{2Q}{\omega_{osc}}(\omega_{osc} - \omega_{inj} - \frac{d\phi}{dt})\big]). \tag{3.25}$$

Then by equating the result to $V_{osc}\cos(\omega_{inj}t + \theta)$, the following expression is obtained

$$\theta = \phi + \tan^{-1}\big[\frac{2Q}{\omega_{osc}}(\omega_{osc} - \omega_{inj} - \frac{d\phi}{dt})\big]. \tag{3.26}$$

Taking the time derivative of Eq. (3.21), we have

$$\frac{d\phi}{dt} = \frac{V_{osc}^2 + V_{osc}V_{inj}\cos(\theta)}{V_{osc}^2 + 2V_{osc}V_{inj}\cos(\theta) + V_{inj}^2}\frac{d\theta}{dt} \approx \frac{d\theta}{dt}. \tag{3.27}$$

Substituting Eq. (3.27) into Eq. (3.26) we arrive at

$$\tan(\theta) = \tan(\phi) + \frac{2Q}{\omega_{osc}}(\omega_{osc} - \omega_{inj} - \frac{d\theta}{dt}). \tag{3.28}$$

And with

$$\tan(\theta - \phi) \approx \frac{V_{inj}}{V_{osc}}\sin(\theta), \tag{3.29}$$

Eq. (3.28) simplifies to

$$\frac{d\theta}{dt} = \omega_{osc} - \omega_{inj} - \frac{\omega_{osc}}{2Q}\frac{V_{inj}}{V_{osc}}\sin(\theta). \tag{3.30}$$

This analysis is originally presented in [65]. Commenting on Eq. (3.30), we see that if the phase shift changes with time, e.g., $\frac{d\theta}{dt} \neq 0$, the oscillator has not established a constant

frequency, and is experiencing injection-pulling. Otherwise, if the time derivative of the phase is 0, the frequency of oscillation is constant, and the oscillator is locked. Therefore equating Eq. (3.30) to 0, we have

$$\omega_{osc} - \omega_{inj} = \omega_L = \frac{\omega_{osc}}{2Q}\frac{V_{inj}}{V_{osc}}\sin(\theta), \tag{3.31}$$

where ω_L is the single-sided lock range. Eq. (3.31) was originally derived in a similar form by Adler using an alternative method where he demonstrated that the lock range is proportional to the impressed voltage and the free-running frequency of the oscillator, and inversely proportional to the quality factor of the tank circuit and the oscillating voltage [66]. Razavi also confirmed Eq. (3.31) using a phasor domain analysis, demonstrating that the lock range can be expressed as

$$\Delta\omega = \frac{\omega_{osc}}{2Q}\frac{I_{inj}}{I_o}\frac{1}{\sqrt{1-(\frac{I_{inj}}{I_o})^2}}, \tag{3.32}$$

where I_{inj} is the injection current, and I_o is oscillating current. In the case when the oscillator is under weak injection, i.e., $I_{inj} << I_o$, Eq. (3.32) can be simplified to the following

$$\Delta\omega \approx \frac{\omega_{osc}}{2Q}\frac{I_{inj}}{I_o}. \tag{3.33}$$

Similar work confirming the expression of the lock range using alternative methods have also been demonstrated in [67, 68, 69].

In summary, we see that the lock range increases with the injection strength applied to the oscillator, and decreases at the presence of larger quality factors. We also observe that if the injected current or voltage is applied at a phase shift of a $\frac{\pi}{2}$ with respect the oscillating voltage, the maximum attainable lock range is achieved. In addition, the relationship between the output voltage and the injection frequency is shown in Eq. (3.25), revealing how a frequency modulated signal can be converted to an amplitude modulated signal via the

injection-locking mechanism. We also see how the lock range plays a key in the FSK-to-ASK conversion.

3.3 Superharmonic Injection-Locking

The above discussion focused on fundamental injection-locking, in which the injection frequency is close to the free-running frequency of the oscillator. In this section we focus on when the injected frequency is an integer multiple of the free-running frequency, i.e., $\omega_{inj} = N\omega_o$, where N = 1, 2, 3, etc. In this case, the oscillator performs frequency division. Common techniques for frequency division used digital-based techniques such as static, dynamic, or current-mode logic circuitry [70, 71, 72]. However, digital prescalers are avoided in low-power applications as they increase design complexity and power consumption. Alternatively, the analog counterparts, e.g., Miller dividers and injection-locking, offer ease of design implementation for frequency division [73, 74]. Fig. 3.7 depicts an example of a divide-by-2 ILFD.

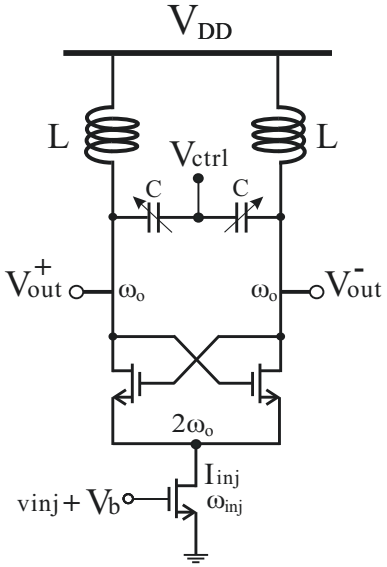


Figure 3.7: Divide-by-2 injection-locked frequency divider.

Before the incident signal is applied, the source node of the cross-coupled pair is oscillating at a frequency of $2\omega_o$. Now, suppose an AC voltage v_{inj}, operating at a frequency of ω_{inj}, that is approximately equal to $2\omega_o$, is applied to the tail transistor of the cross-coupled LC oscillator. This will create a drain-source AC current I_{inj} with a frequency of ω_{inj}. Considering that the cross-coupled transistor pair as two switching mixers, this will cause the incident signal to mix with both the fundamental and harmonic components of the oscillator at the common-source node, inducing a phase shift in the tank circuit and causing the free-running frequency ω_o to alter to $\frac{\omega_{inj}}{2}$. Thus, the oscillator took the frequency of the injected signal and divided it down by a factor of 2. This mechanism is referred to as superharmonic injection-locking and is a powerful technique to achieve low-power frequency division. However, one of the drawbacks is as the modulus increases, the lock range begins to decrease. Therefore, we now examine the lock range describing ILFDs.

Lee and Hajimiri showed that the lock range for superharmonic injection-locking can be expressed as [75]

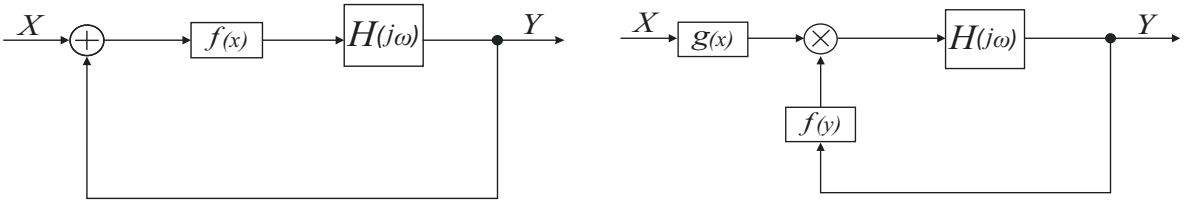
$$\Delta\omega = \frac{\omega_o}{2Q}\frac{V_{in}}{V_{osc}}H_o\left[\sum_{m=1}^{\infty} K_{m,sm\pm1} sin(m\theta)\right], \tag{3.34}$$

where $K_{m,sm\pm1}$ is the intermodulation coefficient, V_{in} is the input voltage, and V_{osc} is the oscillation voltage. Similarly, Razavi showed using a time-invariant method that the divide-by-2 lock range can be approximated as [39]

$$\Delta\omega_{div-2} \approx \frac{\omega_0}{2Q}\frac{4}{\pi}\frac{I_{inj}}{I_{osc}} \tag{3.35}$$

where $4/\pi$ is the conversion gain. From these expressions, we see that the lock range widens as the signal strength increases, and decreases as the quality factor increases, similar to the lock range describing fundamental injection. Unfortunately, these equations do not provide enough insight into the operation of the frequency divider as simulation results will start to present irregularities. We, therefore, investigate an in-depth study of models to describe the frequency division property of the superharmonic injection-locked phenomena.

Injection-locked frequency dividers (ILFDs) can be classified as either regenerative or injection-locked systems. The former requires an injected signal to produce an output and does not contain a free-running clock signal. Whereas the injection-locked model does free-run, and the oscillator locks in phase and frequency to the injected signal [76]. These models are shown in Fig. 3.8(a) and Fig. 3.8(b) respectively, where $X = I_{inj}cos(\omega_{inj}t+\theta)$ and $Y = I_{o}cos(\omega_{o}t)$. Observing that both consist of nonlinear blocks and the transfer function of the RLC resonator $H(j\omega)$. The nonlinear block ensures that the harmonic frequency components are generated for the mixing operation, and the transfer function is necessary for the filtering and the phase properties of the tank circuit.



(a) Injection-locked system. **(b)** Regenerative system.

Figure 3.8: Injection-locked frequency divider models.

Previous analysis describing the lock range for superharmonic dividers derive complex expressions that provide little to no insight between the relationship of the injection transistor and lock range. In [77], a similar regenerative model is used with the cross-coupled pair considered a multiplier and a hard switching mixer. In this work, we employ the regenerative-frequency divide model, as shown in Fig. 3.9 and treat the injection transistor as a harmonic mixer composed of a multiplier and nonlinear block. Using this approach, a relationship between the nonlinearity of the device and the lock range can be established.

Consider the injection and output current denoted as $I_{inj}\cos(\omega_{inj}t+\theta)$ and $I_{o}\cos(\omega_{o}t)$ respectively, where θ is the relative phase difference between input and output. The transfer function of the resonant is given as $H(j\omega)$, defined in Eq. (3.15). We assume that the Q of the RLC tank circuit is high enough to suppress intermodulation and harmonic components upon mixing. The nonlinear block is expressed as a polynomial series given as

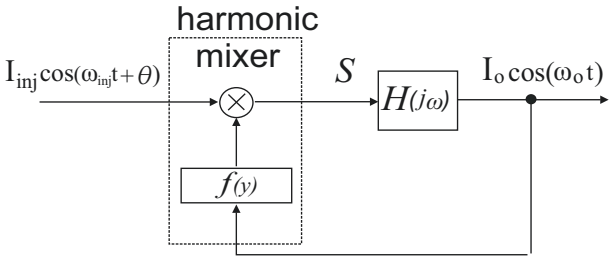


Figure 3.9: Frequency regenerative divide model.

$$f(y) = \sum_{n=0}^{\infty} \alpha_n x^n. \tag{3.36}$$

By approximating to a third-order series and applying the output to the nonlinear block, the following expression is obtained.

$$f(y) \approx \alpha_0 + \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 \tag{3.37}$$

$$f(y) \approx \alpha_0 + \alpha_1 I_o \cos(\omega_o t) + \frac{\alpha_2 I_o^2}{2}\big[1 + \cos(2\omega_o t)\big] + \frac{\alpha_3 I_o^3}{4}\big[3\cos(\omega_o t) + \cos(3\omega_o t)\big] \tag{3.38}$$

For divide-by-4 injection, we have $\omega_{inj} = 4\omega_o$. Then by multiplying Eq. (3.38) by $I_{inj}\cos(\omega_{inj}t+\theta)$, we have

$$\begin{aligned} S(j\omega) = I_{inj}\cos(4\omega_o t + \theta)\Big[\alpha_0 + \alpha_1 I_o \cos(\omega_o t) + \frac{\alpha_2 I_o^2}{2}\big[1 + \cos(2\omega_o t)\big] \\ + \frac{\alpha_3 I_o^3}{4}\big[3\cos(\omega_o t) + \cos(3\omega_o t)\big]\Big]. \end{aligned} \tag{3.39}$$

Expanding and rearranging Eq. (3.39), we have

$$S(j\omega) = I_{inj}\cos(4\omega_o t+\theta)\big[\alpha_0+\frac{\alpha_2 I_o^2}{2}\big]+I_{inj}\cos(4\omega_o t+\theta)\cos(\omega_o t)\big[\alpha_1 I_o+\frac{\alpha_3 3I_o^3}{4}\big] \\ +I_{inj}\cos(4\omega_o t+\theta)\cos(2\omega_o t)\big[\frac{\alpha_2 I_o^2}{2}+\frac{\alpha_4 4I_o^4}{8}\big]+I_{inj}\cos(4\omega_o t+\theta)\cos(3\omega_o t)\big[\frac{\alpha_3 I_o^3}{4}\big]. \tag{3.40}$$

With the resonator blocking out frequency components above and below ω_o, the only component of interest from Eq. (3.40) is

$$S(j\omega) = I_{inj}\cos(4\omega_o t+\theta)\cos(3\omega_o t)\big[\frac{\alpha_3 I_o^3}{4}\big]. \tag{3.41}$$

By multiplying Eq. (3.41) by the transfer function of the resonator and converting to the phasor domain, the output is given as

$$Y = I_{inj}e^{j(\omega_o t+\theta)}\frac{H_o}{1+j2Q\frac{\omega-\omega_o}{\omega_o}}\big[\frac{\alpha_3 I_o^3}{8}\big]. \tag{3.42}$$

Since Eq. (3.42) is equal to the phasor expression of the output current, we have

$$I_o e^{j(\omega_o t)} = I_{inj}e^{j(\omega_o t+\theta)}\frac{H_o}{1+j2Q\frac{\omega-\omega_o}{\omega_o}}\big[\frac{\alpha_3 I_o^3}{8}\big]. \tag{3.43}$$

Which can be further simplified to

$$I_o = I_{inj}e^{j\theta}\frac{H_o}{1+j2Q\frac{\omega-\omega_o}{\omega_o}}\big[\frac{\alpha_3 I_o^3}{8}\big], \tag{3.44}$$

and

$$I_o(1 + j2Q\frac{\Delta\omega}{\omega_o}) = I_{inj}e^{j\theta}H_o[\frac{\alpha_3 I_o^3}{8}]. \tag{3.45}$$

Using the identity that

$$e^{jx} = \cos(x) + j\sin(x), \tag{3.46}$$

and equating to the imaginary part of Eq. (3.45), we have

$$I_o 2Q\frac{\Delta\omega}{\omega_o} = H_o \times I_{inj}\sin(\theta) \times \left[\frac{\alpha_3 I_o^3}{8}\right]. \tag{3.47}$$

Solving for $\Delta\omega$, we arrive at

$$\Delta\omega_{div-4} = \frac{\omega_o}{2Q}\frac{I_{inj}}{I_o}H_o\frac{\alpha_3 I_o^3}{8}\sin(\theta). \tag{3.48}$$

Similarly, by performing the same analysis when the injection frequency is equal to $\omega_{inj} = 2\omega_o$, we have

$$\Delta\omega_{div-2} = \frac{\omega_o}{2Q}\frac{I_{inj}}{I_o}H_o\sin(\theta)\left[\frac{\alpha_3 I_o^3}{2} + \frac{\alpha_1 I_o}{2}\right]. \tag{3.49}$$

And if $\omega_{inj} = 3\omega_o$, we also have

$$\Delta\omega_{div-3} = \frac{\omega_o}{2Q}\frac{I_{inj}}{I_o}H_o\sin(\theta)\frac{\alpha_2 I_o^2}{4}. \tag{3.50}$$

Defining η as

$$\eta = \frac{\omega_o}{2Q}\frac{I_{inj}}{I_o}H_o\sin(\theta), \tag{3.51}$$

and summarizing the above lock range expressions, we have

- Divide By 2:

$$\Delta\omega_{div-2} = \eta(\frac{\alpha_3 I_o^3}{2} + \frac{\alpha_1 I_o}{2})$$

- Divide By 3:

$$\Delta\omega_{div-3} = \eta\frac{\alpha_2 I_o^2}{4}$$

- Divide By 4:

$$\Delta\omega_{div-4} = \eta\frac{\alpha_3 I_o^3}{8}$$

Commenting on the expressions previously derived, we see that the lock range can be widened by increasing the signal strength and decreasing the quality factor of the tank circuit. Additionally, the case for divide-by-3, the lock range is proportional to the second-order coefficient. However, due to the symmetrical properties of the cross-coupled LC oscillator, the second-order coefficient is approximately zero, suggesting a small lock range. Alternatively, the lock range for divide-by-2 and divide-by-4 is proportional to the third-order coefficient. We also see that the divide-by-2 lock range is proportional to the first-order coefficient. In general, the first-order coefficient is much larger than the non-linear coefficients in a mild non-linear system. Therefore, α_3 exhibits less impact on the lock range of divide-by-2. It is more efficient to increase α_1 to widen the lock range rather than altering α_3 in divide-by-2. On the other hand, in divide-by-4, α_3 influences the lock range directly. An in-depth analysis is given in the next chapter.

So far, we have exploited the locking behaviour of fundamental injection-locking and superharmonic injection-locking. The lock range affects the ability of FSK-to-ASK conversion, which means a wider lock range leads to a more efficient frequency to amplitude conversion. Due to the nature of the differential configuration of the circuit, the small lock range from divide-by-3 is not useful for the receiver. We will demonstrate by making use of fundamental injection, divide-by-2 and divide-by-4, OOK and FSK signals in multi-bands can be demodulated through a single LC oscillator.

Additionally, consider that the receiver detects a signal with small input power. The LNA stage must amplify the received signal at a sufficient amplitude for the injection-locked oscillator to lock to the incident frequency. If the signal is not large enough in magnitude, the oscillator will start experiencing injection-pulling. Thus, there is a direct relationship between the lock range of the oscillator and the highest attainable sensitivity of the receiver. Since we have obtained these alternative equations describing new insights to enhance the lock range for divide-by-2 and divide-by-4 injection, we can now investigate techniques to improve the performance of the receiver design that does not rely solely on increasing the strength of the incident signal. Therefore, the following section provides an examination of the transistors operating in the weak and strong inversion region to investigate the nonlinear properties of transistors.

3.4 Transistors in Weak and Strong Inversion

In this section, a study of transistors operating in the weak and strong inversion is performed to demonstrate optimum biasing techniques for the injection transistor to enlarge the lock range for divide-by-4 operation. This will allow us to process the FSK modulated signal at the high-frequency band while the LC oscillator is designed in the lower GHz range.

When a transistor operates with a gate-source voltage V_{gs}, that is smaller than the threshold voltage V_{th}, the device exhibits severe nonlinear characteristics. The region of operation is referred to as the weak inversion or subthreshold region, with a drain-source current expressed as [78]

$$I_{ds,sub} = I_{d0} e^{\frac{Vgs - V_{th}}{n\phi_t}} (1 - e^{\frac{-V ds}{\phi_t}}), \tag{3.52}$$

where

$$I_{d0} = 2\mu_n C_{ox} n \phi_t^2 \frac{W}{L}. \tag{3.53}$$

Here, V_{ds} is the drain-source voltage, W is the width of the device, L is length of the channel, μ_n is the surface mobility of the electrons in the NFET, C_{ox} is the gate-oxide capacitance per unit area, n denotes the subthreshold slope, and ϕ_t is the thermal voltage given as $\frac{kT}{q}$. Further, k is Boltzmann's constant and q is the electron charge with values of 1.38×10^{-23} J/K and 1.6×10^{-16} C respectively. T is absolute temperature in degrees Kelvin. If the drain-source voltage is larger than $3\phi_t \approx 78mV$ (at room temperature), the term of $e^{\frac{-V_{ds}}{\phi_t}}$ in Eq. (3.52) can be neglected. Therefore, we can simplify Eq. (3.52) to

$$I_{ds,sub} = I_{d0} e^{\frac{V_{gs}-V_{th}}{n\phi_t}}. \tag{3.54}$$

Recall that the small-signal drain-source current of a MOSFET can be expressed as a third-order Taylor series denoted by

$$I_{ds} = g_m V_{gs} + \frac{g'_m}{2!} V_{gs}^2 + \frac{g''_m}{3!} V_{gs}^3, \tag{3.55}$$

where V_{gs} is the small-signal gate-to-source voltage and the coefficients are given by $g_m = \partial I_{ds}/\partial V_{gs}$, $g'_m = \partial^2 I_{ds}/\partial V_{gs}^2$ and $g''_m = \partial^3 I_{ds}/\partial V_{gs}^3$. Computing the first, second, and third-order derivative of Eq. (3.54), we have the following coefficients

$$g_m = \frac{I_{d0}}{n\phi_t} e^{\frac{V_{gs}-V_{th}}{n\phi_t}}, \tag{3.56}$$

$$g'_m = \frac{I_{d0}}{(n\phi_t)^2} e^{\frac{V_{gs}-V_{th}}{n\phi_t}}, \tag{3.57}$$

$$g''_m = \frac{I_{d0}}{(n\phi_t)^3} e^{\frac{V_{gs}-V_{th}}{n\phi_t}}. \tag{3.58}$$

Observing that Eq. (3.58) is positive in the weak inversion region, resulting in gain expansion. Alternatively, the drain-source current of a transistor operating in the strong inversion region can be expressed as [78]

$$I_{ds,n} = \frac{1}{2}\frac{W_n}{L_n}\mu_0 C_{ox}\frac{(V_{gs}-V_{th,n})^2}{1+(\frac{\mu_0}{2v_{sat}L_n}+\theta_{sat})(V_{gs}-V_{th,n})}, \tag{3.59}$$

where μ_0 is the mobility, v_{sat} is the saturation velocity, and θ_{sat} is a fitting parameter. The expressions for the first, second, and third-order coefficients can also be determined after computing the necessary derivative. Arriving at

$$g_{mn} = \frac{C_{ox}W_n\mu_0 v_{sat}(V_{gs}-V_{thn})(4L_n v_{sat}+(V_{gs}-V_{thn})(\mu_0+2L_n\theta_{sat}v_{sat}))}{(2L_n v_{sat}+(V_{gs}-V_{thn})(\mu_0+2L_n\theta_{sat}v_{sat}))^2}, \tag{3.60}$$

$$g'_{mn} = \frac{8W_n L_n^2\mu_0 C_{ox}v_{sat}^3}{(2L_n v_{sat}+(V_{gs}-V_{thn})(\mu_0+2L_n\theta_{sat}v_{sat}))^3}, \tag{3.61}$$

$$g''_{mn} = -\frac{24W_n L_n^2\mu_0 C_{ox}v_{sat}^3(\mu_0+2L_n\theta_{sat}v_{sat})}{(2L_n v_{sat}+(V_{gs}-V_{thn})(\mu_0+2L_n\theta_{sat}v_{sat}))^4}. \tag{3.62}$$

Observing that the third-order coefficient in the strong inversion is negative, resulting in gain compression.

It is well known that the transistor in the weak inversion exhibits more severe non-linearity than in the strong inversion. This is illustrated in Fig. 3.10, depicting the simulated third-order nonlinear coefficient of BSIM4 models versus the gate-source voltage. The threshold voltage of the device is approximately 405 mV, located at the zero crossing. When V_{gs} << 405 mV, the transistor is operating in weak inversion, and when $V_{gs} \sim$ 405 mV, the transistor is operating in the moderate inversion region. Whereas, when V_{gs} >> 405 mV, the transistor is operating in the strong inversion region. Observing that large positive peak is located in weak inversion region with a V_{gs} of 345 mV, compared to the negative peak in strong inversion region. We thus conclude that an optimum biasing point, resulting in larger third-order non-linear coefficient and subsequent wider lock range for divide-by-4, is located in the weak inversion region.

However, we can further increase the coefficient via triple-well CMOS process since the transistor is a four terminal device with the threshold voltage defined as [79]

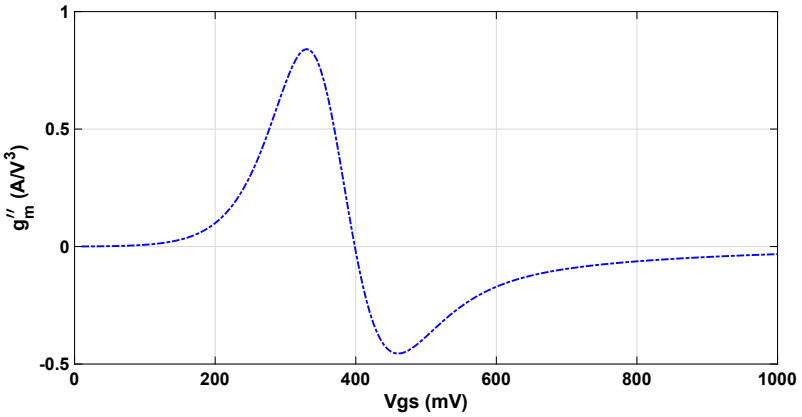


Figure 3.10: Third-order nonlinear coefficient vs. V_{gs}, with transistor W = 45 μm and L = 180 nm.

$$V_{th} = V_{t0} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}). \tag{3.63}$$

Where V_{t0} is the threshold voltage when the source and body are at the same potential, ϕ_s is the surface potential at the threshold, and γ is the body effect coefficient. Although, before arbitrarily selecting a body biasing voltage, the device model is reviewed. Fig. 3.11 depicts a simplified structure of a triple-well NFET.

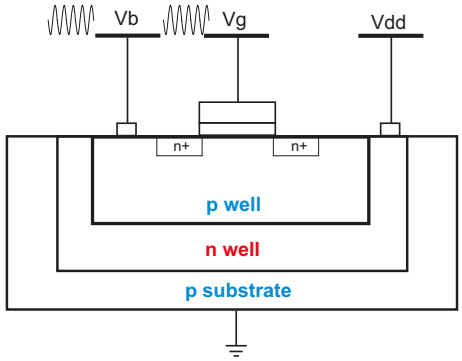


Figure 3.11: Simplified structure of triple-well NFET.

For low supply voltage designs, e.g., 0.7 V, the value of V_b should be chosen such that a forward biased diode is not formed between the p-well and n-well. Furthermore, if the injected signal is applied to the body terminal such that

$$V_b = V_B + V_a \cos(\omega_{inj} t), \tag{3.64}$$

the injection power is increased, suggesting an increase in the lock range. Fig. 3.12 illustrates the third-order nonlinear coefficient versus V_{gs} for various body biasing voltages and observing that the coefficient increases as the body bias voltage increases.

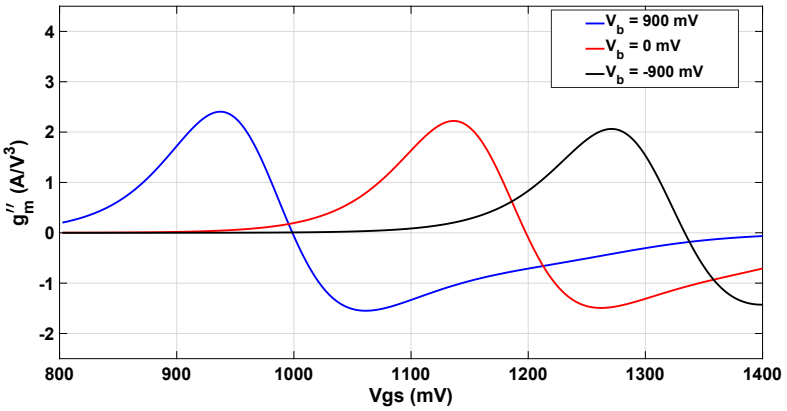


Figure 3.12: Third-order nonlinear coefficient vs. V_{gs}.

3.5 Simulations

In this section we simulate the injection-locking cross-coupled LC oscillator using Cadence tools to observe the frequency-to-amplitude conversion after the locking condition is satisfied and compare the lock range when the injection transistor is operating in both the weak and strong inversion region.

Fig. 3.13 depicts the simulated transient response of a cross-coupled LC oscillator operating at a free-running frequency of 982 MHz with an applied 50 mVp signal of 985

MHz injected at 2 ns. Observing the oscillator locking to the incoming signal and the output voltage remains constant with time. We also see a slight decrease in the output voltage upon locking, confirming the frequency-to-amplitude conversion property. In addition, the frequency of the oscillator is measured versus time to illustrate the fast locking procedure achieved by the oscillator. In this example, the oscillator took approximately 400 ps to complete the locking procedure.

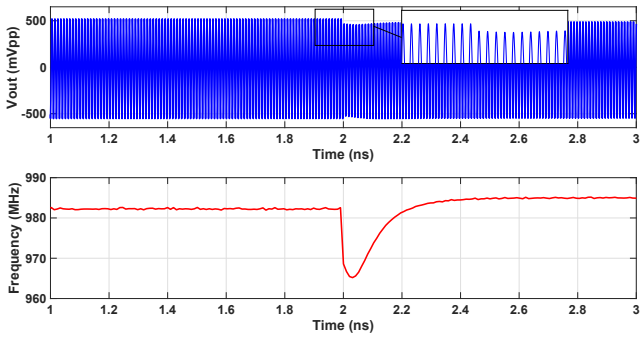


Figure 3.13: Injection-locking transient response.

Fig. 3.14 depicts the transient response of the unwanted effect of injection-pulling. Observing the amplitude of the output voltage varies with time after the injected signal is applied at 2 ns operating at 995 MHz, located outside the lock range. Similarly, the frequency is not constant versus time..

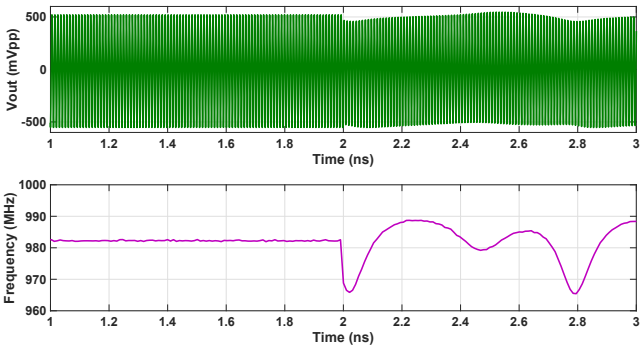


Figure 3.14: Injection-pulling transient response.

To confirm the optimal biasing point of the ILFD for divide-by-4 injection, the circuit as shown in Fig. 3.15 is designed in GF 130 nm 1.2 V CMOS technology. The tuning range is from 766 MHz to 1.66 GHz as V_{ctrl} varies from 0 V to 2.6 V. For testing purposes, the circuit is tuned to resonate at a center frequency of 1 GHz. Transistor M_4 is treated as a harmonic mixer with the injected signal v_{inj} applied directly to the common-drain nodes, i.e., direct injection. The biasing voltage V_g varies to alter the nonlinearity characteristics of the harmonic mixer.

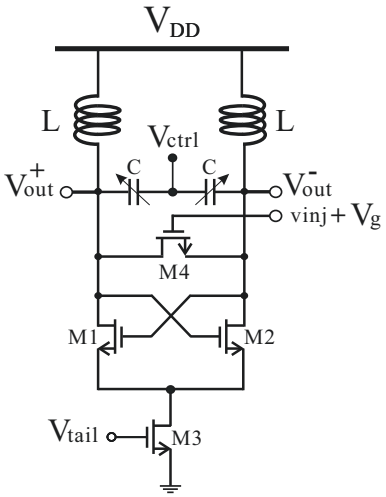


Figure 3.15: Schematic of injection-locked frequency divider. Circuit parameters: $W_{1,2} = 35$ μm, $W_3 = 40$ μm, $W_4 = 25$ μm, $L_{1,2,3,4} = 180$ nm, $V_{tail} = 0.65$ V, $V_{DD} = 1.2$ V, L = 6.2 nH, C = 1.082 - 5.5 pF.

Fig. 3.16 depicts the lock range for the divide-by-4 injection of the oscillator versus the applied injection power to the oscillator. Observing that a V_{gs} of 345 mV, i.e., V_g - V_{DD}, results in a larger lock range as opposed to a V_{gs} of 475 mV when the transistor is operating in the strong inversion region. Confirming that divide-by-4 injection exhibits a larger lock range when the transistor is biasing in the weak inversion region.

To acquire the optimal biasing point, the gate voltage V_g is altered and the lock range is measured. Fig. 3.17 depicts the divide-by-4 lock range versus V_{gs} for various input powers. Observing that the divide-by-4 lock range emulates the third-order nonlinear coefficient

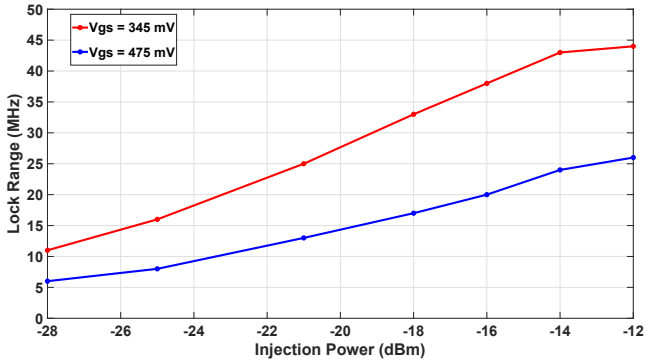


Figure 3.16: Simulated divide-by-4 lock range versus injection-power.

curve, with the optimal biasing condition attained at the peak curve with a V_{gs} of 345 mV. Therefore, this confirms the discovering of an optimal biasing point for divide-by-4 injection.

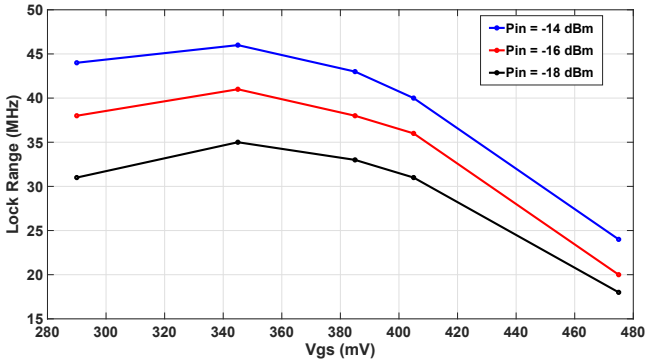


Figure 3.17: Simulated divide-by-4 lock range versus V_{gs}.

Fig. 3.18 depicts the divide-by-2 lock range versus injection power. Since the divide-by-2 lock range is proportional to the first and third-order coefficients, we see a wider lock range is attained when the harmonic mixer is operating in the strong inversion region. This is because the first-order coefficient is dominant. However, when biased at the peak third-order V_{gs}, the divide-by-2 lock range is larger than the divide-by-4 lock range since the coefficient is associated with a larger factor.

Fig. 3.19 depicts the divide-by-4 ILFD with a triple-well NFET device as the harmonic mixer. In this simulation, we inject an AC signal directly into the gate and p-well of the

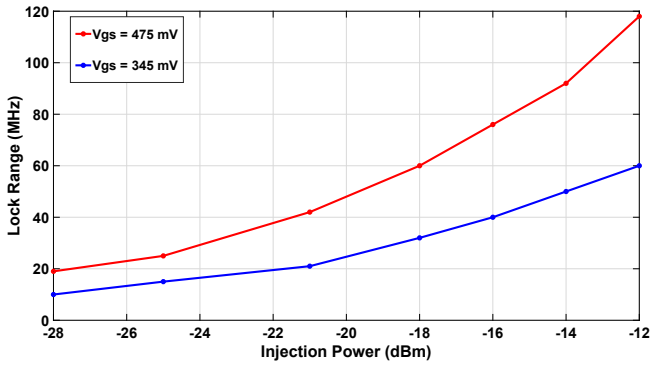


Figure 3.18: Simulated divide-by-2 lock range versus injection-power.

device. We will then alter the body bias voltage V_b to change the threshold of the device, which will vary the magnitude of the third-order nonlinear coefficient. As we vary V_b, we modify the gate voltage V_g such that it is placed at the peak of the third-order nonlinear coefficient. A transient analysis is then performed to measure the lock range.

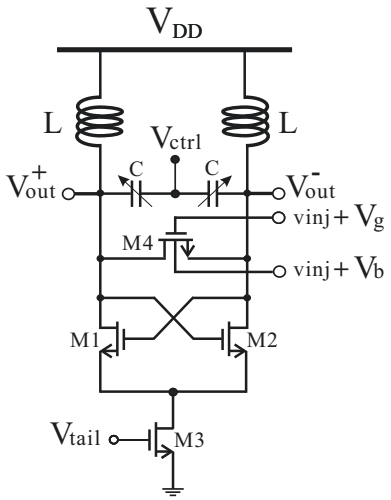


Figure 3.19: Schematic of injection-locked frequency divider with triple-well NFET. Circuit parameters: $W_{1,2}$ = 60 μm, W_3 = 85 μm, W_4 = 95 μm, $L_{1,2,3,4}$ = 120 nm, V_{tail} = 0.46 V, V_{DD} = 0.7 V, L = 22 nH, C = 1.34 - 6.85 pF.

As depicted in Fig. 3.20, we see that the lock range increases substantially as the body bias voltage increases. Noting that as V_b = 1.7 V, 1.5 V, 900 mV, 400 mV, 0 V, -400 mV, and -900 mV, we adjust V_g = 750 mV, 830 mV, 935 mV, 1.05 V, 1.14 V, 1.2 V, and

1.27 V respectively to ensure optimal biasing. The original lock range is 34 MHz with V_b = 0, and as we increase V_b to 1.2 V, the lock range reaches a value of 55 MHz. We also note that with V_b = 1.2 V, the forward bias voltage between the p-well and n-well is 0.5 V. However, as the body bias voltage reaches a value of approximately 1.5 V, the lock range decreases. This is because the forward voltage across the p-well and n-well form a forward biased diode, degrading the performance of the device. We can assume that the body bias voltage between the p-well and n-well should not exceed 0.7 V. Therefore, when designing the receiver, a reasonable body bias voltage is selected to avoid this effect.

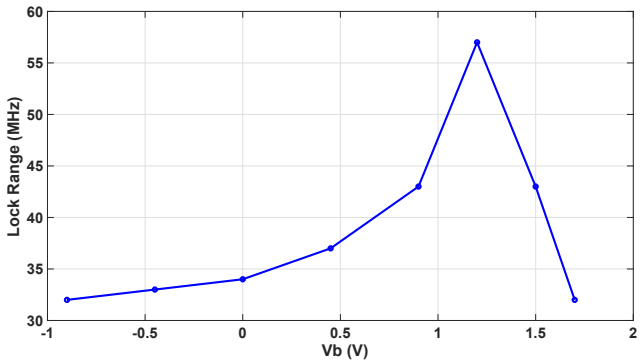


Figure 3.20: Simulated divide-by-4 lock range versus body bias voltage with Pin = -20 dBm.

3.6 Summary

This chapter presented an overview of injection-locked LC oscillators. Discussing the theory of the lock range and the frequency-to-amplitude conversion property. In addition, superharmonic injection-locking is presented with a mathematical description of the lock range derived using the regenerative frequency divide model. The model treats the injection transistor as a harmonic mixer composed of a pure multiplier and nonlinear block. This provides insight between the dependency of the nonlinear coefficients of the device and the lock range. It was shown that the divide-by-4 lock range depends on the third-order nonlinear coefficient. As a result, the divide-by-4 superharmonic injections attain a wider lock range

when biased at the V_{gs} located at the peak of the third-order nonlinear curve, confirming the discovering of an optimal biasing point [80]. Additionally, it was shown by utilizing the body effect and p-well injection using a triple n-well device, the lock range can further be increased based on increasing the third-order coefficient. With this analysis performed, the receiver can operate in the low-frequency GHz range, obtaining a sufficient lock range for divide-by-2 and divide-by-4 to process high-frequency signals. This will also allow the main oscillator to reduce its dynamic power consumption, as the free-running frequency of the design can be relaxed. Lastly, a widened lock range enables the receiver to achieve high sensitivity performance.

Chapter 4

Ultra-Low-Power Linearized LNA

From the previous chapter, we observed the advantages of increasing the nonlinear characteristics of the injection transistor to enhance the lock range for divide-by-4 ILFDs. In this chapter, we take a different approach and use the knowledge gained from analyzing transistors operating in the weak and strong inversion region, and apply it to a ultra-low-power (ULP) low noise amplifier (LNA) to improve its linearity properties, e.g., 1-dB compression point (P_{1dB}), third-order intercept (IIP3). It begins with a brief overview of low-power linearization techniques, followed by the proposed design. Next, optimal biasing and complementary derivative superposition (DS) is presented to demonstrate the linearization technique employed. Then, an analysis of the noise and input impedance is given, followed with simulations results and a comparison with state-of-the-art work. Section 4.1 presents the proposed ULP LNA. In section 4.2, the simulations results are presented. Lastly, section 4.3 summarizes this chapter.

4.1 Proposed ULP LNA

One of the main challenges in designing ULP LNAs is maintaining high linearity in conjunction with high gain and power efficiency. The dependency of the linearity of the amplifier arises from the biasing condition of the main transistor. Since ULP amplifiers are typically operating in the weak inversion region, they conduct ultra-low currents, exhibiting severe nonlinear characteristics. As a result, the input compression point and third-order

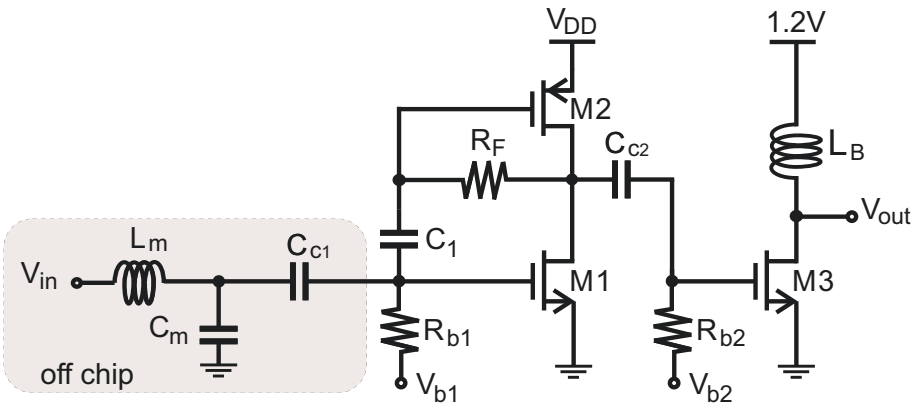


Figure 4.1: Proposed ultra-low-power LNA. Circuit parameters: $V_{DD} = 0.7$ V, $R_F = 15$ kΩ, $C_1 = 2$ pF, $M_1 = 3$ μm/120 nm, $M_2 = 10$ μm/120 nm, $M_3 = 200$ μm/120 nm, $M_4 = 20$ μm/120 nm.

intercept are usually small. For example, recent LNA designs have been proposed operating in the sub-100 μW range [81, 82], demonstrating effective performance in ultra-low-power (ULP) applications. However, they all suffer from poor linearity attributed to the biasing condition of the main transistor. Summarized in [83] describes linearization techniques to mitigate nonlinear effects of CMOS LNAs, mainly by reducing the magnitude of the third-order nonlinear coefficient around the DC operating point of the FET device. A practical approach that merely requires negligible additional power consumption is multiple gated transistor (MGTR), which utilizes small parallel auxiliary FETs biased in the subthreshold region to compensate for the nonlinear effects of the MT [84, 85]. As a result, the third-order intermodulation component is suppressed dramatically. Similarly, complementary derivative superposition (DS) implemented through body-bias control can increase the linearity of the LNA using the symmetrical properties of the DC operating points in an NFET/PFET transistor pair [86]. Unfortunately, the self-body biasing technique requires a triple-well CMOS process. Therefore, there is a need for a novel approach to improve the linear properties for ULP LNAs. We propose the LNA as shown in Fig. 4.1, which consists of a selective biased NFET and a self-biased PFET followed by a CS inductive load output buffer with an off-chip input impedance matching network.

4.1.1 Optimal Biasing

The biasing voltage of the NFET plays a critical role in dictating the overall performance of the LNA and requires extra considerations in sub-100 μW operation. Demonstrated in [87], the gate-source voltage that captures both power and bandwidth efficiency can be attained by finding the peak of $(g_{\mathrm{m}}/\mathrm{I_d})$ $\mathrm{f_t}$. Similarly, an ULP and ultra-low-voltage (ULV) biasing metric expanding upon the above condition, introduces the intrinsic gain, defined by $(g_{\mathrm{m}}/g_{\mathrm{ds}})$ $(g_{\mathrm{m}}/\mathrm{I_d})$ $\mathrm{f_t}$ [88], to achieve high-voltage amplification. The simulated biasing metric results as a function of V_{gs} for the NFET with dimensions of W = 3 μm and L = 120 nm, are shown in Fig. 4.2, illustrating a biasing voltage of approximately 500 mV which can optimize the LNA for gain, power, and bandwidth efficiency. Unfortunately, the linearity is neglected and requires further considerations.

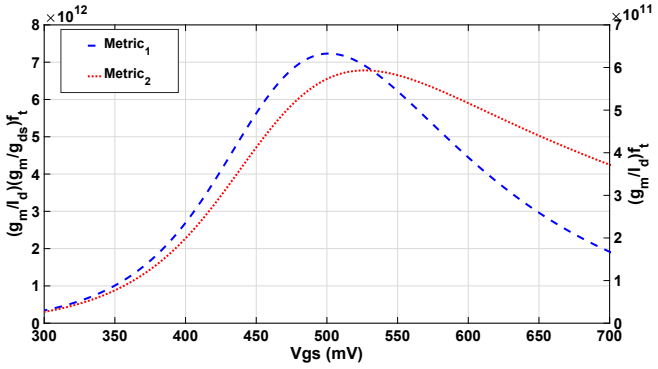


Figure 4.2: Metric 1 - $(g_m/I_d)(g_m/g_{ds})f_t$. Metric 2 - $(g_m/I_d)f_t$.

It is well known that the third-order intercept point of the circuit is heavily dependent on g_m'', where g_m'' exhibits a positive peak in weak inversion and a negative peak in the strong inversion region based up V_{gs} for an NFET transistor. Similarly, the PFET exhibits the same third-order nonlinear profile but in an inverse manner. Referred to as the "sweet spot," the MT of the LNA can be biased at the zero-crossing of g_m'' to reduce the nonlinear effects and improve linearity performance [89]. The drawback with this approach is that the nonlinearity is only reduced for a small perturbation of V_{gs} requiring auxiliary transistors for further

compensation. Additionally, the zero-crossing V_{gs} is lower than the optimal peak voltage attained previously, degrading voltage gain, power and bandwidth efficiency. Generally, the latter three performance properties are preferred resulting in a transistor biased near the negative peak of g_m'' exhibiting severe nonlinear characteristics. This, however, can be avoided using the complementary configuration such that the NFET is still optimally biased, and the PFET is sized accordingly to compensate for the nonlinear effects, resulting in LNA that can maintain low-power operation while achieving improvement in the linearity performance. Illustrated in Fig. 4.3, the small-signal model of LNA excluding the output buffer combines the nonlinear effects from both transistors.

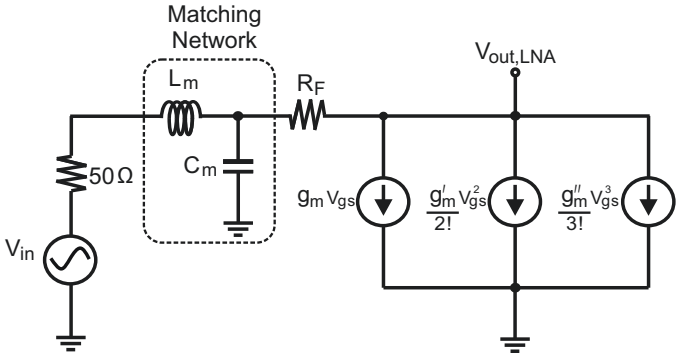


Figure 4.3: Simplified small-signal model of proposed LNA (w/o buffer).

For the PFET to effectively compensate the $g''_{m,n}$ of the NFET, the self-biased PFET has to offer the same magnitude of $g''_{m,n}$ with opposite phase so as to meet the resultant $g''_m = (g''_{m,p}) + (-g''_{m,n}) \approx 0$ for a linearized region of V_{gs}. Noting that the NFET is operating in the strong inversion region, in which the negative $g''_{m,n}$ can be expected whereas the PFET must then operate in the weak inversion region to obtain the positive $g''_{m,p}$.

Recall from the previous chapter we observed that the third-order coefficient for an NFET device in the strong and weak inversion region results in gain compression and expansion respectively. This relationship is also equivalent for a PFET transistor. Therefore, from Eq. (3.58) and Eq. (3.62) we conclude that $g''_{m,n}$ is negative and $g''_{m,p}$ is positive and

since $g''_m = g''_{m,n} + g''_{m,p}$, the dimensions, threshold voltages, and overdrive voltages of the transistors can be adjusted accordingly to reduce g''_m to zero.

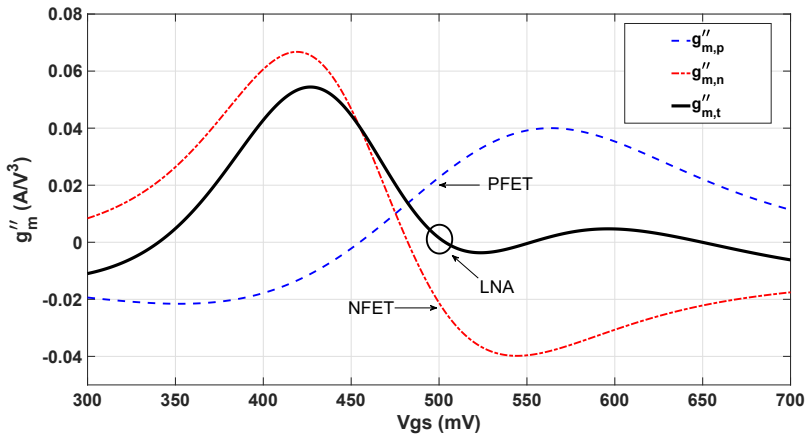


Figure 4.4: Third-order nonlinear coefficients.

Fig. 4.4 shows simulated NFET and PFET third-order nonlinear coefficients of BSIM4 models where $g''_{m,t}$ is the combined $g''_{m,p}$ and $g''_{m,n}$. Using the optimal biasing voltage of 500 mV, and sizing the PFET 3.5 times larger in which the self-biased voltage is approximately 225 mV, the $g''_{m,p}$ is located near the positive peak in the weak inversion region. Noting that the PFET curve is shifted to left by 275 mV, the resultant $g''_{m,t}$ is approximately zero, obtaining a compensated third-order nonlinear coefficient around the LNA's operating point. Thus, keeping the gm-boosting and current reuse properties, the overall third-order coefficient is significantly reduced close to zero in comparison with that of the NFET and PFET without introducing auxiliary transistors such that low-power and high linearity performance can be obtained. Table 4.1 summarizes the detail of each transistor and component values. The inductor at the output of the buffer stage is sized accordingly such that the buffer exhibits a 50 Ω output impedance at 915 MHz. The architecture of the design remains simple, achieving dual "sweet spots" based on linearity, power, gain and bandwidth efficiency.

Table 4.1: Design Parameters.

Component	Value
M_1	3/0.12 μm
M_2	10.5/0.12 μm
M_3	30/0.12 μm
V_{b1}	500 mV
V_{b2}	1 V
L_B	10.5 nH
R_F	15 kΩ
C_1	2 pF

4.1.2 Noise Analysis

Presume the noise component are uncorrelated, and ignore the gate noise. The main noise sources of the LNA is the channel noise due to M_1 and M_2, as well as the noise component attributed to R_F. In addition, the gate-source capacitance and gate-drain capacitance will affect the noise response. The noise factor can be estimated from Eq. (4.1).

$$F = 1 + \frac{\gamma g_m}{R_s}\Big[\frac{R_F + R_s + j\omega R_F R_s(C_{gd}+C_{gs})}{(1 - R_F g_m) + j\omega C_{gd} R_F}\Big]^2$$

$$+ \frac{R_F}{R_s}\Big[\frac{R_s g_m + 1 + j\omega C_{gs} R_s}{(1 - R_F g_m) + j\omega C_{gd} R_F}\Big]^2 \tag{4.1}$$

where $C_{gs} = C_{gs,n} + C_{gs,p}$, $C_{gd} = C_{gd,n} + C_{gd,p}$, $g_m = g_{m,n} + g_{m,p}$, and γ is the excess noise coefficient. The second term in Eq. (4.1) is due to the channel noise from both MOS devices and the third term is due to the thermal noise of the feedback resistor.

4.1.3 Input Impedance

At sub-GHz frequencies, the gate-drain and gate-source capacitance should be accounted for to accurately design the matching network. Therefore, the L-matching network, composed of inductor L_m and capacitor C_m is designed in accordance with the input impedance of the LNA as shown in (4.2).

$$Z_{in}(j\omega) \approx \frac{R_F + r_o + j\omega\frac{r_o}{\omega_{c1}}}{(1 + \frac{g_m}{g_{ds}} - \frac{\omega^2}{\omega_{c1}\omega_{c3}}) + j\omega(\frac{1}{\omega_{c1}}(1 + \frac{g_m}{g_{ds}}) + \frac{1}{\omega_{c2}} + \frac{1}{\omega_{c3}})} \tag{4.2}$$

where $r_o = r_{on}||r_{op}$, $g_{ds} = g_{ds,n}||g_{ds,p}$, $\omega_{c1} = 1/C_{gd}R_F$, $\omega_{c2} = 1/C_{gs}R_F$, and $\omega_{c3} = 1/C_{gs}r_o$.

4.2 Simulation Results

The LNA operates with a 0.7 V supply voltage, drawing 48 μA of DC current from the supply. Excluding the power dissipated from the buffer, the total power consumption is approximately 35 μW. As shown from Fig. 4.5, the simulated forward voltage gain S_{21} and input reflection coefficient S_{11} are 15.7 dB and -15 dB, respectively. The simulated

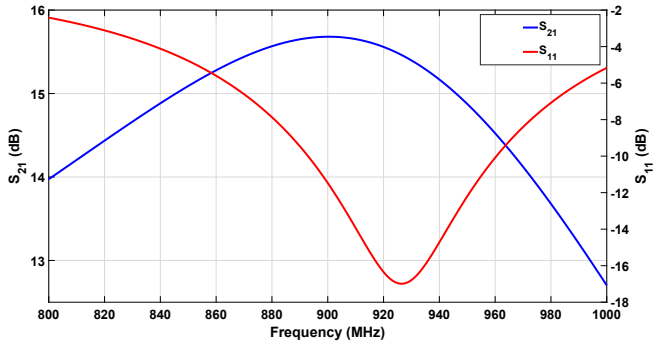


Figure 4.5: Simulated forward voltage gain and input reflection coefficient.

bandwidth is approximately 100 MHz and covers the desired 902 - 928 MHz ISM band. Fig. 4.6 depicts the noise figure at the output of the buffer and the output of the LNA. The LNA exhibits a noise figure of 5.3 dB, and the total noise figure at the output of the buffer is 5.7 dB.

To simulate the linearity performance a two-tone test is performed at 910 MHz and 920 MHz. As shown from Fig. 4.7, the simulated third-order intercept point (IIP3) and 1-dB compression point (P_{1dB}) are -6.5 dBm and -17.5 dBm, respectively.

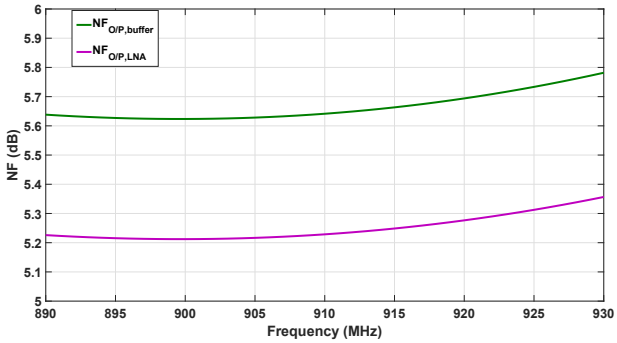


Figure 4.6: Simulated noise figure at output and input of buffer.

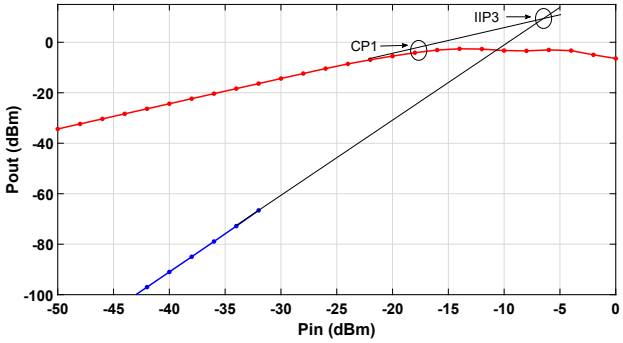


Figure 4.7: Simulated IIP3 and P_{1dB}.

4.3 Summary

To evaluate the overall performance of the LNA, the figure-of-merit (FOM) in (4.3) is used where the IIP3 and P_{dc} are in units of mW, F is the noise factor, and A_v is the voltage gain, which are both unitless quantities. The calculated FOM is 15.19 and compared with state-of-the-art work targeting low-power LNAs. As shown in Table 4.2, the results of this work obtain the highest FOM due to the enhanced IIP3 and minimal power consumption. Demonstrating effective performance for ULP applications.

$$FOM = \frac{IIP3 \times A_v}{P_{dc} \times (F-1)}. \tag{4.3}$$

In summary, a CS-based LNA implemented in GF 130 nm CMOS technology, composed of a selective biased NFET and a self-biased PFET, employing complementary DS is

Table 4.2: Performance Comparison.

Reference	**This Work**	[81]	[82]	[88]	[91]	[92]
Tech [nm]	130	130	40	90	110	180
Pdc [μW]	35	60	30	750	336	200
Gain [dB]	15.7	13.1	14.2	12.6	14.8	17
IIP3 [dBm]	-6.5	-12.2	-13.2	-6	-3.7	-14
P_{1dB} [dBm]	-17.5	-19	-	-18	-12.6	-
NF [dB]	5.7	5.3	3.3	5.5	3.7	4.2
FOM	**15.19**	1.9	7.19	0.56	5.2	0.86

proposed. The design procedure consists of selecting a biasing voltage for the NFET where the LNA is optimized for voltage gain, power, and bandwidth efficiency. In addition, by utilizing an accurately sized self-biased PFET load to compensate for the nonlinear effects of the NFET's biasing condition, resulting in enhanced linearity. The LNA targets the 915 MHz ISM band and operates with a 0.7 V supply consuming 35 μW of power. The linearity performance was simulated by Spectre, resulting in an IIP3 of -6.5 dBm, and P_{1dB} of -17.5 dBm. The simulated voltage gain, input reflection coefficient and noise figure are 15.7 dB, -15 dB and 5.7 dB respectively. The evaluated performance of the design using a classical FOM is compared with similar literature targeting ULP LNA designs, resulting in the highest known value [90].

Chapter 5

Receiver Design

This chapter presents the design and analysis of the front-end receiver, implemented in GF 130 nm CMOS technology, consisting of a LNA, ILO and ED. The performance of each circuit block is shown, which was simulated and tested using Cadence Design Systems. Next, the overall functionality of the receiver is demonstrated and compared with state-of-the-art work based on injection-locked receiver designs. In section 4.1, the LNA design is shown, presenting the voltage gain, noise and input matching performance. Section 4.2 demonstrates the design of the ILO, showing the frequency-to-amplitude conversion property for each frequency band. Next, section 4.3 shows the ED design used for data extraction. Following is section 4.4 showing the receiver performance. Lastly, section 4.5 summarizes this chapter.

5.1 Low-Noise Amplifier

The LNA stage is used to amplify the received signal detected from the antenna while minimizing the noise. Since the ILO requires a sufficient amplitude to lock to the received signal, the design motivation of the LNA is to achieve a large voltage gain while maintaining low-power dissipation. There are a number of circuit topologies suitable for the LNA, among them is the cascode common-source (CS) stage with an inductive load. This topology offers a high voltage gain under low current and supply voltages attributed to its large output impedance. The circuit schematic of the LNA is shown in Fig. 5.1, composed of two stages.

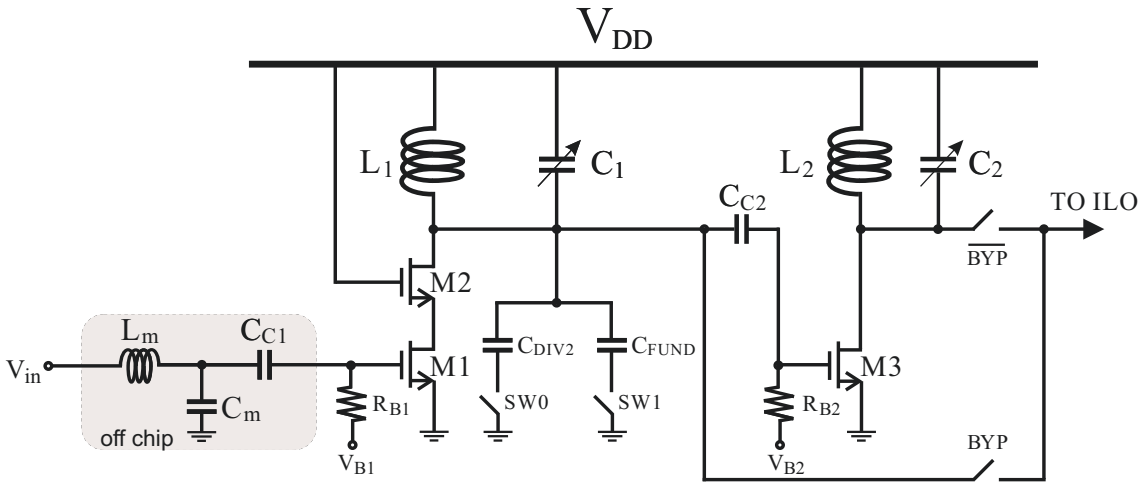


Figure 5.1: Schematic view of LNA. Circuit parameters: $M_{1,2}$ = 16 μm/180 nm, M_3 = 6 μm/180 nm, $V_{B1,B2}$ = 450 mV, V_{DD} = 0.7 V, L_1 = 8.5 nH, L_2 = 4.7 nH, C_{DIV2} = 2.15 pF, C_{FUND} = 10 pF, $R_{B1,B2}$ = 50 kΩ, C_{C1} = 5 pF, C_{C2} = 1 pF, C_1 = 100 - 400 fF, C_2 = 40 - 200 fF.

The first stage is the cascode used for amplification and the second stage is cascaded as a buffer. With a supply voltage of 0.7 V, the cascode and buffer stage draw 260 μA and 120 μA, consuming 182 μW and 84 μW of power respectively. The biasing of transistor M_1 and M_3 is optimized for bandwidth and power efficiency by setting $V_{B1,B2}$ at the peak of (g_m/I_d) f_t [87]. Since the LNA contains inductors and targets various frequency bands, the LNA stage operates in three different modes.

- **Mode 1**: The first mode, targets the 2.36 - 2.4 GHz band. The bypass switches are implemented by large NFET transistors with a width of 100 μm and a length of 120 nm. In this mode, the BYP switch is left open, and the cascode stage amplifies the received signal which is then passed through the buffer towards the ILO. The switches from the capacitor bank SW0 and SW1 are both turned off, and the varactors C_1 and C_2 are used to accurately tune the tanks to maximize the impedance centered around 2.38 GHz. The resonance frequency of the first and second tank circuit are set as $\omega_{2400} = 1/\sqrt{L_1C_1}$ and $\omega_{2400} = 1/\sqrt{L_2C_2}$ respectively. Noting that SW0 and SW1 are NFET transistors with widths of 70 μm and lengths of 120 nm. These dimensions are chosen because they contribute only a small amount of parasitic capacitance to the LC tank circuit, allowing L_1 to maintain large in inductance. The buffer stage

is employed due to its high input impedance, ensuring that the inductor L_1 is large enough to obtain a sufficient voltage gain. The buffer is only designed for this band. This is because parasitic capacitance at the input of the ILO is too large, leading to smaller L_1, resulting in a smaller voltage gain.

- **Mode 2**: The second mode targets the 860 - 868 MHz, 902 - 928 MHz, and 950 - 958 MHz frequency bands. Switch BYP is closed, and the buffer is bypassed, reducing power consumption. Also, $\overline{\text{BYP}}$ is open and SW0 is turned on, in which the total capacitance of the tank circuit is from the parallel combination of C_{DIV2} and C_1, peaking the resonance frequency around 900 MHz. Varactor C_1 is used for accurate impedance modification. The resonant frequency of the tank circuit is given as $\omega_{950,915,868} = 1/\sqrt{L_1(C_1 + C_{\text{DIV2}})}$.

- **Mode 3**: The third mode, targets the 433 MHz band, requiring both SW0 and SW1 to be on such that the tank is resonating around 433 MHz, as the total capacitance is the parallel combination of C_{FUND}, C_{DIV2} and C_1. Also, the bypass switch BYP is on similar to the mode 2, with $\overline{\text{BYP}}$ open. As a result, the resonant frequency of the tank circuit can be expressed as $\omega_{433} = 1/\sqrt{L_1(C_1 + C_{\text{DIV2}} + C_{\text{FUND}})}$.

5.1.1 Voltage Gain

Neglecting parasitics capacitance, the gain of the cascode stage can be expressed as

$$A_{v1} = -G_m R_{out} = -g_{m1}(R_{p1}||(r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2}), \tag{5.1}$$

where $R_{p1} = Q_1 L_1 \omega$ and is the equivalent resistance of the tank circuit at resonance. Q_1 is the quality factor of the tank, L_1 is the inductance, ω is the frequency, $g_{m1,m2}$ and $r_{o1,o2}$ are the transconductance and channel length modulation from transistors M_1 and M_2 respectively, and g_{mb2} is the body-channel transconductance of M_2. Next, the voltage gain of the CS buffer stage can be expressed as

$$A_{v2} = -g_{m3}(R_{p2}||r_{o3}), \tag{5.2}$$

where r_{o3} is the channel length modulation from transistor M_3 and $R_{p2} = Q_2 L_2 \omega$ is the equivalent resistance of the second tank circuit. Therefore, the overall voltage gain can be given as the product of Eq. (5.1) and Eq. (5.2)

$$A_{vt} = g_{m1} g_{m3}(R_{p2}||r_{o3})(R_{p1}||(r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}). \tag{5.3}$$

Noting that Eq. (5.3) only applies to the 2.4 GHz frequency band. Observing that for the LNA to obtain a large voltage gain, the overall output impedance should be maximized. Since the transistor configuration branch dominates the output impedance, the gain mainly depends on the impedance of the tank circuits. Therefore, a larger inductance is more desirable due to the proportional relationship to the equivalent resistance of $\mathrm{R_p}$.

5.1.2 Input Impedance

To accurately design the matching network, the gate-drain and gate-source capacitance from transistor $\mathrm{M_1}$ should be considered. Therefore, we have

$$Z_{in,1}(j\omega) = \frac{(1 + \frac{g_{m2}}{g_{ds1}}) + \frac{j\omega}{\omega_1}}{j\omega\big[C_{gd1}(1 + \frac{g_{m1}+g_{m2}}{g_{ds1}}) + C_{gs1}(1 + \frac{g_{m2}}{g_{ds1}})\big] - \frac{\omega^2 C_{gd1} C_{gs1}}{g_{ds1}}}, \tag{5.4}$$

where $\omega_1 = 1/C_{gd1} r_{o1}$. The matching network used is type L-match consisting of a series inductor, and a shunt capacitor configured off-chip, i.e., not placed on the substrate. Noting that the values for inductor $\mathrm{L_m}$ and capacitor $\mathrm{C_m}$ change depending on which frequency band is being targeted.

5.1.3 Noise Analysis

The noise figure of the LNA is acquired by first finding the input impedance of the second stage, expressed as

$$Z_{in,2}(j\omega) = \frac{R_{p2} + r_{o3} + j\omega C_{gd3} R_{p2} r_{o3}}{j\omega\left[\frac{1}{\omega_2} + \frac{1}{\omega_3} + \frac{C_{gd3} R_{p3} g_{m3}}{g_{ds3}}\right] - \frac{\omega^2}{\omega_4 \omega_5}}, \tag{5.5}$$

where $\omega_2 = 1/C_{g3} r_{o3}$, $\omega_3 = 1/C_{g3} R_{p3}$, $\omega_4 = 1/C_{gs3} r_{o3}$, $C_{g3} = C_{gd3} + C_{gs3}$, and $\omega_5 = 1/C_{gd3} R_{p3}$. Next, the output resistance of the cascode stage is given as

$$R_{out,1} = R_{p1} || (r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}). \tag{5.6}$$

With the main noise sources of the LNA attributed from the channel noise from transistors M_1, M_2 and M_3, and the thermal noise from the equivalent tank impedance at resonance of both tank circuits, i.e., $R_{p1,p2}$, the expression for the noise factor can be acquired. The noise factor is determined by first finding the total output noise power spectral density from stage 1, given as

$$\begin{aligned} S_{vo,1} = {} & 4kTR_{p1}\left(\frac{r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}}{r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2} + R_{p1}}\right)^2 \\ & + 4kT\gamma g_{m1} \left(R_{p1} || (r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2})\right)^2 \\ & + 4kT\gamma g_{m2} \left(\frac{R_{p1} r_{o2}}{R_{p1} + r_{o2} + r_{o1} + g_{m2} r_{o2}}\right)^2, \end{aligned} \tag{5.7}$$

where γ is the excess noise coefficient approximately equal to 2 for short-channel devices [93]. The first, second, and third terms of Eq. (5.7) are the output power spectral noise densities from the thermal noise due to R_{p1}, and channel noise from M_1 and M_2 respectively. The output noise power spectral density of the second stage can be expressed as

$$S_{vo,2} = 4kT\gamma g_{m3} (R_{p2} || r_{o3})^2 + 4kTR_{p2} \left(\frac{r_{o3}}{r_{o3} + R_{p2}}\right)^2, \tag{5.8}$$

where the first term in Eq. (5.8) is the channel noise due to M_3 and the second term is thermal noise from R_{p2}. Next, ϵ_1 and ϵ_2 are given as

$$\epsilon_1 = \frac{Z_{in,1}}{Z_{in,1} + R_s}, \tag{5.9}$$

and

$$\epsilon_2 = \frac{Z_{in,2}}{Z_{in,2} + R_{out,1}} \tag{5.10}$$

respectively. Therefore, the overall noise factor of the LNA stage is expressed as

$$F = 1 + \frac{S_{vo,1}}{(A_{v1}\epsilon_1)^2 4kTR_s} + \frac{S_{vo,2}}{(A_{v1}\epsilon_1 A_{v2}\epsilon_2)^2 4kTR_s}. \tag{5.11}$$

5.1.4 Simulation Results

In this section, the simulated voltage gain, input reflection coefficient, and noise figure are shown. As seen from Fig. 5.2, the maximum and minimum simulated voltage gain for the 2.4 GHz band is 42 and 40 dB respectively. In addition, the simulated input reflection coefficient reaches a minimum of -25 dB and a maximum of -15 dB. Noting that each frequency band has its own unique L-match network since the input impedance of the LNA varies with frequency. The signal bandwidth is approximately 80 MHz. The noise figure, as seen from Fig. 5.3, has a minimum value of 2.075 dB at 2.4 GHz and a maximum value of 2.125 dB at 2.36 GHz. Observing that a large voltage gain is attained since the capacitor bank is switched off. Also noting that the buffer stage only provides a gain of approximately 2 dB.

Shown in Fig. 5.4, the simulated voltage gain for the 863, 915 and 950 MHz frequency bands is 29, 31, and 30 dB respectively. Additionally, the bandwidths are 25 MHz, 30 MHz and 20 MHz respectively. The gain decreases from 42 dB since one of the switches is turned

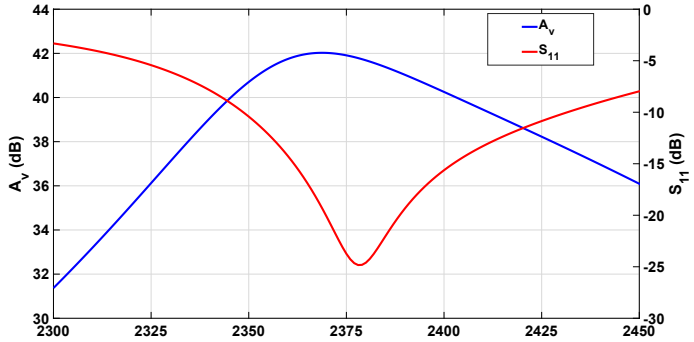


Figure 5.2: Simulated voltage gain and input reflection coefficient for the 2.4 GHz frequency band.

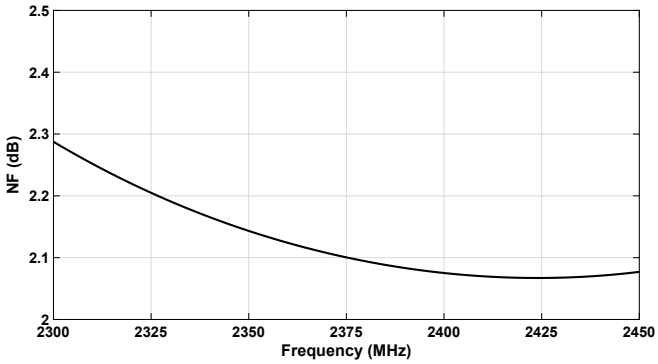


Figure 5.3: Simulated noise figure for the 2.4 GHz frequency band.

on. With the voltage gain mainly determined by the equivalent tank resistance R_{p1}, an additional on resistance r_{on} is introduced in parallel, thus degrading the output impedance.

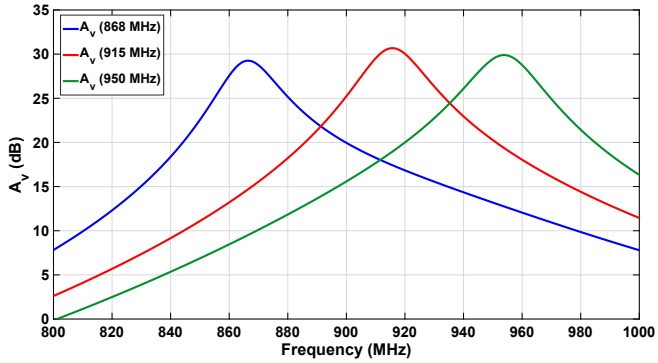


Figure 5.4: Simulated voltage gain for the 863, 915, and 950 MHz frequency bands.

The simulated input reflection coefficients for the 863, 915, and 950 MHz frequency bands, as seen from Fig. 5.5, are -15, -16, and -17 dB respectively. Additionally, as shown in Fig. 5.6, the simulated noise figure is 3 dB for the three frequency bands.

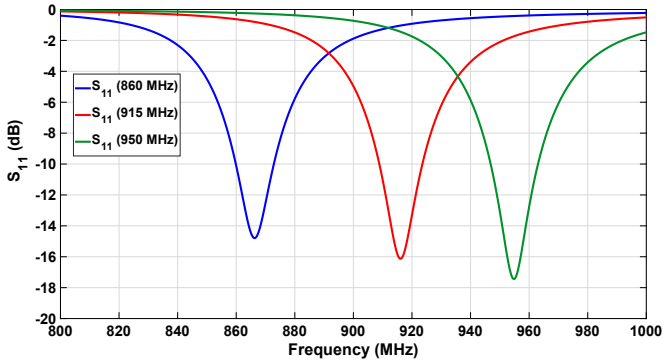


Figure 5.5: Simulated input reflection coefficients for the 863, 915, and 950 MHz frequency bands.

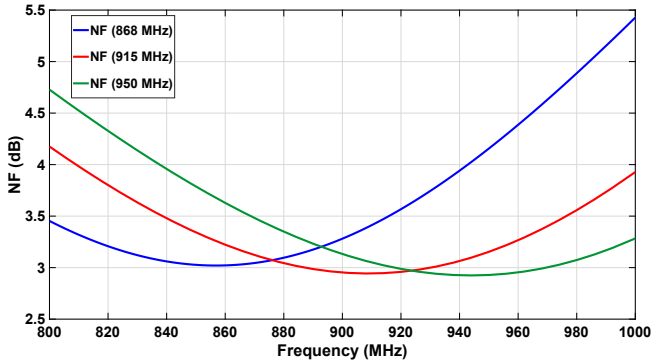


Figure 5.6: Simulated noise figure for 863, 915, and 950 MHz frequency bands.

Shown in Fig. 5.7, the simulated voltage gain for the 433 MHz frequency band is approximately 20 dB with a bandwidth of 20 MHz. In addition, the input reflection coefficient is -13 dB. Lastly, as shown in Fig. 5.8, the simulated noise figure is 2.5 dB.

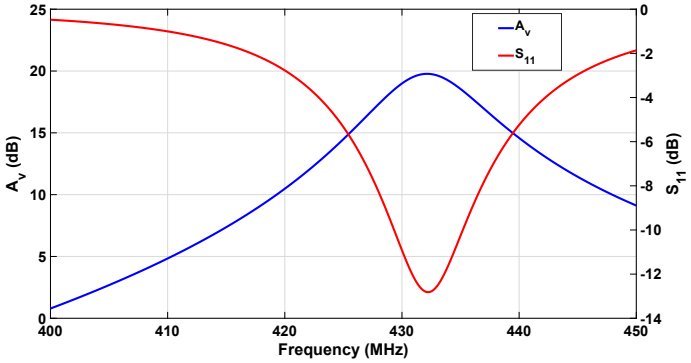


Figure 5.7: Simulated voltage gain and input reflection coefficient for the 433 MHz frequency band.

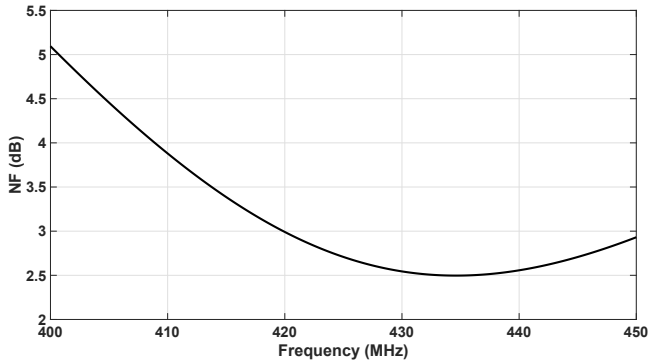


Figure 5.8: Simulated noise figure for the 433 MHz frequency band.

5.1.5 Discussion

This section presented the LNA design and analysis of the gain, input impedance, and noise. It was shown that the cascode stages provides a large voltage gain while maintaining minimal power consumption and noise. The gain of the LNA reaches a maximum value of 42 dB for the 2.4 GHz band and a minimum value of 20 dB for the 433 MHz band. Additionally, the 863 MHz, 915 MHz, and 950 MHz frequency bands each achieve voltage gains of approximately 30 dB. This section also showed the noise figures for each frequency band, which ranges from 2 to 3 dB. The off-chip input matching networks for all five frequency bands were designed using a simple L-match, providing reasonable matching performance, e.g. lower than -10 dB.

5.2 Injection-Locked Oscillator

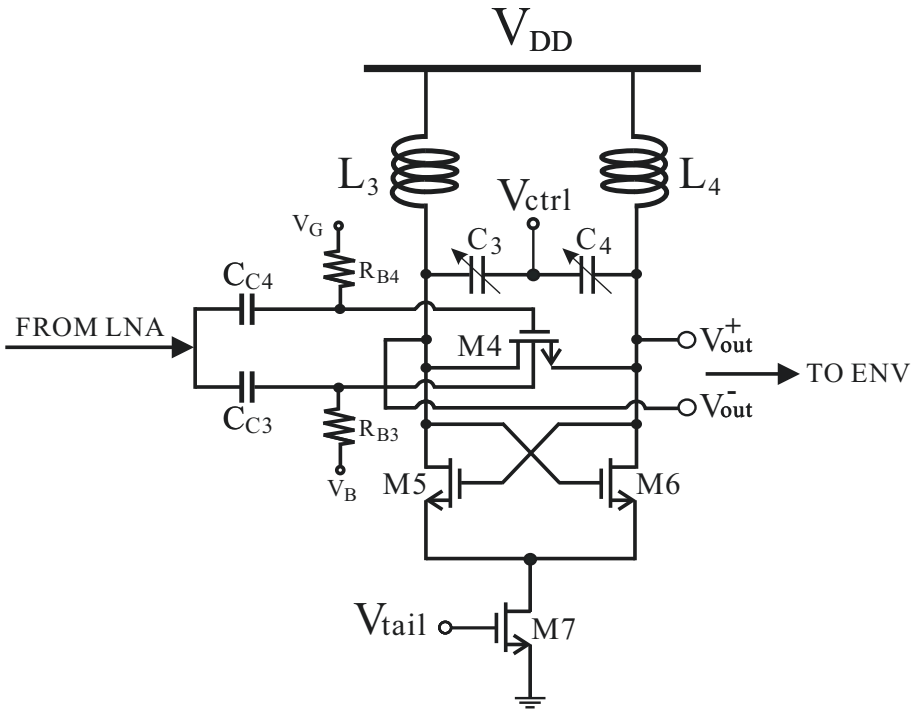


Figure 5.9: Schematic of injection-locked oscillator. Circuit parameters: M_4 = 95 μm/120 nm, $M_{5,6}$ = 60 μm/120 nm, M_7 = 90 μm/120 nm, V_{tail} = 0.45 V, V_{DD} = 0.7 V, $L_{3,4}$ = 22 nH, $C_{3,4}$ = 1.40 - 7.14 pF, $C_{C3,C4}$ = 10 pF, $R_{B3,B4}$ = 50 kΩ, V_B = 900 mV.

The ILO is implemented by the LC cross-coupled oscillator, as shown in Fig. 5.9. This circuit is the most critical block in the receiver to demodulate the ASK and FSK signals. In comparison with the ring oscillator, the LC oscillator offers better phase noise performance, affecting the BER directly. The design of the ILO mainly lies in the frequency bands that need to be covered while minimizing power consumption. Discussed in Chapter 3, the frequency-to-amplitude conversion happens on fundamental injection-locking and superharmonic injection-locking. Table 5.1 summarizes the WSN frequency bands of interest, with their injection-locking division and corresponding lower and upper bounds of the locking frequencies. From Table 5.1, we notice that the lowest frequency of the oscillator, 430 MHz, is determined by the frequency band 860-868 MHz, and the highest frequency, 600 MHz, is set by the 2.4 GHz frequency band.

Table 5.1: ILO Frequency Plan.

Frequency Band (MHz)	**433-434.8**	**860-868**	**902-928**	**950-958**	**2360-2400**
Division Ratio	1	2	2	2	4
f_{locked} (MHz)	433-434.8	430-434	451-468	475-479	590-600

Therefore, at a minimum the ILO must have a frequency tuning range between 430 - 600 MHz and realizing that ILO can perform divide-by-4, divide-by-2 and fundamental injection, the oscillator can target the WSN frequencies within the 400 - 2400 MHz spectrum. The ILO draws 720 μA of DC current under a 0.7 V supply voltage, consuming about 500 μW of power. The signal at the output of the LNA is injected in the gate and body of transistor M_4 to perform locking, resulting in frequency-to-amplitude conversion. The voltages V_B and V_G are the body and gate biasing voltages configured such that the harmonic mixer exhibits high third-order nonlinear characteristics for a wide divide-by-4 and divide-by-2 lock range. V_B is set to 900 mV to modify the threshold via body effect, increasing the third-order nonlinear coefficient of M_4. V_G is set to 935 mV, located at the peak of the third-order coefficient, when performing divide-by-2 and divide-by-4 superharmonic injection. When performing fundamental injection for the 433 MHz band, V_G is increased to 985 mV since a larger biasing voltage for M_4 results in a larger injection current and thus, a wider lock range. However, it is important not to increase V_G any larger as the output voltage of the ILO starts to decrease due to the parasitics of the injection transistor. The RF signal from the LNA is directly coupled to the gate and body to increase the injection power applied to the ILO. The control voltage V_{ctrl} is used to adjust the capacitance from the varactors C_3 and C_4 to tune the center frequency of the oscillator at a value depending on which frequency band is being targeted. Consider that the frequency band of interest is 2.36 - 2.4 GHz. The center frequency should be set at approximately 595 MHz because the upper and lower frequencies, when divided by four, are 590 MHz and 600 MHz. And since the lock range is typically symmetrical around the center frequency, the ILO can lock to these frequencies as long as it is under its locked status. Transistor M_7 sets the biasing current of the oscillator, and transistors M_5 and M_6 consist of the cross-coupled pair to exhibit a

negative transconductance for sustained oscillation. The output voltage nodes V_{out}^{+} and V_{out}^{-} at the drain node of the cross-coupled pair are then applied to the input of the ED for data extraction. Following this section is the simulation results. Recall that the main parameter of interest is the frequency-to-amplitude conversion of the ILO.

5.2.1 Simulation Results

As seen from Fig. 5.10, the simulated center frequency varies from 600 MHz to 400 MHz when the control voltage alters from 400 mV to 700 mV. This frequency selectivity is sufficient as the slope or sensitivity is maximum within the frequency range of interest. Also observing that the differential peak output voltage varies from 190 mV to 130 mV. The reason for the decrease is attributed to the LC tank circuit becoming more capacitive. However, the output voltage is still large enough for the ED.

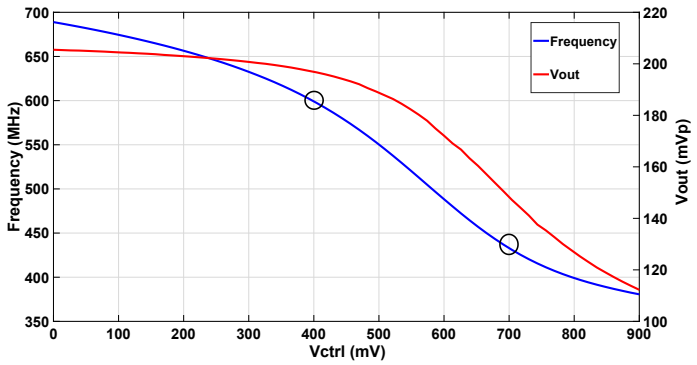


Figure 5.10: Simulated frequency and output voltage vs. control voltage.

Fig. 5.11, shows the frequency-to-amplitude conversion property for divide-by-4 injection of the ILO. The center frequency of the ILO is tuned to 597 MHz to avoid incident frequencies having identical output voltages upon frequency locking. Recall that the frequency-to-amplitude is ideally symmetrical around the lock range, which may result in different incident frequencies having the same output voltage. This needs to be avoided because if the receiver senses an FSK signal with frequencies that have identical output volt-

ages after the ILO, the output of the ED will exhibit the same amplitude. In this simulation, the LNA detects a -50 dBm signal, and as the incident frequency varies from 2360 - 2400 MHz, the peak differential output voltage alters from 155 mV to 185 mV.

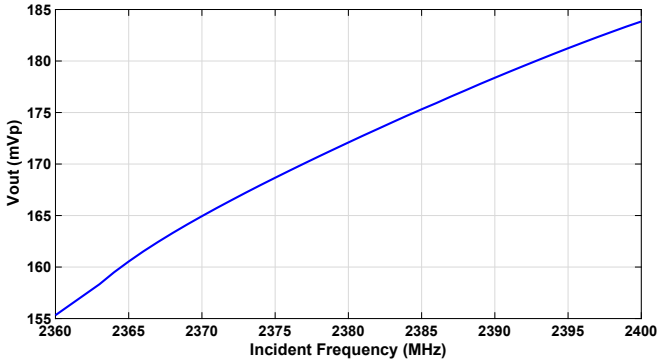


Figure 5.11: Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 597$ MHz.

Similarly, Fig. 5.12 illustrates the simulated frequency-to-amplitude for the divide-by-2 operation when targeting the 915 MHz frequency band. With the center frequency set at 460 MHz, specific incident frequencies map to the same output voltage. This is because the LNA has a voltage gain less than 10 dB compared to the 2.4 GHz operation, resulting in a smaller lock range. However, this can be alleviated by adjusting the center frequency near the upper or lower bounds. But some frequencies within the band may not lie within the lock range.

Alternatively, as seen from Fig. 5.13 and Fig. 5.14, illustrating the frequency-to-amplitude conversion for the 950 MHz and 863 MHz bands does not experience the same effect. This is because the frequency bands are not large in size, and it is easier to ensure that each incident frequency has its unique output voltage by placing the center frequency near the edge of bands, e.g., $f_c = 958/2 = 479$ MHz.

Fig. 5.15 shows the frequency-to-amplitude conversion for the 433 MHz band which varies by approximately 5 mV across the incident frequency range of 431 to 435 MHz.

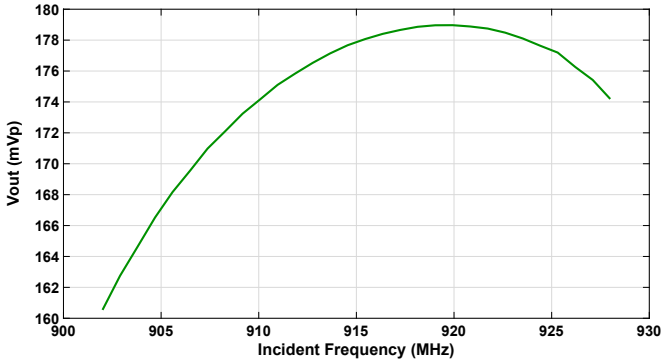


Figure 5.12: Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 460$ MHz.

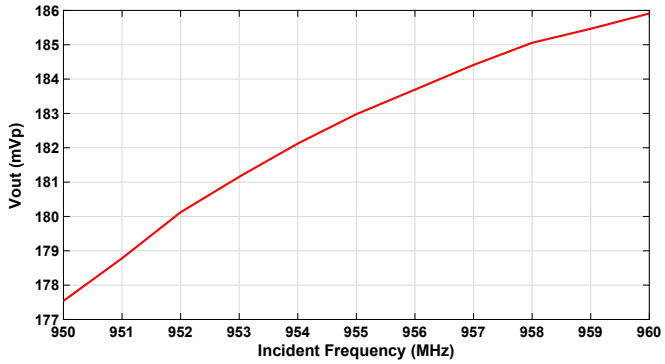


Figure 5.13: Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 479$ MHz.

In addition to FSK signals, an OOK signal can also be detected using the frequency-to-amplitude conversion property of the ILO. This is accomplished by ensuring that the output voltage of the ILO for a given free-running frequency is different than the output voltage for an incident frequency of the OOK signal. Suppose that when the OOK signal is in its ON state and is detected by the receiver, the ILO will lock to the incident frequency, obtaining an output voltage of V_{locked}. Now, when the OOK signal is not present and in its OFF state, the ILO will return to its free-running output voltage V_{osc}, thus able to detect OOK signals.

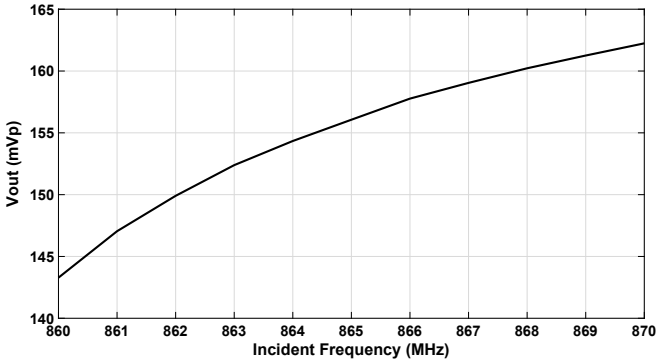


Figure 5.14: Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 435$ MHz.

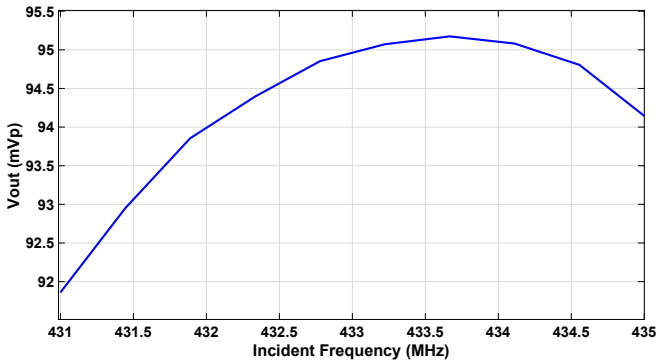


Figure 5.15: Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 434$ MHz.

5.2.2 Discussion

This section presented the design and operation of the ILO. Showing that by accurately setting the frequency tuning range of the ILO, the receiver can target a wide range of frequency bands by performing alternative forms of injection-locking. This ILO performs fundamental, divide-by-2 and divide-by-4 injection covering the WSN frequency bands from 433 - 2400 MHz. Additionally, the frequency-to-amplitude conversion property from each band was presented. The gain or conversion from frequency to voltage can be given as $\frac{d_{Vout}}{df}$ with units V/Hz. It was shown that when the LNA receives a -50 dBm input, the gain or slope is approximately 1 mV/MHz. The ED circuit can then amplify the voltage variations

through its nonlinear operation. As a result, the ILO remains simple in design and can target a variety of frequency bands while maintaining low-power dissipation.

5.3 Envelope Detector

The ED circuit is used to extract the received signal by amplifying the voltage differences measured from the ILO. Since the ILO contains differential outputs, the ED used is the pseudo-differential CS topology as seen from Fig. 5.16. With a current of 10 μA, and a supply voltage of 0.7 V, the power consumption is 7 μW. The differential output from the ILO is applied to the input transistors M_8 and M_9. Transistor M_{12} provides the bias current from a diode connected current source which is copied to the envelope detector through the PFET current mirror composed of transistors M_{10} and M_{11}. To maintain low-power consumption, the input transistors M_8 and M_9 are biased in the subthreshold region, thus the drain-source current can be expressed as

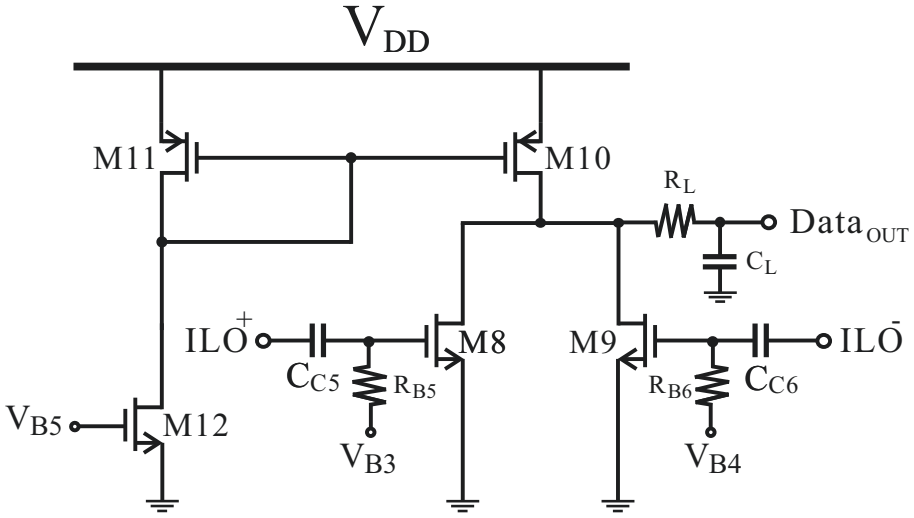


Figure 5.16: Schematic of envelope detector. Circuit parameters: $M_{8,9}$ = 2 μm/120 nm, M_{10} = 40 μm/180 nm, M_{11} = 20 μm/180 nm, M_{12} = 1 μm/180 nm, V_{DD} = 0.7 V, $V_{B3,B4,B5}$ = 450 mV, $C_{C5,C6}$ = 1 pF, $R_{B3,B4}$ = 50 kΩ, R_L = 5 kΩ, C_L = 500 fF.

$$I_{ds,sub} = I_{d0} e^{\frac{V_{gs}-V_{th}}{n\phi_t}}, \tag{5.12}$$

where I_{d0} is the current constant, n is subthreshold slope, and ϕ_t is the thermal voltage approximately equal to 26 mV at room temperature. In the presence of a RF signal, V_{gs} can be expressed as $V_b + V_a cos(\omega t)$, where V_b is the gate bias voltage imposed by an RF signal given as $V_a cos(\omega t)$. The frequency of RF the signal is given as ω and its peak voltage as V_a. Therefore, Eq. (5.12) can be expanded as

$$I_{ds,sub} = I_{d0} e^{\frac{V_b + V_a cos(\omega t) - V_{th}}{n\phi_t}} = I_{B0} e^{\frac{V_a cos(\omega t)}{n\phi_t}}, \tag{5.13}$$

where $I_{B0} = I_{d0} e^{\frac{V_b - V_{th}}{n\phi_t}}$. Noting that for this design, V_a ranges from approximately 50 - 100 mV as the frequency of the ILO varies from 430 - 600 MHz. These peak voltages are large enough to extract the transmitted data properly. Furthermore, the exponential term can be expressed as a power series given as

$$I_{ds,sub} = I_{B0}\big[1 + (\frac{V_a}{n\phi_t})^2 + \frac{V_a}{n\phi_t} cos(\omega t) + (\frac{V_a}{2n\phi_t})^2 cos(2\omega t)\big]. \tag{5.14}$$

Initially, the common-drain node is pulled to approximately the supply voltage V_{DD} and as the amplitude V_a of the input RF signal increases, the DC output node which is charged by the biasing current provided by M_{10} begins to discharge through either transistor M_8 or M_9 to ground, pushing the DC output voltage downwards. In other words, as the RF signal increases, the DC output voltage decreases. From Eq. (5.14), the DC output RC load filters the high-frequency components and reacts to the DC current given by

$$I_{ds,sub} = I_{B0}\big[1 + (\frac{V_a}{n\phi_t})^2\big]. \tag{5.15}$$

As a result, the ED can extract the voltage variations exhibited from the ILO to output the received data.

5.3.1 Simulations Results

To observe the RF to DC conversion property of the ED, the DC output voltage is measured when a differential RF input signal with a frequency of 600 MHz is applied to input gates of transistors M_8 and M_9 to replicate the ILO output signal. The peak amplitude voltage is then varied between 0 to 100 mVp. As seen from Fig. 5.17, the DC output voltage is approximately equal to V_{DD} when the RF peak voltage is 0. And as the input continues to increase, the DC output voltage approaches 0 V. Taking the derivative of the curve in Fig. 5.17, gives the conversion gain of the ED. The gain is shown in Fig. 5.18, with an output in units V/V. When an input voltage of approximately 100 mVp is applied to the input, the gain reaches a value 13.3 dB.

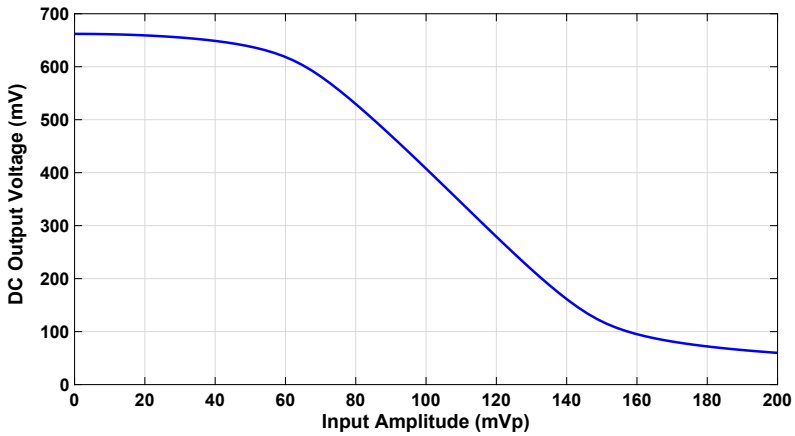


Figure 5.17: Simulated DC output voltage vs. RF input amplitude with frequency of 600 MHz.

5.3.2 Discussion

This section presented the analysis of the ED circuit used in the receiver chain, demonstrating how the employment of the pseudo-differential CS topology achieves a simple structure and maintains low-power consumption. Based on the simulation results, it was shown that the RF signal applied to the input gates needs to be within the range of 60 mV

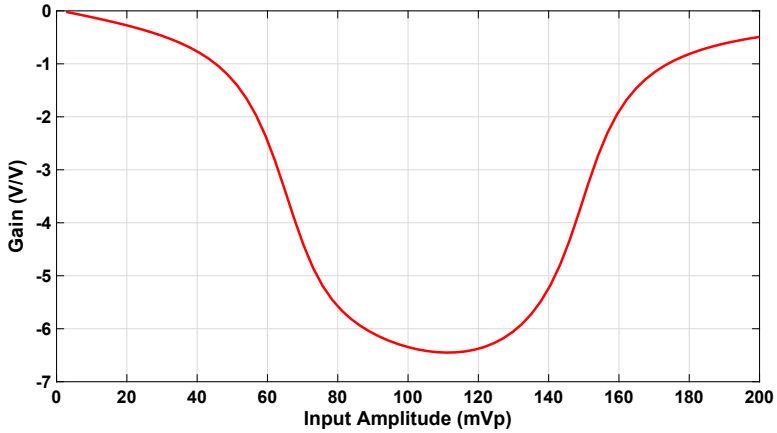


Figure 5.18: Simulated conversion gain of envelope detector.

to 160 mV for proper conversion gain. Since the ILO produces output voltages in the range of about 70 mV to 100 mV, the operation is effective for data recovery. Following this section is the overall performance of the receiver.

5.4 Receiver Performance

In this section, the overall functionality of the receiver is presented, demonstrating the power consumption, energy efficiency, and maximum attainable sensitivity and data rate. To test the data rate performance, first an OOK signal is applied to the input of the receiver with an input power of -60 dBm. Then, a transient analysis is performed to measure the DC output voltage of the ED. An input power of -60 dBm, which is equivalent to 100 nW for a 50 Ω source impedance, is selected to demonstrate the performance of the receiver. The simulation is configured as shown in Fig. 5.19.

The simulation uses a pulse controlled switch connected between the input port and the receiver. The switch is configured to have an ON voltage of 1 V and an OFF voltage of 0 V. The pulse timing parameters used are the period T_s and the pulse on time T_{on}. To test a 5 Mpbs signal, T_{on} is set to 200 ns, and T_s is set to 400 ns. The voltages of the control pulse are set to be 1 V for 200 ns and 0 V for the remaining 200 ns. This will cause the switch connection to turn on and off every 200 ns, emulating a 5 Mpbs OOK signal applied to the

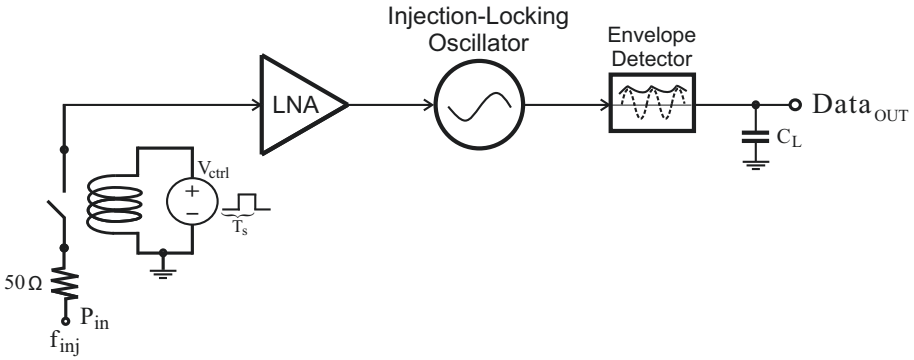
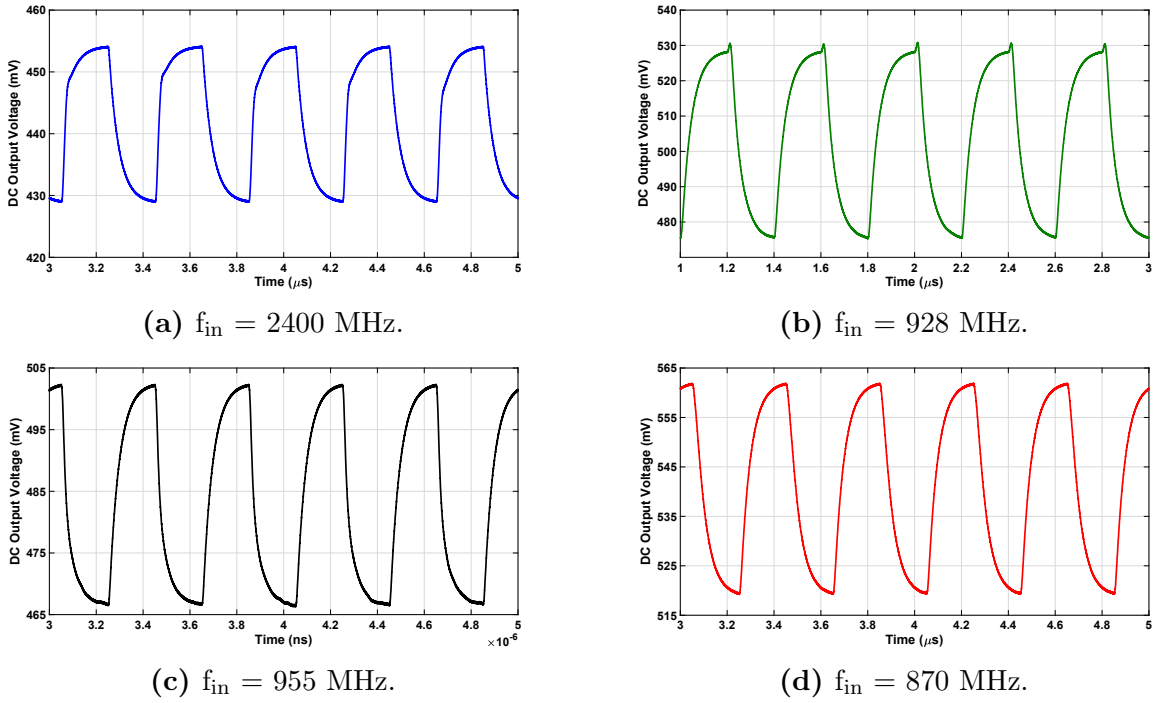


Figure 5.19: Simulation configuration for OOK signal generation.



(a) f_{in} = 2400 MHz.

(b) f_{in} = 928 MHz.

(c) f_{in} = 955 MHz.

(d) f_{in} = 870 MHz.

Figure 5.20: Simulated envelope detector output with a -60 dBm input OOK signal to receiver.

receiver. The mode of the LNA is configured such that it amplifies the frequency interest. Fig. 5.20 depicts the output response of the ED for the 2400 MHz, 950 MHz, 915 MHz, and 863 MHz frequency bands. Observing that the receiver can achieve a data rate of 5 Mbps. Consider Fig. 5.20(a) where the input OOK signal is operating at a frequency of 2400 MHz. After the LNA performs amplification and the ILO locks to the frequency via divide-by-4 superharmonic injection, the output voltage of ILO will decrease causing the DC output

voltage of ED to increase to approximately 455 mV. When the 2400 MHz signal is switched off, the ILO returns back to its free running frequency, causing the ILO output voltage to increase and thus decreasing the DC output voltage of the ED down to approximately 430 mV.

As shown in Fig. 5.21, the 433 MHz band for fundamental injection achieves a data rate of 4 Mbps. The decrease in data rate can be attributed to the extra capacitance within the signal path. The ILO takes longer to lock to the incident signal since there is an additional capacitance at lower frequencies, which increases the time constant. However, a data rate of 4 Mbps remains fast for data extraction and meets the requirements for most applications.

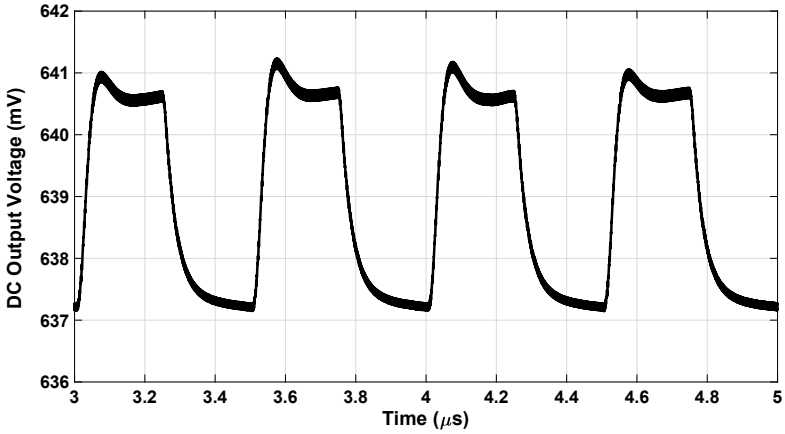


Figure 5.21: Simulated envelope detector output with a -60 dBm input 433 MHz OOK signal to receiver.

Next, a FSK signal is applied to the receiver and a transient analysis is performed to measure the DC output voltage of the ED to determine the data rate performance. The configuration for the simulation is shown in Fig. 5.22. The FSK signal is generated similar to the OOK signal. However, the simulation requires two switches, two ports and two control pulses, that are connected in parallel at the input of the receiver. The ports are set with different frequencies of f_1 and f_2. The differences between the two control pulses are the voltages they produce in their ON and OFF state. This will cause the switches to simultaneously switch ON and OFF, emulating an FSK signal. As seen from Fig. 5.23, the

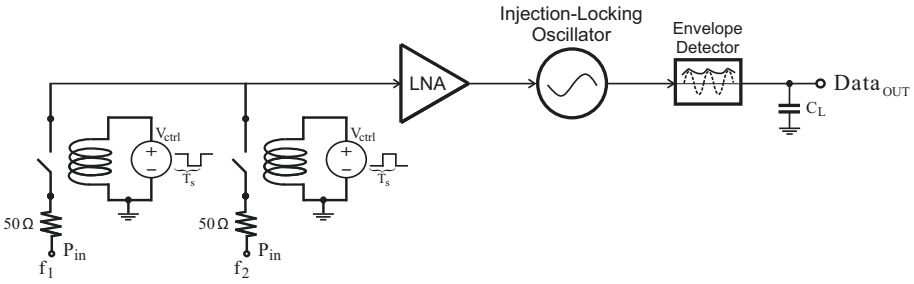
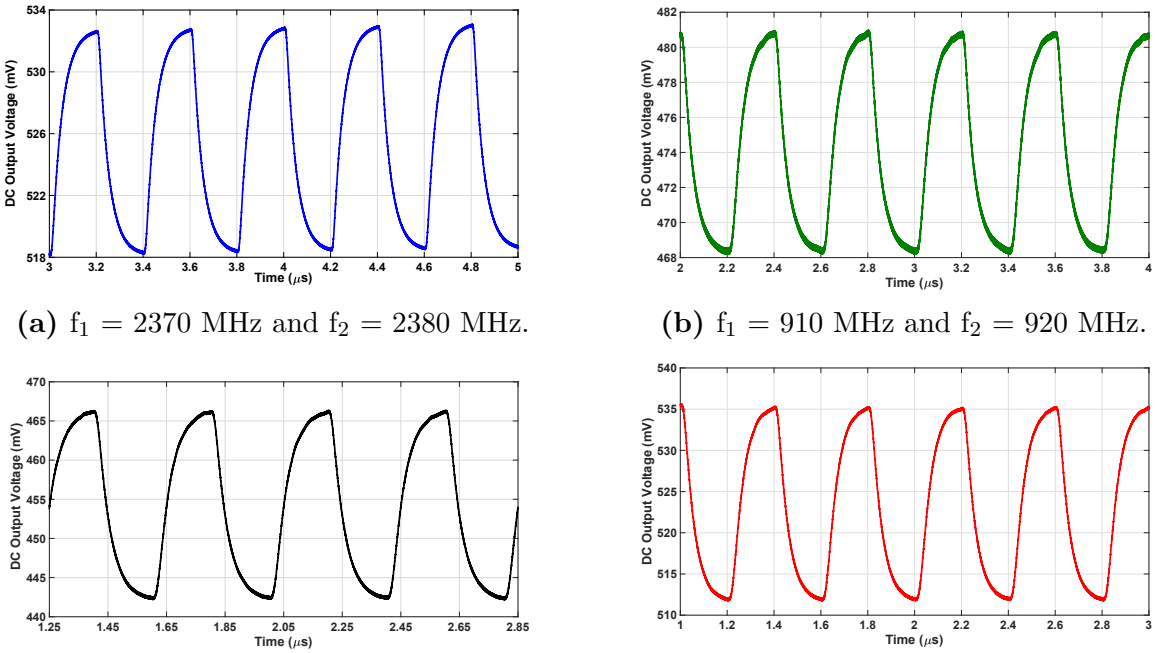


Figure 5.22: Simulation configuration for FSK signal generation.

2400, 950, 915, and 863 MHz frequency bands all achieve a data rate of 5 Mbps. Fig. 5.23(b) depicts the DC output voltage of the ED when the frequency of the FSK signal is 910 and 920 MHz. Observing that the DC voltage transitions from 468 mV to 480 mV.



(a) f_1 = 2370 MHz and f_2 = 2380 MHz.

(b) f_1 = 910 MHz and f_2 = 920 MHz.

(c) f_1 = 950 MHz and f_2 = 960 MHz.

(d) f_1 = 863 MHz and f_2 = 870 MHz.

Figure 5.23: Simulated envelope detector output with a -60 dBm input FSK signal to receiver.

The receiver operates in two modes. The first mode captures the 2.36 - 2.4 GHz frequency band performing divide-by-4 injection, requiring an additional power consumption from the LNA stage due to the buffer stage. The static power consumption is determined

using a DC analysis and the DC current is annotated through the supply voltage. Therefore, with the ILO, LNA, and ED consuming 500 μW, 265 μW, and 7 μW, the total power consumption is 770 μW. And with the data rate of 5 Mbps, the energy/bit is 155 pJ/b. The second mode targets the 433 MHz, 863 MHz, 915 MHz, and 950 MHz frequency bands, performing divide-by-2 and fundamental injection. The 863 MHz, 915 MHz, and 950 MHz bands all achieve a data rate of 5 Mbps, whereas the 433 MHz achieves a data rate of 4 Mbps. In this mode, the buffer stage from the LNA is bypassed and switched off. As a result, the total power consumption is 685 μW, achieving an energy/bit of 137 pJ/b. The highest sensitivity the receiver can achieve is based on whether the ILO can lock the incident frequency detected from the receiver. In the first and second mode, the receiver achieves a sensitivity of -85 dBm and -75 dBm respectively.

5.5 Summary

Table 5.2: State-of-the-art injection-locked based low-power receivers.

Ref.	**Power (μW)**	**Data Rate (Mbps)**	**Sensitivity (dBm)**	**Scheme**	**Energy/Bit (pJ/b)**	**Tech. (nm)**	**Year**
This Work	770/685	5	-85/-75	OOK/FSK	155/137	130	2019
[59]	45	0.312	-62	FSK	145	180	2015
[60]	39	0.2	-55	FSK	195	130	2012
[61]	639	8	-78	FSK	80	130	2015
[62]	54	0.2	-80	OOK/FSK	270	180	2016
[63]	420	5	-73	FSK	84	180	2011

This chapter presented the design of the injection-locked multi-band receiver, implemented in GF 130 nm CMOS technology. Beginning with the design and performance results of the CS cascode and buffer LNA used for signal amplification. Followed by the design of the ILO, demonstrating how the receiver can target multiple frequency bands by accurately setting the tuning frequency range of the ILO and performing various forms of injection-locking.

Next, the ED detector design was shown to extract and interpret the received information. Lastly, the performance of the receiver was shown, which is summarized in Table 4.2. We now make a comparison with state-of-the-art work injection-locked based receiver designs to determine the overall performance of this design. As seen in Table 4.2, this work achieves the highest sensitivity owing to the lock range enhancement technique based on increasing the third-order nonlinearity of the injection transistor. This relaxes the LNA amplification requirements and enables the ILO to lock to smaller input powers. [61] and [63] perform better in the energy/bit metric. However, this receiver can target a total of 5 frequency bands whereas previous work optimizes their design only for a single band, putting fewer constraints on the LNA stage. There is a slight increase in power consumption. This was because, at low-frequency operation, parasitics significantly reduce the output voltage of the ILO, therefore additional biasing current from the tail transistor was necessary to increase the amplitude. The data rate of this work also compares effectively. Additionally, this work performs both OOK and FSK demodulation. Concluding that the design maintains high performance in comparison with state-of-the-art work.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

This work presented the design of a front-end low-power multi-band injection-locked wireless receiver for WSN applications, implemented in GF 130 nm CMOS technology. The receiver is composed of a LNA, ILO, and an ED, targeting the 433 MHz, 863 MHz, 915 MHz, 950 MHz, and the 2.4 GHz frequency bands. The complexity of the receiver design was reduced by making use of the injection-locking technique in the demodulation of OOK and FSK signals. The remarkable ability of the oscillator to lock to incoming signals and to inherently amplify the weak signal was adopted in the design to reduce the power consumption while offering comparable performance. Thanks to the fundamental injection locking, divide-by-2 and divide-by-4 injection locking, modulated signals in multiple frequency bands can be recovered through a single LC oscillator. In this work we also demonstrated a lock range enhancement technique for direct-injection cross-coupled divide-by-4 frequency dividers by utilizing the regenerative frequency divide model which treats the injection transistor as a harmonic mixer composed of a pure multiplier and nonlinear block. With this approach, a mathematical model that shows that the divide-by-4 lock range is proportional to the third-order nonlinear coefficient was exploited. An examination of transistors in the weak and strong inversion region was performed, demonstrating that since transistors in the weak inversion region exhibit severe nonlinear characteristics, the injection transistor biased in the subthreshold region results in a wider lock range as opposed to biasing the transistor in the

strong inversion region. In addition, the discovery of an optimal biasing point was shown, located at the peak of the third-order nonlinear coefficient, resulting in the highest attainable divide-by-4 lock range [80]. From this nonlinear relationship, we further presented how to increase the third-order coefficient via body effect and p-well injection using triple-well NFET device. This allowed extending the lock range further by increasing both the nonlinear properties of the harmonic mixer and the applied injection power. Moreover, the lock range of divide-by-2 affected by the first-order and third-order coefficient of the nonlinearity was explored in detail, providing a great deal of intuition that is necessary in this design. By utilizing these lock range enhancement techniques in the receiver design process, both low-power and high sensitivity were achieved. With two modes of operation, the receiver consumes a total of 770 μW and 685 μW of static power. The first mode targets the 2.4 GHz frequency band, attaining a sensitivity of -85 dBm and a FOM of 155 pJ/b. The second mode targets the 433 MHz, 863 MHz, 915 MHz, and 950 MHz frequency bands, attaining a sensitivity of -75 dBm and FOM of 137 pJ/b. A comparison is made with state-of-the-art injection-locked based designs, resulting in a high-performance receiver.

This work also presented CS-based 35 μW LNA implemented in GF 130 nm CMOS technology operating under a 0.7 V supply. The LNA consists of a NFET transistor that is optimally biased for gain, power, and bandwidth efficiency. Then, it was shown how an accurately sized PFET load, operating in the strong inversion region, reduces the nonlinearity of the LNA by compensating the third-order gain expansion properties of the NFET device. This technique ensured that the trade-off between linearity, voltage gain, and power performance does not suffer, which resulted in the highest classical FOM compared with state-of-the-art work. The simulated voltage gain, IIP3, P_{1dB}, and NF are 15.7 dB, -6.5 dBm, -17.5 dBm and 5.7 dB respectively.

6.2 Future Work

Completing the remaining work of the layout for the receiver is the next design stage. The pre-finalized version of the layout is shown in Appendix D, Fig. D.1, with only the DRC

completed. The dimensions of the chip are 1.5 mm by 1.5 mm. The next step is to pass the LVS and perform post-layout simulations. Then, to improve the overall functionality, the digital control circuity would be implemented to operate the switches and fine tune the varactors. Additionally, an alternative LNA design may be investigated to reduce the amount of on-chip inductors. This could be achieved by replacing the passive inductors with active inductors.

It was shown how the performance of the receiver relies on nonlinear properties of both the ILO and ED. In addition to the injection transistor being in the nonlinear region, the cross-coupled pair may also be in a bias conditioning to exhibit high third-order nonlinearity. This may also further extend the lock range in the case for divide-by-4.

Furthermore, the regenerative frequency divide-model suggests that the lock range can also be extended for subharmonic injection-locking used for frequency multipliers. The multiply-by-4 lock range is similar to divide-by-4 in the case of the proportionality of the third-order nonlinear coefficient. This may suggest that the lock range is maximized using the same techniques presented for superharmonic injection. In addition, various types of oscillators, e.g., ring, Colpitts, etc., that do not have differential properties, may benefit for performing divide-by-3 or multiply-by-3 super and subharmonic injection. This is because it was shown that lock range for the divide-by-3 case is proportional to the second-order coefficient and since single-ended configurations do not exhibit small-second order coefficients, an optimal biasing point may be located at the peak of the second-order coefficient to maximize the lock range.

Appendix A

Circuit Schematics

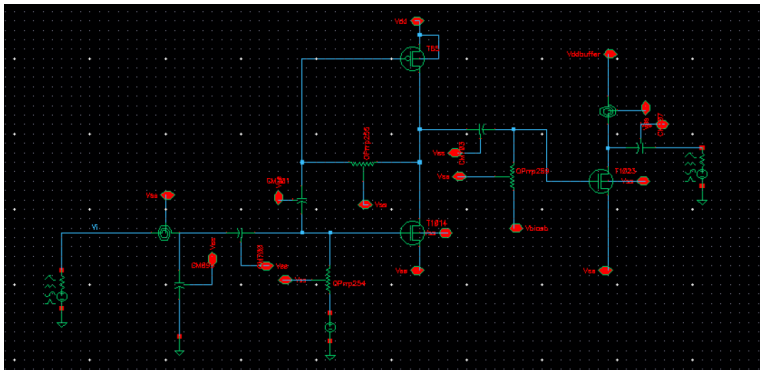


Figure A.1: Cadence schematic view of uitra-low-power LNA.

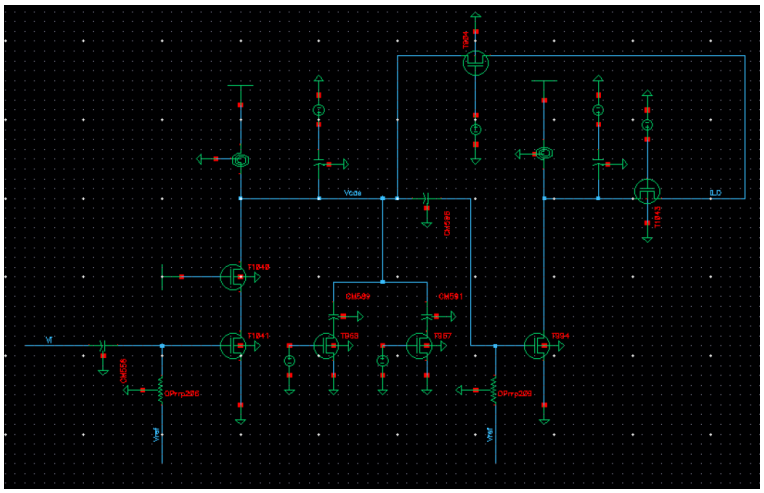


Figure A.2: Cadence schematic view of LNA.

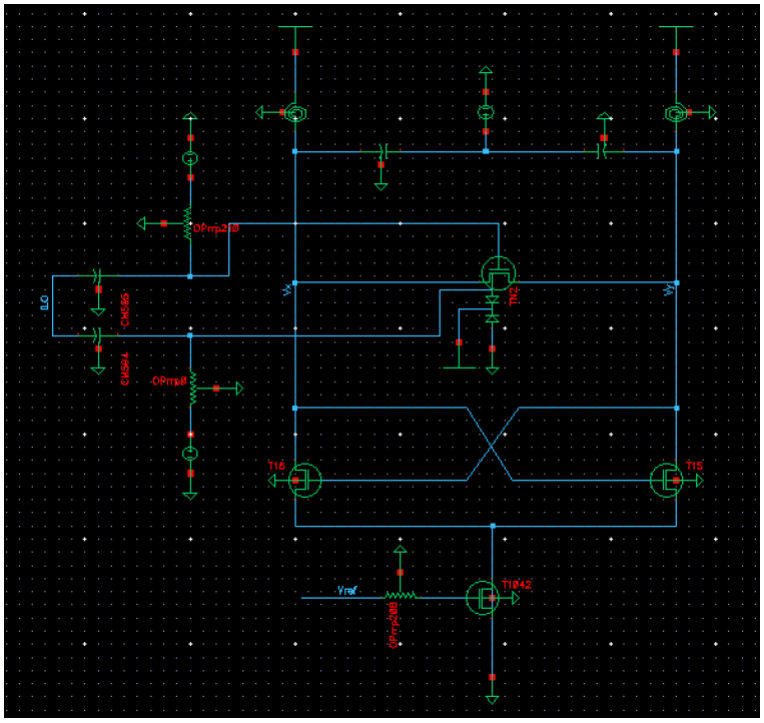


Figure A.3: Cadence schematic view of injection-locked oscillator.

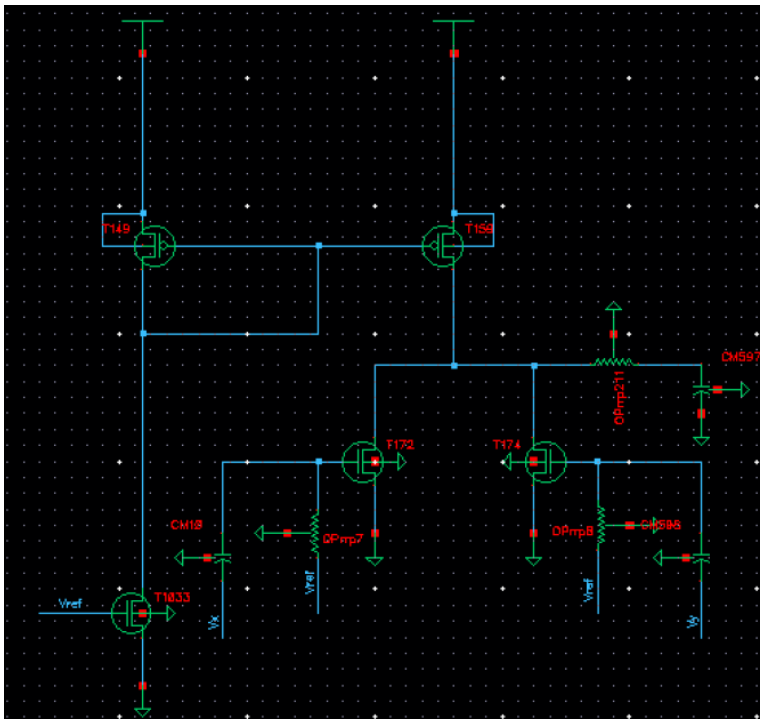
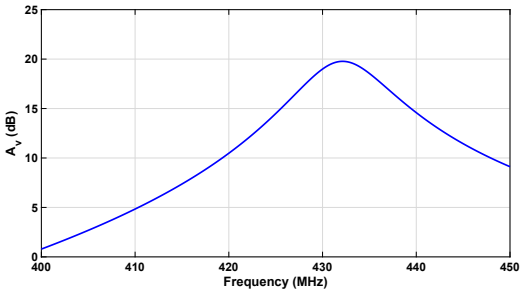


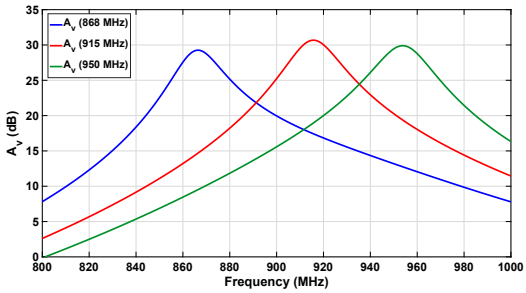
Figure A.4: Cadence schematic view of envelope detector.

Appendix B

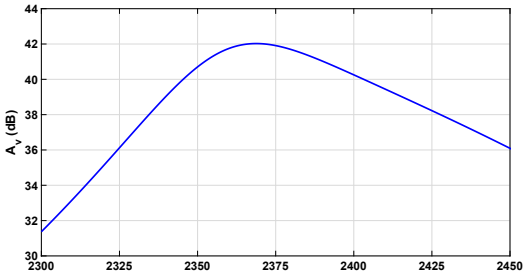
Simulated Waveforms



(a) Simulated voltage gain for the 433 MHz frequency band.



(b) Simulated voltage gain for the 863, 915, and 950 MHz frequency bands.



(c) Simulated voltage gain for the 2.4 GHz frequency band.

Figure B.1: Simulated voltage gains for targeted frequency bands.

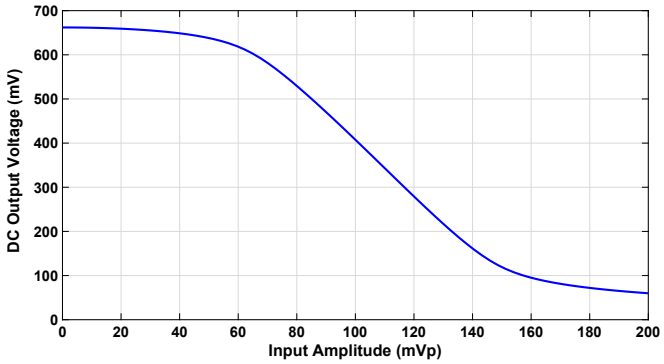
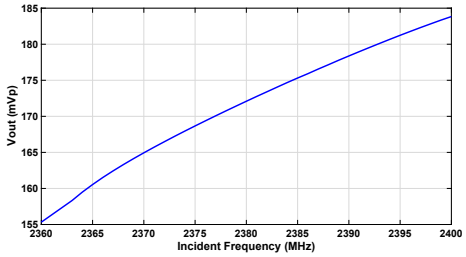
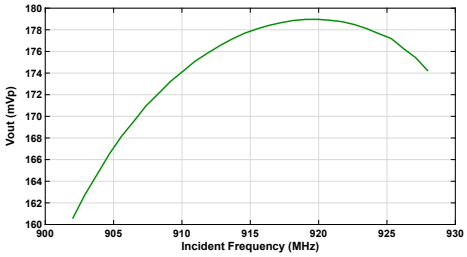


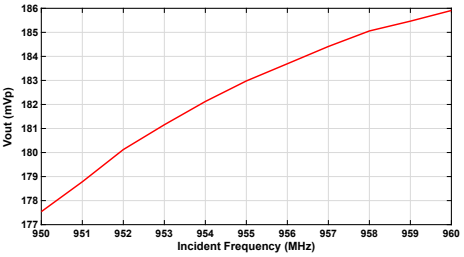
Figure B.2: Simulated DC output voltage vs. RF input amplitude with frequency of 600 MHz.



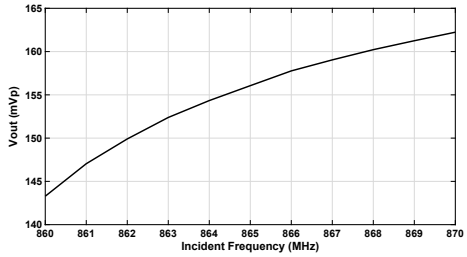
(a) Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 597$ MHz.



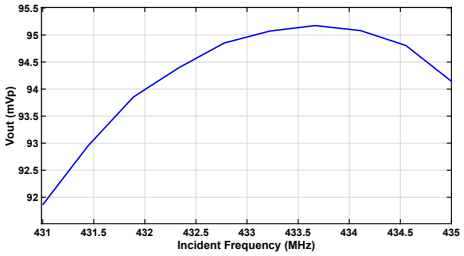
(b) Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 460$ MHz.



(c) Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 479$ MHz.

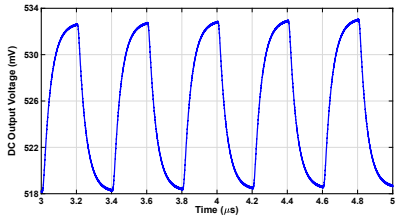


(d) Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 435$ MHz.

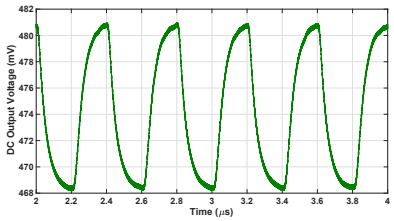


(e) Simulated incident frequency vs. output voltage. $P_{in} = -50$ dBm and $f_c = 434$ MHz.

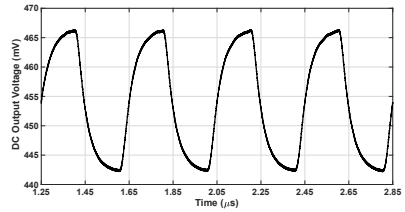
Figure B.3: Frequency-to-amplitude conversion of injection-locked oscillator.



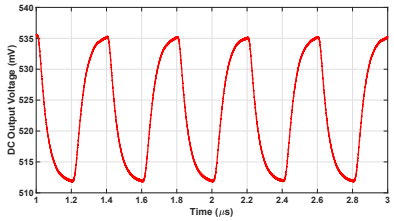
(a) f_1 = 2370 MHz and f_2 = 2380 MHz.



(b) f_1 = 910 MHz and f_2 = 920 MHz.

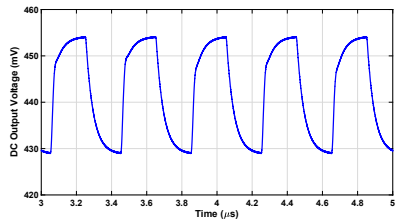


(c) f_1 = 950 MHz and f_2 = 960 MHz.

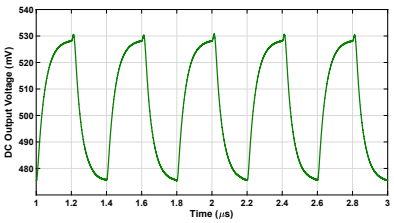


(d) f_1 = 863 MHz and f_2 = 870 MHz.

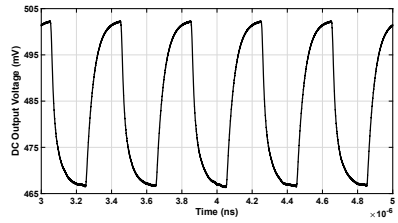
Figure B.4: Simulated envelope detector output with a -60 dBm input FSK signal to receiver.



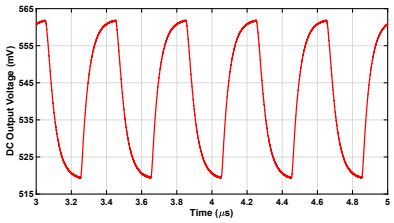
(a) f_{in} = 2400 MHz.



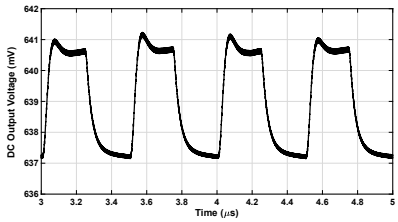
(b) f_{in} = 928 MHz.



(c) f_{in} = 955 MHz.



(d) f_{in} = 870 MHz.



(e) f_{in} = 433 MHz.

Figure B.5: Simulated envelope detector output with a -60 dBm input OOK signal to receiver.

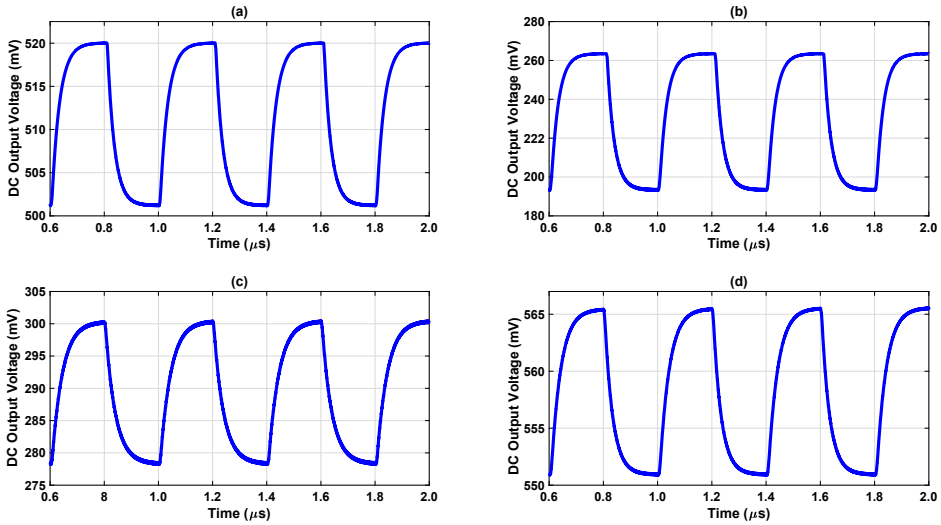


Figure B.6: Simulated envelope detector output for process corners with 2.4 GHz OOK signal applied to receiver: (a) FF (fast nMOS/fast pMOS), (b) FS (fast nMOS/slow pMOS), (c) SF (slow nMOS/fast pMOS), and (d) SS (slow nMOS/slow pMOS).

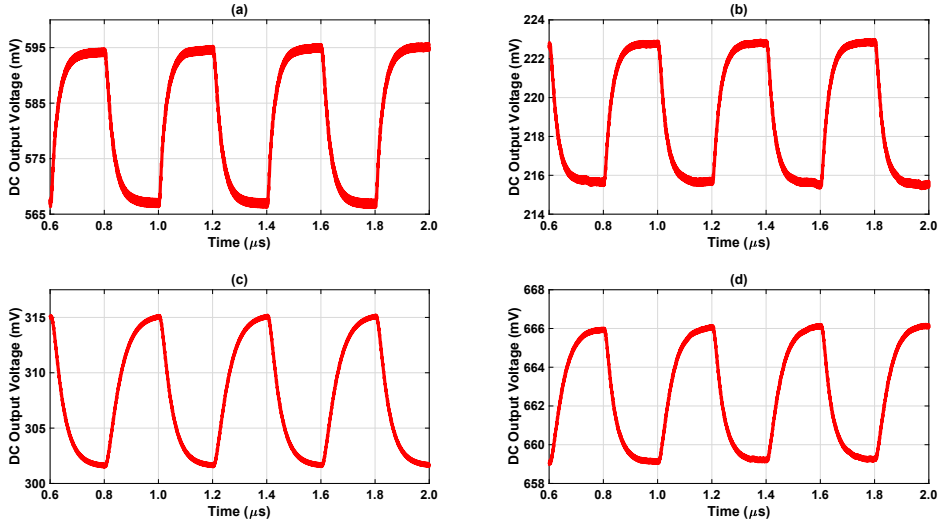


Figure B.7: Simulated envelope detector output for process corners with 2.4 GHz FSK signal applied to receiver: (a) FF (fast nMOS/fast pMOS), (b) FS (fast nMOS/slow pMOS), (c) SF (slow nMOS/fast pMOS), and (d) SS (slow nMOS/slow pMOS).

Appendix C

MATLAB Code

```
clc;
syms gm1 Rp1 ro1 ro2 gm2 gmb2 Vx Vy Vo s Cgs1 Cgd1 gm1 ro1 Cgs2 gm2 ro2 Zout Ix gm3 ro3 Rp3 Cgd2 k T gamma Rp2 Rs

Av2 = -gm2*(ro3*Rp2/(ro3+Rp2));
Av1 = -gm1*1/((1/Rp1)+(1/(ro1+ro2+(gm2+gmb2)*ro1*ro2)));
Rout1 = 1/((1/Rp1)+(1/(ro1+ro2+(gm2+gmb2)*ro1*ro2)));

%Input Impedance Cascode%
EQ1 = Vx*s*Cgs1 + (Vx-Vy)*s*Cgd1 == Ix;
EQ1 = solve(EQ1,Vy);
Vy = (Cgd1*Vx*s - Ix + Cgs1*Vx*s)/(Cgd1*s);
EQ2 = Vy/ro1 + gm1*Vx + gm2*Vy == (Vx-Vy)*s*Cgd1;
EQ2 = solve(EQ2,Vx);
EQ2 = simplify(EQ2/Ix);
Zin1 = EQ2;

%Input Impedance Buffer%
EQ1 = Vx*s*Cgs2 + (Vx-Vy)*s*Cgd2 == Ix;
EQ1 = solve(EQ1,Vy);
Vy = (Cgd2*Vx*s - Ix + Cgs2*Vx*s)/(Cgd2*s);
EQ2 = Vy/ro3 + gm3*Vx + Vy/Rp3 == (Vx-Vy)*s*Cgd2;
EQ2 = solve(EQ2,Vx);
EQ2 = simplify(EQ2/Ix);
Zin2 = EQ2;

%Noise Stage 1%
SvoRp1 = 4*k*T*Rp1*(((ro1+ro2+(gm2+gmb2)*ro1*ro2)/(ro1+ro2+(gm2+gmb2)*ro1*ro2+Rp1))^2);
SvoM1 = 4*k*T*gamma*gm1*(Rout1^2);
SvoM2 = 4*k*T*gamma*gm2*(((Rp1*ro2)/(Rp1+ro1+ro2+gm2*ro2))^2);
SvoCAS = SvoM1 + SvoM2 + SvoRp1;

%Noise Stage 2%
SvoRp2 = 4*k*T*Rp2*(((ro3)/(ro3+Rp2))^2);
SvoM3 = 4*k*T*gamma*gm3*((Rp3*ro3)/(Rp3+ro3)^2);
SvoBuff = SvoM3 + SvoRp2;

alpha1 = Zin1/Zin1+Rs;
alpha2 = Zin2/Zin2+Rout1;

F1 = SvoCAS/(4*k*T*Rs*((Av1)^2)*(alpha1)^2);
F2 = SvoBuff/((Av2*Av1*alpha1*alpha2)^2*4*k*T*Rs);
F = 1 + F1 + F2;

```

Figure C.1: MATLAB code for circuit analysis of cascode and buffer amplifiers.

```
syms Vx Ix s Zf Zl gm ro RF Cgd CL Cgs Vo w
clc;

ZL = (ro/(1+s*CL*ro)); % ro||CL
ZF = (RF/(1+s*Cgd*RF)); % RF||Cgd
EQ1 = Ix == (Vx-Vo)/((RF/(1+s*Cgd*RF)));
EQ2 = (Vx-Vo)/((RF/(1+s*Cgd*RF))) == gm*Vx + Vo/((ro/(1+s*CL*ro)));
EQ2 = solve(EQ2,Vo);
Vo = -(Vx*gm - (Vx*(Cgd*RF*s + 1))/RF)/((CL*ro*s + 1)/ro + (Cgd*RF*s + 1)/RF);
EQ3 = Ix == (Vx-(-(Vx*gm - (Vx*(Cgd*RF*s + 1))/RF)/((CL*ro*s + 1)/ro + (Cgd*RF*s + 1)/RF)))/((RF/(1+s*Cgd*RF)));

Zin = expand(solve(EQ1,Vx));
Zin = simplify(Zin/Ix);
```

Figure C.2: MATLAB code for input impedance derivation of ultra-low-power LNA.

```
clc;
syms Vi Vs Vo w Zf ZL CL gm ro RF Rs Cgd Cgs k T s gammma Ix Vx i

% Active Pair
Num = ro*RF + ro*Rs +  w*i^2*Cgd*RF*Rs*ro +  w*i^2*Cgs*RF*Rs*ro;
Alpha = RF + Rs + ro + Rs*gm*ro;
Beta =  w*i^2*(Cgd*RF*Rs + Cgs*RF*Rs + CL*RF*ro + Cgd*RF*ro + CL*Rs*ro + Cgs*Rs*ro + Cgd*RF*Rs*gm*ro);
Gamma = w^2*i^2*(CL*Cgd*RF*Rs*ro + CL*Cgs*RF*Rs*ro + Cgd*Cgs*RF*Rs*ro);
Den = Alpha + Beta + Gamma;
Zout = simplify(expand((Num/Den))^2);
NFm = Zout*4*k*T*gamma*gm;

% RS
Num = w*i^2*ro*Cgd*RF - RF*gm*ro + ro;
Alpha = RF + Rs + ro + Rs*gm*ro;
Beta = w*i^2*(Cgd*RF*Rs + Cgs*RF*Rs + CL*RF*ro + Cgd*RF*ro + CL*Rs*ro + Cgs*Rs*ro + Cgd*RF*Rs*gm*ro);
Gamma = w^2*i^2*(CL*Cgd*RF*Rs*ro + CL*Cgs*RF*Rs*ro + Cgd*Cgs*RF*Rs*ro);
Den = Alpha+Beta+Gamma;
Av = (Num/Den)^2;
NFRS = Av*4*k*T*Rs;

% RF
Num =  RF*ro*Rs*gm + w*i^2*RF*ro*Cgs*Rs + RF*ro;
Den = (RF+Rs+ro+Rs*gm*ro) + w*i^2*(Cgd*RF*Rs+Cgs*RF*Rs+CL*RF*ro+Cgd*RF*ro+CL*Rs*ro+Cgs*Rs*ro+Cgd*RF*Rs*gm*ro) + w^2*i^2*(CL*Cgd*RF*Rs*ro + CL*Cgs*RF*Rs*ro + Cgd*Cgs*RF*Rs*ro);
NFRF = ((Num/Den)^2)*(4*k*T/RF);

pretty((simplifyFraction(factor(expand(NFRF/NFRS)))))
```

Figure C.3: MATLAB code for noise figure derivation of ultra-low-power LNA.

Appendix D

Layout

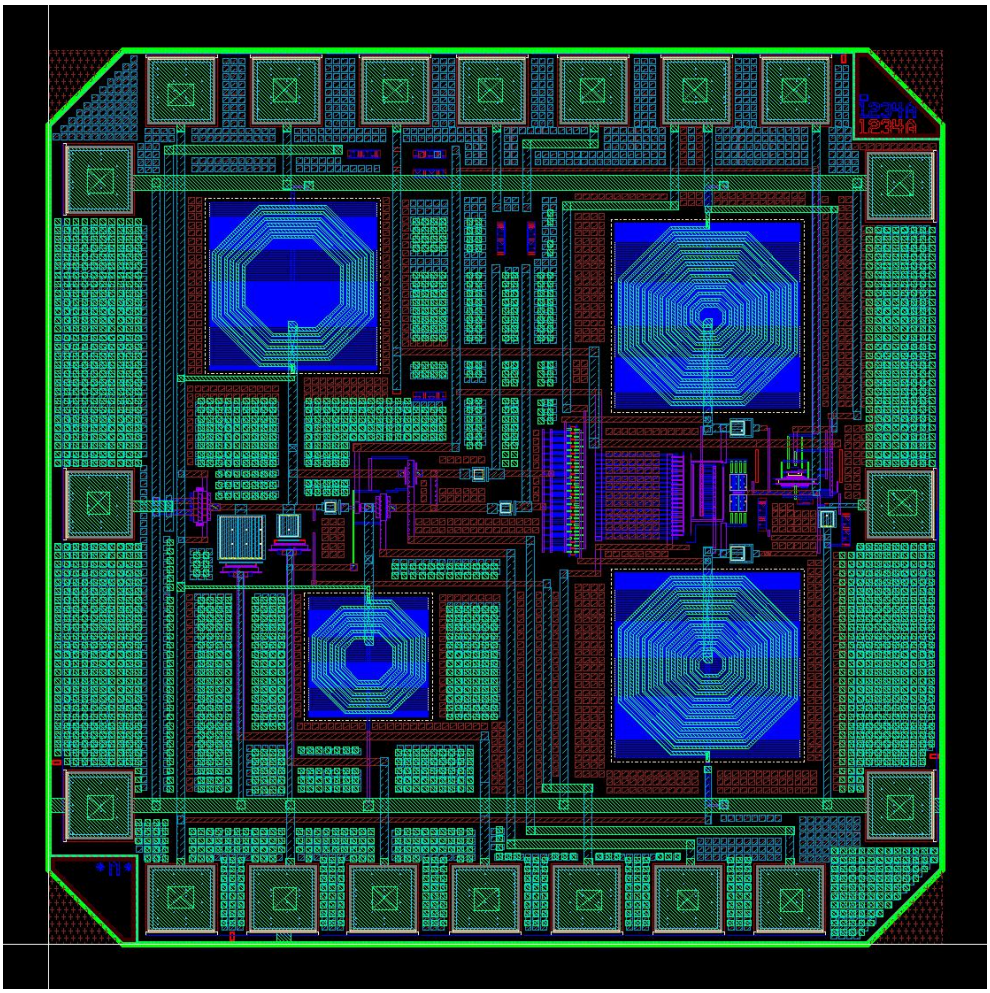


Figure D.1: Pre-finalized layout view of receiver.

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