Design Methodology for Class D Ultrasound Transducer Drivers

by

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Abstract

Ultrasound refers to sound waves with frequencies above the upper limit of human hearing. Due to the high frequency, the energy can be concentrated and used for therapeutic applications, such as ultrasound imaging and therapeutic devices. This thesis focuses on the design of driving circuits for ultrasound transducers. The Class D amplifier loaded with a piezoelectric ultrasound transducer is analyzed, and a design methodology is developed. The resulting design achieves high efficiency and can handle transducer impedance variations by adjusting two capacitances in the matching network. The amplifier topology is simple and low-cost. If this design is implemented in the lab, it will require a variable DC voltage supply, a gate driver, two NMOSs, an L-C filter, and a parallel capacitor.

A reference design to drive disc-shaped transducers with a radius of 20 mm, and a thickness of 2.8 mm, made of piezo-composite crystal, is presented to illustrate the design methodology. The resulting amplifier can provide a power of near 50 W at 1034 kHz with 97 % efficiency when driving six different transducer samples. The analysis and design methodology are validated by simulating the amplifier performance in LTSpice and a corner analysis considering matching network component variations.

Acknowledgments

I would like to thank my supervisor, Dr. Carlos Christoffersen, and my co-supervisor, Dr. Yushi Zhou, for the invaluable opportunity to do this research. They gave me a great deal of academic support and taught me more than this paper can encapsulate. I would also like to thank my family members for their love and financial support. Finally, thanks to Misty Wu for being a good friend and supporting me through these tough times.

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B_s – Susceptance of the series branch.
C_{ds} – Drain-to-source capacitance.
C_f – Filter capacitor.
C_o – Parallel capacitor in the transducer.
C_p – Parallel capacitance.
C'_p – Nominal parallel capacitor.
C_s – Series capacitance.
D – Duty cycle.
D_{min} – Minimum duty cycle.
$D1$ – Parallel diode one.
$D2$ – Parallel diode two.
E_{po} – Output power error between simulation and calculation.
E_{PLoss} – Total power loss error between simulation and calculation.
E_η – Overall efficiency error between simulation and calculation.
f – Frequency (Hz).
f_o – Operating frequency (Hz).
f_p – Parallel resonance frequency (Hz).
f_s – Series resonance frequency (Hz).
f_{sw} – Switching frequency (Hz).
G_s – Conductance of the series branch.
I_{CC} – Quiescent current.
I_{DC} – DC Drain current.
I_{HB} – HB quiescent current.
I_{HBS} – High-side to low-side leakage current.
$I_m(Z_s)$ – The imaginary component of the series branch.
$I_m(Z_t)$ – The imaginary component of the transducer.

I_p – The peak current of the inductor.
I_1 – The fundamental drain current.
i_{C1} – Parallel current of S1.
i_D – Drain current.
i_{DP} – Peak value of drain current.
i_{D1} – Current of diode is in parallel of S1.
i_{D2} – Current of diode is in parallel of S2.
i_L – Inductor current.
i_o – The series branch current.
i_Q – The biasing current.
i_s – Amplitude of the fundamental component of the drain current.
i_{s1} – Instantaneous current of S1.
i_{s2} – Instantaneous current of S1.
L_f – Filter inductor.
L_s – Series inductance.
P_D – Power consumption of the transistor.
P_{D2} – Diode D2 power loss.
P_{Dmax} – Maximum power of the transistor.
P_{IHBS} – Static level-shifter power.
P_{in} – Input power.
P_G – Gate drive power.
P_L – Average inductor power consumption.
P_{LS} – Dynamic level-shifter level-shifter power.
P_{Loss} – Total power loss.
P_{Lossc} – Total calculation power loss.
P_{Losss} – Total simulation power loss.
P_m – Mosfet power consumption.
P_o – Output power.
P_{oc} – Calculation output power.
P_{os} – Simulation output power.
P_{QG} – Dynamic gate power.
P_{sw} – Switch condcution power.

Q – Quality factor.
Q' – Actucal calculated quality factor.
q_p – Parasitic level-shifter charge.
q_g – Gate charge.
q_d – Total drain charge.
R – Output resistance.
$R_e(Z_s)$ – The real component of the transducer of series branch.
$R_e(Z_t)$ – The real component of the transducer.
R_{eq} – The real component of the impedance of the transducer and filter capacitor.
R_{GATE} – External gate drive resistance.
R_{GD} – Average pull-up and pull down resistance.
R_{GFET} – MOSFETs' internal gate resistance.
R_{in} – The input impedance of the load.
r_{ds} – Transistor turn-ON resistance.
r_L – Inductor resistance.
R_s – Series resistance.
R_t – Transducer equivalent resistance.
R'_t – New transducer equivalent resistance.
$R_{\theta JA}$ – Junction-to-ambient thermal resistance.
S_1 – Upper switch.
S_2 – Bottom switch.
T_J – Recommended maximum operating junction temperature.
T_A – Ambient temperature of the gate driver.
t – time.
t_{ON} – Turn-ON time.
V_{CC} – Driver supplyy voltage.
V_{DD} – Supply voltage.
V_{D2} – Diode D2 voltage.
V_{dd} – Supply voltage.
V_{DH} – Booststrap diode forward voltage.
V_{ds} – Drain-to-source voltage.
V_{ds1} – Drain-to-source voltage of S1.

V_{ds2} – Drain-to-source voltage of S2.
V_{gs} – Gate-to-source voltage.
V_{HB} – High-sdie bootstrap supply voltage.
V_{in} – Input voltage of the load.
V_L – Inductor voltage.
V_o – Output voltage.
V_p – Peak-to-peak voltage of the input voltage of the load.
V_{pp} – Peak-to-peak voltage.
V_{th} – Thresehold voltage.
V_1 – The fundamental component of the drain voltage.
X_{eq} – The imaginary part of impedance of the transducer and filter capacitor.
X_{in} – The imaginary part of input impedance of the load.
X_t – The imaginary part of impedance of the transducer.
X_t' – The new imaginary part of impedance of the transducer.
Y_s – Adimittance of the series resonant branch.
Z – The equivalent impedance of the transducer.
$|Z|$ – The magnitude impedance of the transducer.
Z_{eq} – The equivalent impedance of the transducer and filter capacitor.
Z_{in} – Input impedance of the load.
Z_{in}' – Nominal input impedance of the load.
$|Z_{in}|$ – The magnitude impedance of the load.
$|Z_{in}'|$ – The nominal magnitude impedance of the load.
Z_s – Impedance of the series branch.
$|Z_s|$ – The magnitude impedance of the series branch.
Z_t – Equivalent impedance of the transducer.
$Z_t{}'$ – New equivalent impedance of the transducer.

α – Load factor.
θ_a – Conduction time in phase.
θ_c – Conduction angle.
θ_1 – Diode conduction.
ω – angular frequency.

ϕ – Current and voltage phase displacement.
η – Overall efficiency.
η_c – Calculated overall efficiency.
η_{max} – Maximum efficiency.
η_s – Simulation overall efficiency.

List of Abbreviations

BVD – Butterworth Van Dyke.
CMOS – Complementary Metal-Oxide Semiconductor.
CMUT – Capacitive Micromachined Ultrasonic Transducer.
HIFU – High Intensity Focused Ultrasound.
LCR – Inductor-Capacitor-Resistor.
LIPUS – Low-Intensity Pulsed Ultrasound.
MOSFET – Metal-Oxide Semiconductor Field-Effect Transistor.
NMOS – N-channel MOSFET.
PMOS – P-channel MOSFET.
PWM – Pulse width modulation.
RC – Resitor-Capacitor.
RF – Radio Frequency.
TSLs – Thermosensitive liposomes.
TTL – Transistor-Transistor Logic.
ZDS – Zero Derivative Switching.
ZVS – Zero Voltage Switching.

Chapter 1

Introduction

1.1 Motivations and Objectives

Sound waves are generated by mechanical vibration. Ultrasound refers to the vibration frequencies of sound waves that are greater than 20kHz; it is above the upper limit of human hearing. At high intensities, the energy is easily concentrated and used for therapeutic applications. Ultrasound produces biological effects that apply to low power and high power therapy ultrasound applications. The low power applications include physiotherapy, fracture repair, sonophoresis, sonoporation, and gene therapy. The most common high power application is high intensity focused ultrasound. The absorption of ultrasonic energy causes thermal effects and non-thermal effects [1]. Thermal effects of ultrasound are enabled to increase the efficacy of drug therapies [2]. Drugs are encapsulated by thermosensitive liposomes (TSLs), which are released by thermal effects of ultrasound to the desired region [3]. Other body parts avoid unwanted effects because drugs effectively deliver to the target organ and less medication in the blood. Non-thermal effects of ultrasound

can temporarily increase the permeability of biological barriers by acoustic cavitation. For example, ultrasound is to increase the permeability of the blood-brain barrier to treat the brain organ. The permeability of cell membranes also can be increased by the same technique. Kivinen developed a prototype device for a large molecule delivery *in vitro* using ultrasound, producing cavitation at a high power level [4]. It is helpful to explore the potential of this technology for targeted therapies in sonoporation.

An ultrasound transducer is a device that converts electrical energy into ultrasound energy. Typical ultrasonic transducers are piezoelectric transducers, capacitive transducers, and magnetostrictive transducers. Piezoelectric transducers comprise piezoelectric crystals, oscillating at a specific frequency to produce ultrasound [5, 6]. The conductive diaphragm of capacitive transducers vibrates in the electrical fields at high frequencies. Magnetostrictive transducers use iron-rich metals that expand and contract in a variable magnetic field. Radio-frequency (RF) power amplifiers drive ultrasound transducers and amplifiers to cooperate with a given transducer. For example, the electrical model of the sonoporation device consists of a set of piezoelectric transducers and specific driving circuits [4]. Kivinen designed a Class DE amplifier. However, this amplifier is sensitive to impedance variations, which will affect design flexibility. Hence, a Class D amplifier is used in this thesis.

The advantages of the Class D amplifier are ideal 100% efficiency, simple topology, and variations in impedance to the load. Class D amplifiers are commonly used to drive ultrasound transducers in [9–19, 21–24, 26, 27]. In these applications, there is no explicit design methodology for Class D am-

plifiers. This thesis presents a design methodology for Class D amplifiers driving piezoelectric transducers. The methodology can be applied in the sonoporation system [4], which comprises a set of six ultrasound transducers operated at frequencies close to 1MHz. Simulation results for all six transducers verify design performance and the circuit analysis, including analysis for components parameter variations. This proposed amplifier can provide approximately up to 50W at 1034kHz with a power efficiency of 97%. This design is low-cost, power-efficient, and tolerant to variations in component values and transducer impedance.

1.2 Thesis Overview

Chapter 2 illustrates the basic information about power amplifiers and reviews the literature on power amplifiers for piezoelectric transducers loads. Chapter 3 analyzes the proposed Class D ultrasound driver and presents the design methodology demonstrated in the sonoporation system to the transducers. Chapter 4 summarizes the conclusions of this thesis and suggests future work.

Chapter 2

Literature Review and Basic Concepts

2.1 Introduction

Power amplifiers, such as Class A, Class D, and Class DE amplifiers, commonly drive ultrasound transducers. However, Class A amplifiers are less efficient. Other published works that provide high efficiencies, such as Class D amplifiers or other types of amplifiers, for driving piezoelectric transducer loads, will be reviewed. This chapter is organized as follows: Section 2.2 illustrates the basic concepts of different power amplifiers, and Section 2.3 covers the electrical model of the ultrasound transducer. Section 2.4 reviews previously published works.

2.2 Background of Power Amplifiers

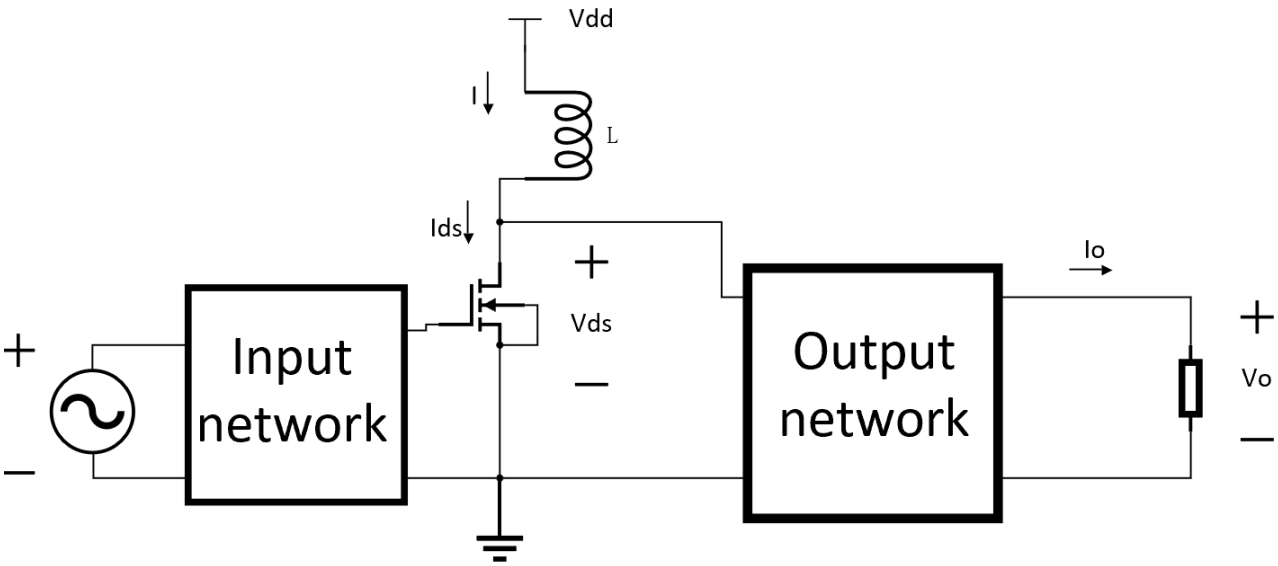

Figure 2.1: A diagram of an RF power amplifier [7].

The diagram of the RF power amplifier is shown in Figure 2.1. Radio-frequency (RF) power amplifiers consist of an RF choke, a MOS transistor, an input network, and an output network. In the circuit, the transistor can work as a dependent current source or a switch. If the transistor operates as a dependent current source, this amplifier is called a current-mode amplifier; if the transistor operates as a switch, the amplifier is called a switch-mode amplifier [7] [8]. The basic concepts of different mode amplifiers will be explained as follows.

2.2.1 Current-mode Power Amplifiers

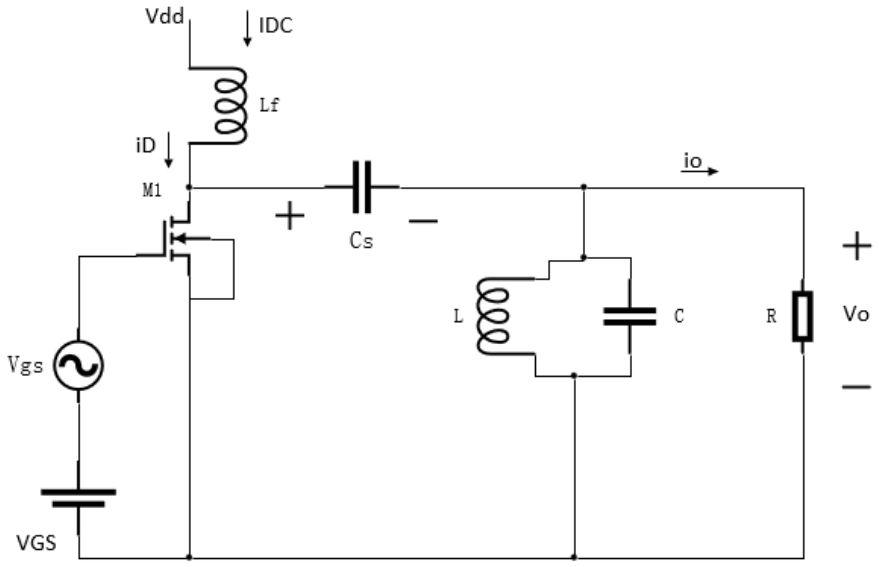

Figure 2.2: A schematic of the Class A, Class B, and Class C amplifier [7].

The general schematic of the current-mode amplifier is shown in Figure 2.2, which is connected to the capacitor, the impedance tuning network, and the load. The classification of current-mode amplifiers is based on the conduction angle of the drain current and biasing conditions. The transistor operates as a dependent current source, which is controlled by the gate-to-source voltage V_{gs}. Conduction angles vary between different classes of amplifiers as follows: the transistor of Class A conducts the whole cycle ($\theta_c = 360°$), the transistor of the Class B amplifier conducts half a cycle ($\theta_c = 180°$), and that of Class C conducts less than a half cycle ($\theta_c < 180°$). Figure 2.3 illustrates the relationship between the drain current i_D of current-mode amplifiers and conduction angles [7].

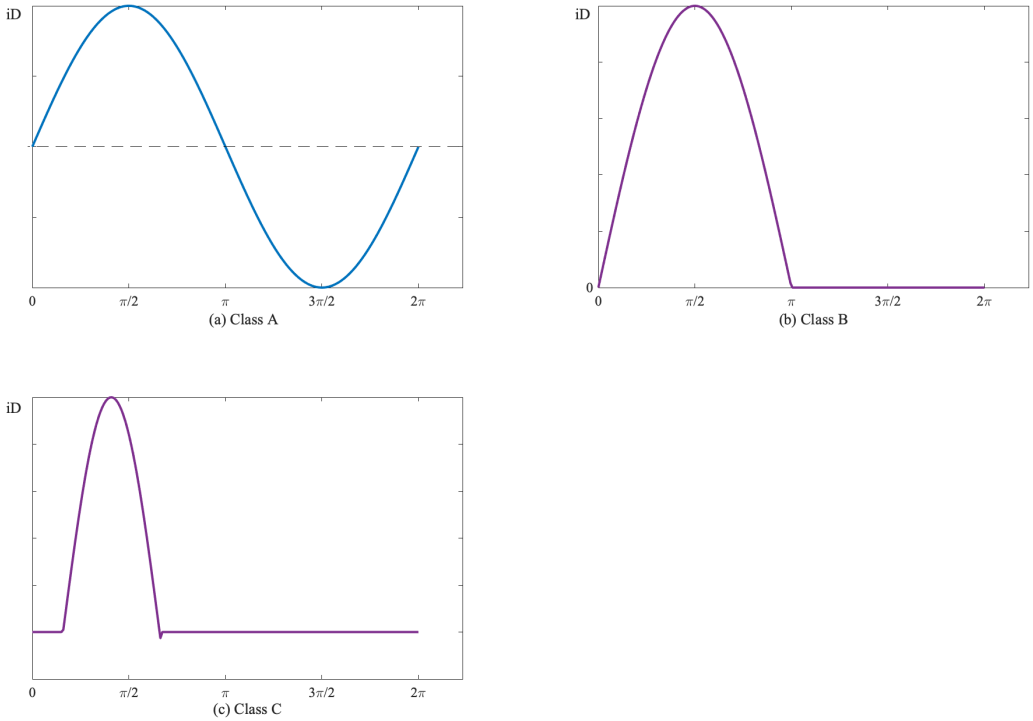

Figure 2.3: Waveforms of the drain current i_D of different class operations: (a) Class A, (b) Class B; (c) Class C.

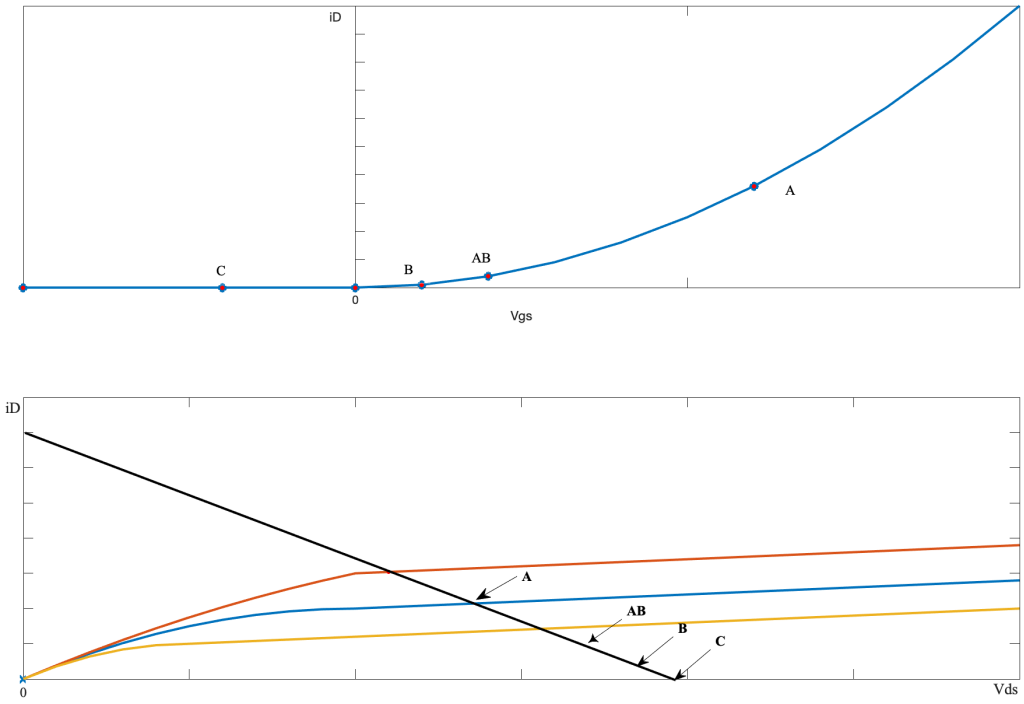

Figure 2.4: The operating points of different classes of amplifiers.

Figure 2.4 shows the operating points of the current-mode amplifiers [7]. The gate-to-source voltage V_{gs} of the transistor in the Class A amplifier is greater than the threshold voltage V_{th}, and the drain-to-source voltage V_{ds} is higher than $V_{gs}-V_{th}$. Therefore, the transistor is in the saturation region. The transistor in the Class B amplifier is between the cut-off and the saturation region because of $V_{gs} = V_{th}$ and $V_{ds} > V_{gs} - V_{th}$. Due to $V_{gs} < V_{th}$, the transistor of the Class C amplifier is in the cut-off region.

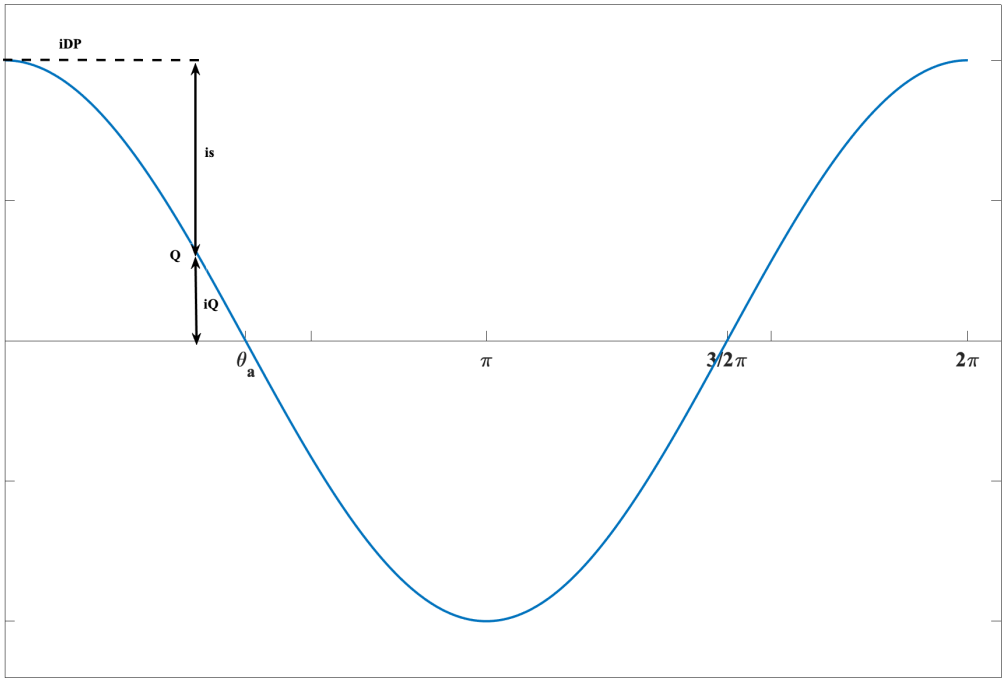

Figure 2.5: The waveform of the drain current i_D is in the time domain.

The drain current at the biasing point can be presented by a function of the conduction angle θ_c, as the following:

$$i_D(\theta_c) = i_Q + i_s \cos(\theta_c), (-\theta_a < \theta_c < \theta_a) \ . \tag{2.1}$$

As shown in Figure 2.5, i_{DP} is zero when $\theta_c = \theta_a$; thus,

$$\cos(\theta_a) = -\frac{i_Q}{i_s} \ , \tag{2.2}$$

and

$$i_s = i_{DP} - i_Q \ , \tag{2.3}$$

where i_{DP} is the maximum drain current and i_Q is biasing DC current. There-

fore, the drain current i_D can be represented by

$$i_D(\theta_c) = \frac{i_{DP}}{1-\cos(\theta_a)}[\cos(\theta_c) - \cos(\theta_a)] \ . \tag{2.4}$$

The DC current during the conduction period $[-\theta_a,\ \theta_a]$ is

$$I_{DC} = \frac{1}{2\pi}\int_{-\theta_a}^{\theta_a} i_D(\theta_c)d(\theta) \ . \tag{2.5}$$

Substituting into Eq.(2.4),

$$I_{DC} = \frac{i_{DP}}{2\pi}\cdot\frac{2\sin(\theta_a) - 2\theta_a\cdot\cos(\theta_a)}{1-\cos(\theta_a)} \ . \tag{2.6}$$

The fundamental component of the drain current is

$$I_1 = \frac{1}{\pi}\int_{-\theta_a}^{\theta_a} i_D(\theta_c)\cdot\cos(\theta_c)d(\theta) = \frac{i_{DP}}{2\pi}\cdot\frac{2\theta_a - \sin(2\theta_a)}{1-\cos(\theta_a)} \ . \tag{2.7}$$

The input power is

$$P_{in} = V_{dd}\cdot I_{DC} = \frac{V_{dd}}{2}\cdot\frac{i_{DP}}{2\pi}\cdot\frac{2\sin(\theta_a) - 2\theta_a\cdot\cos(\theta_a)}{1-\cos(\theta_a)} \ . \tag{2.8}$$

The output power is

$$P_o = V_{dd}\cdot I_1 = V_{dd}\cdot\frac{i_{DP}}{2\pi}\cdot\frac{2\theta_a - \sin(2\theta_a)}{1-\cos(\theta_a)} \ . \tag{2.9}$$

Therefore, the power efficiency is

$$\eta = \frac{P_o}{P_{in}} = \frac{2\theta_a - \sin 2\theta_a}{2\cdot[2\sin(\theta_a) - 2\theta_a\cdot\cos(\theta_a)]} \ . \tag{2.10}$$

Class A amplifier

The schematic of the Class A amplifier is shown in Figure 2.2. The operating point of a transistor for a Class A amplifier is not in the cut-off region because of $V_{gs} > V_{th}$ and $V_{ds} > V_{gs} - V_{th}$. Thence, the transistor M1 conducts

the whole duty cycle so that the conduction angle is $\theta_c = 2\pi$. From Eq.(2.10), the maximum efficiency is

$$\eta_{max} = \frac{2\pi - \sin 2\pi}{2 \cdot [2 \sin \pi - 2\pi \cdot \cos \pi]} = \frac{1}{2} . \tag{2.11}$$

Class A amplifiers have high linearity and low distortion but offer poor efficiency. As a result, high power losses are large, and heat problems are generated, which raises the temperature and damages the circuitry. Therefore, it is not the preferred choice.

Class B amplifier

Figure 2.3 demonstrates the operation diagram for Class B power amplifiers. As shown in Figure 2.4, $V_{gs} = V_{th}$, the operating point of the transistor is at the boundary between the cut-off region and saturation region. The transistor M1 will conduct when $V_{gs} > V_{th}$, and it will be in the saturation region for $V_{ds} > V_{gs} - V_{th}$. Therefore, the transistor conducts half a cycle for the Class B amplifier [7]. The drain current i_D is a half-wave, and the conduction angle of the Class B amplifier is π. Using $\theta_c = \pi$, the maximum efficiency of the Class B amplifier becomes

$$\eta_{max} = \frac{\pi - \sin \pi}{2 \cdot [2 \sin \frac{\pi}{2} - \pi \cdot \cos \frac{\pi}{2}]} = \frac{\pi}{4} . \tag{2.12}$$

Hence, the maximum efficiency of the Class B amplifier is higher than Class A.

Class C amplifier

The operating point of the transistor for the Class C amplifier is in the cut-off region because of $V_{gs} < V_{th}$. The Class C amplifier has a conduction

angle range from 0 to π so that the drain efficiency can increase from 50% to 100%. Since the reduction conduction angle, the Class C amplifier has a higher efficiency than Class B and Class A amplifiers. However, the transistor conducts less than half a cycle, and the conduction angle is small, which means the most input signals are missing in output signals. This case causes distortions between input signals and output signals, so the Class C amplifier is non-linear.

2.2.2 Switch-mode Power Amplifiers

Switch-mode amplifiers are classified by operating principle. They are commonly used in many applications because of their high-efficiency and simple circuitry. The efficiency of switch-mode amplifiers is high since the transistor nonzero voltage and current do not overlap. If the voltage is high, the current is zero and vice versa. Therefore, the maximum efficiency is 100% in theory [7]. In practice, the high efficiency of a switch-mode amplifier is above 90%, and the efficiency reduces by the conduction and switching loss of the transistor.

Class D amplifier

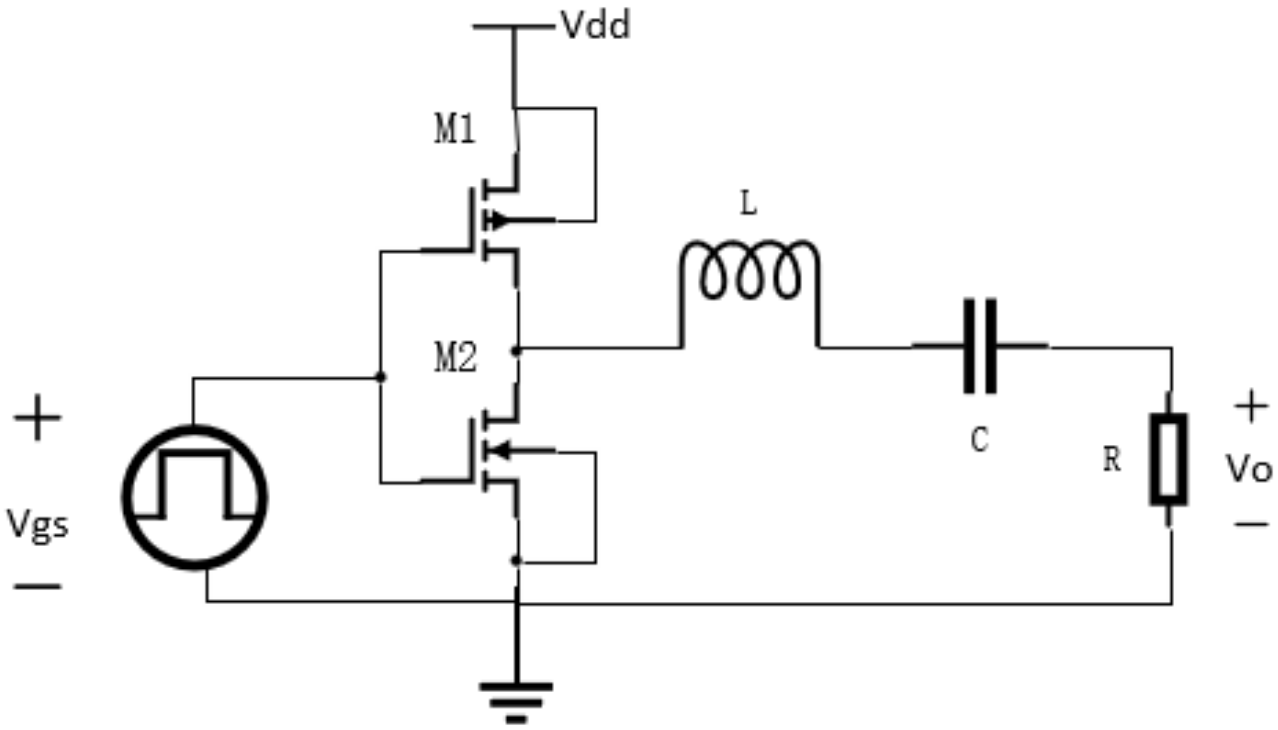

Figure 2.6: A schematic of the Class D amplifier [7].

The schematic of the Class D half-bridge amplifier is shown in Figure 2.6. Two transistors act as two switches, and the series resonant circuit is connected to the output of two switches. The series resonant circuit charges and discharges are based on turning the two switches ON and OFF. The L-C matching network eliminates harmonics caused by the square waveforms from the output of the two switches. Furthermore, the matching network is used to match impedance and reduce noise. If the loaded quality factor Q of the series resonant circuit is high enough, the current is sinusoidal. Pulse width modulation (PWM) is a typical method to drive the Class D amplifier.

The input signals are converted to continuous square pulses by this modulation technique. The carrier frequency should be at least ten times the input modulating frequency for correct amplification [17].

Generally, the operating frequency of the Class D amplifier should be above the resonant frequency of the matching network. If the operating frequency is less than the resonant frequency, the resonant circuit represents a capacitive load. The high current spike caused by the capacitive load current can damage the MOSFET device during the on-off transition. Several methods avoid capacitive behaviours, such as snubber circuits, an inductor, or high on-resistance transistors [7].

The Class D amplifier is commonly used to drive an ultrasound transducer because of low voltage stress, high efficiency, and simple topology characteristics. More details of the Class D amplifier analysis are presented in Chapter 3.

Class E amplifier

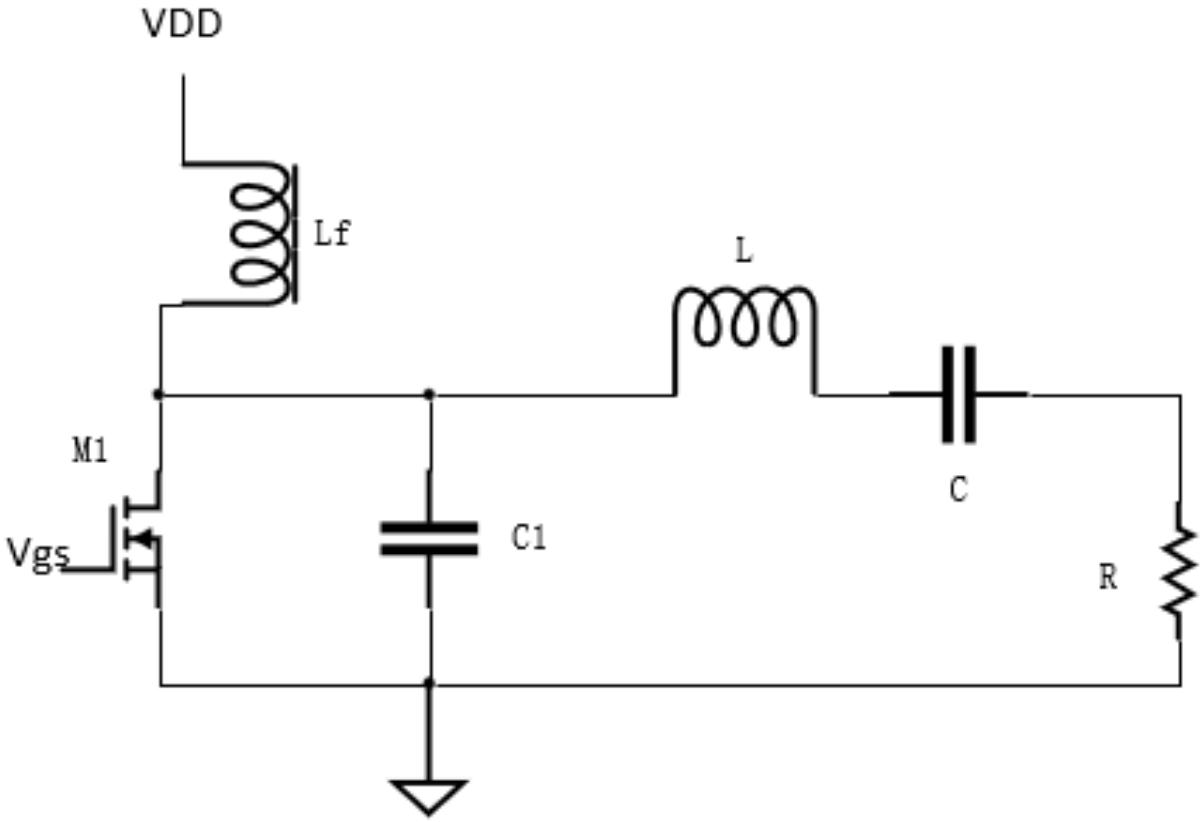

Figure 2.7: A schematic of the Class E amplifier [8].

The circuit configuration of the Class E amplifier is shown in Figure 2.7. The Class E amplifier consists of a choke inductor L_f, one transistor M1, a shunt capacitor C1, and an L-C-R series resonant circuit. The transistor turns on at zero voltage and zero derivative voltage, so the turn-on switching loss is zero [8].

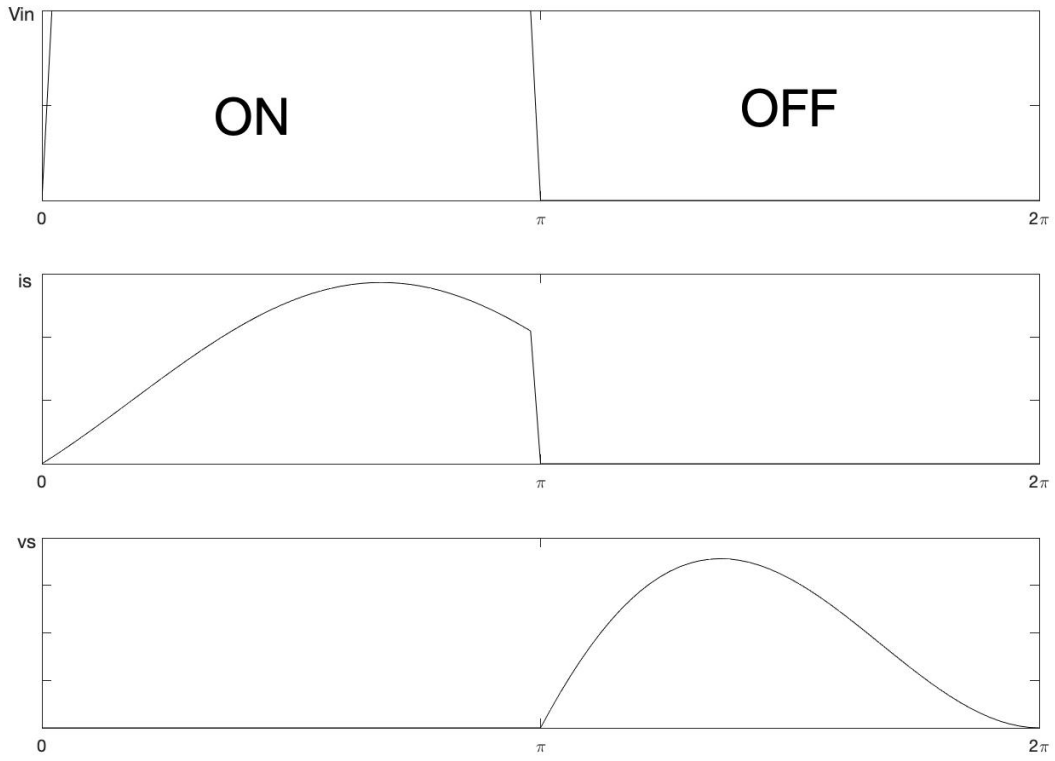

Figure 2.8: Waveforms of the gate singal, switch current and switch voltage [7].

Figure 2.8 demonstrates the waveforms of switch operations. The top figure shows the gate signal of the transistor, the medium figure illustrates the transistor current, and the bottom figure plots the voltage through the switch. As Figure 2.8 shows, the voltage and the current of the transistor are not overlapped, yielding the switching loss as low. The transistor turns ON at zero voltage and zero derivative voltage, so the Class E amplifier satisfies zero-voltage switching (ZVS) and zero-derivative switching (ZDS) operations. Combining waveform equations with ZVS and ZDS operations, find the relationship between the conduction angle and switch voltage and current, resulting in the amplitude of switch voltage V_{dsmax} is 3.562 times the supply

voltage, and the peak value of the switch current I_{SM} is 2.862 times of the input current [7].

Class DE amplifier

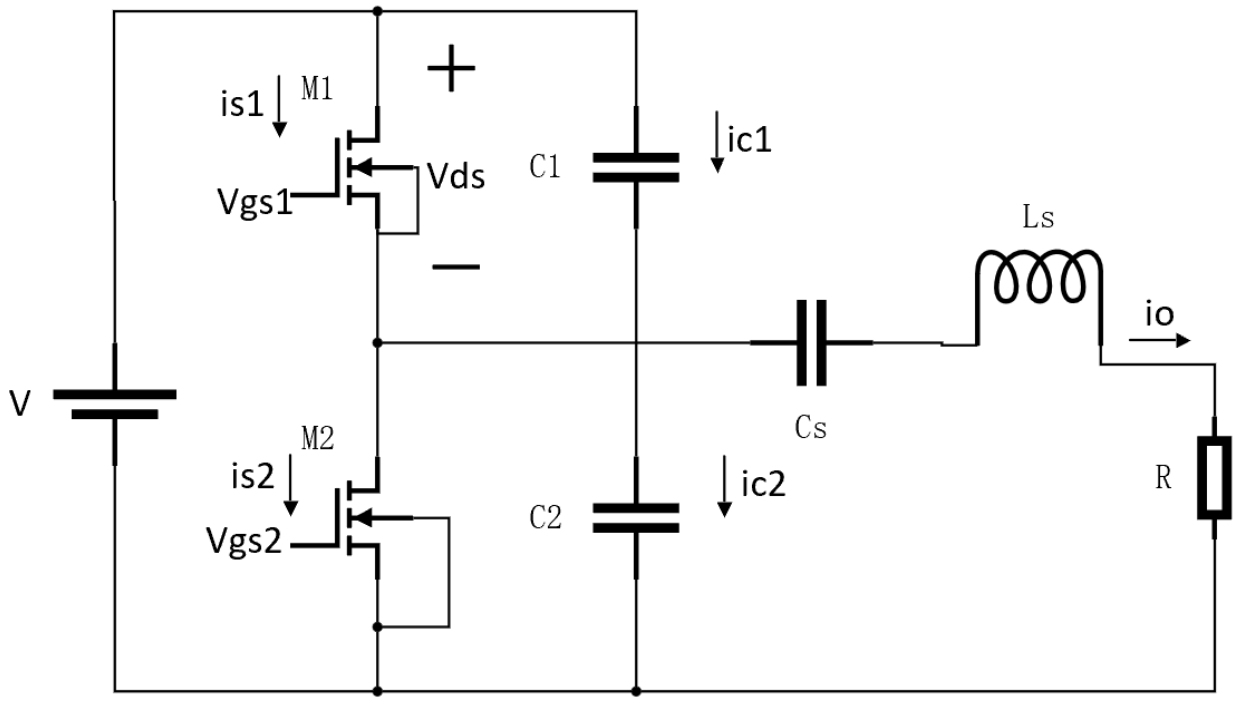

Figure 2.9: A schematic of the Class DE amplifier [7].

The circuit of the Class DE amplifier consists of two transistors, a series resonant circuit, and shunt capacitors. Its schematic is shown in Figure 2.8. The Class DE amplifier combines the properties of Class D with Class E operations to reach high efficiency. The M1 and M2 are alternatively ON and OFF, and the typical duty cycle D of the Class DE amplifier is 0.25.

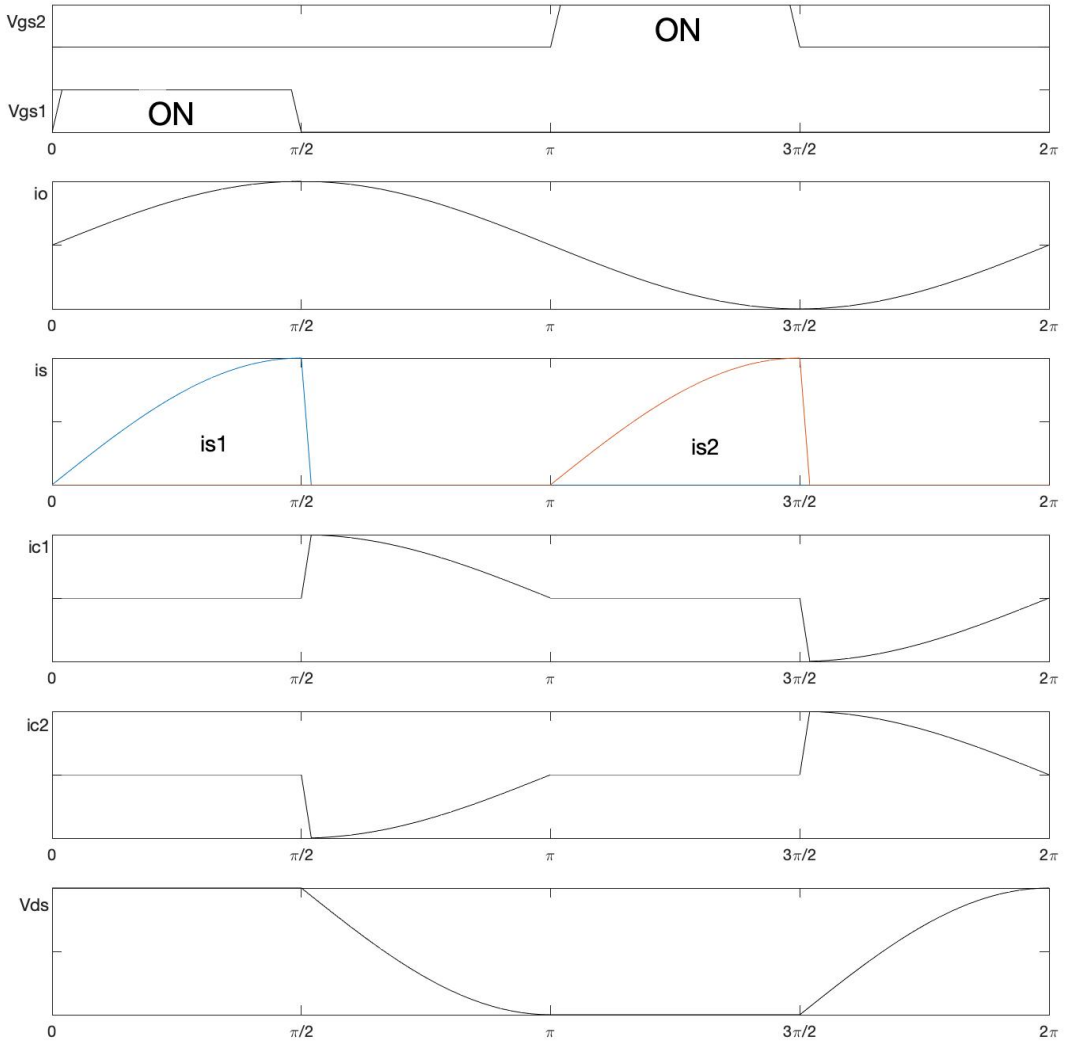

Figure 2.10: Waveforms of gate signals, switch currents, parallel capacitor currents and switch voltages [7].

Figure 2.10 illustrates the operations of the Class DE amplifier. From 0 to $\frac{\pi}{2}$, M1 is ON, and M2 is OFF. The drain-to-source voltage V_{ds1} of the transistor M1 is 0 V in this interval, and the voltage V_{ds2} of the transistor M2 is equal to the supply voltage V_{DD}. During this time interval, the current of

the series branch i_o is rising, and the current of parallel capacitors i_{c1} is zero since $V_{ds} = 0$.

From $\frac{\pi}{2}$ to π, both M1 and M2 are OFF. Two currents of two transistors i_{s1} and i_{s2} are 0 during this interval. The parallel capacitor C1 will provide the current for the series resonant circuit, and i_{C1} reduces from the peak value to zero. The output voltage decreases to the minimum ($V_{ds2} = 0V$), and the derivative of the output voltage is zero at t=π. As a result, ZVS and ZDS conditions are met.

From π to $\frac{3\pi}{2}$, M1 is still OFF, and M2 turns ON. The current i_{s2} flows to the switch M2 in the opposite direction of i_{s1} ($i_{s2} = -i_{s1}$). The voltage of the two switches at the output is 0V, with no voltage across M2. No current in the parallel capacitor C_p and the series resonance branch will discharge to M2.

From $\frac{3\pi}{2}$ to 2π, M1 and M2 are OFF. The operations will be the same as the last deadtime.

The disadvantage of the Class DE amplifier is that it is less flexible and that it is required to work at a fixed duty cycle and satisfy both ZVS and ZDS operations. Otherwise, the efficiency will decrease.

A summary of the different classes of amplifiers is shown in the following.

Table 2.1: A summary of the different classes of amplifier

Class	Mode	Maximum Efficiency	Characteristics
A	Current-mode	50%	Low distortion $\theta = 2\pi$ Linear
B	Current-mode	78.5%	Linear $\theta = \pi$ High efficiency
C	Current-mode	50-100%	Non-linear $\theta < \pi$
D	Switch-mode	100%	Low voltage stress
E	Switch-mode	100%	High voltage stress ZVS and ZDS conditions
DE	Switch-mode	100%	Low voltage stress ZVS and ZDS conditions

2.2.3 Other Topologies for Switch-mode Amplifiers

In this section, some variations of switch-mode amplifiers are described.

Step-up topology

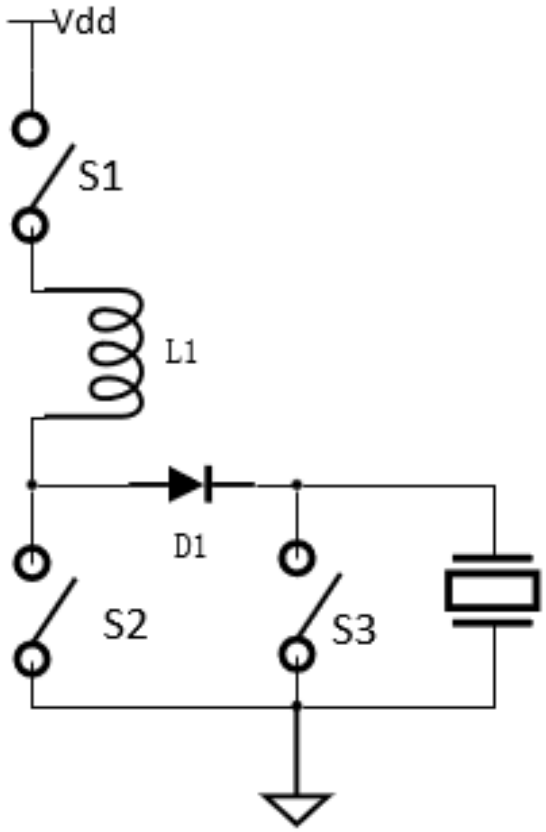

Figure 2.11: A schematic of the step-up driving topology [9].

The schematic of the step-up driving topology is shown in Figure 2.11. Firstly, switches S1 and S2 are ON, and the inductor L1 is charging. After this period, S2 is OFF, and the inductor charges the transducer. Lastly, S1 turns OFF, and S3 turns ON, and the transducer is discharged [9].

This topology has three switches, and the circuit that controls these switches gets complex. Additionally, the diode in this circuit will increase power consumption.

Flyback topology

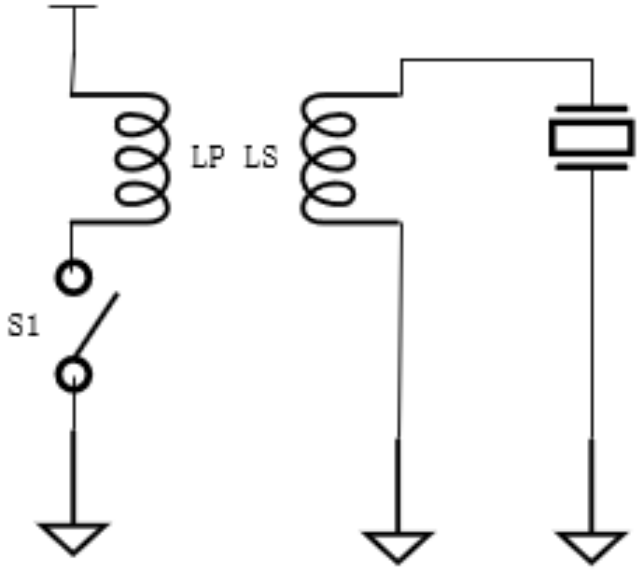

Figure 2.12: A schematic of the flyback topology [9].

Figure 2.12 illustrates the flyback topology that uses a transformer with a switch. The primary winding is connected to the supply voltage, and the secondary winding is connected to the transducer. This topology is simple, but the transducer and the secondary winding can create an oscillation loop [9].

Push-pull topology

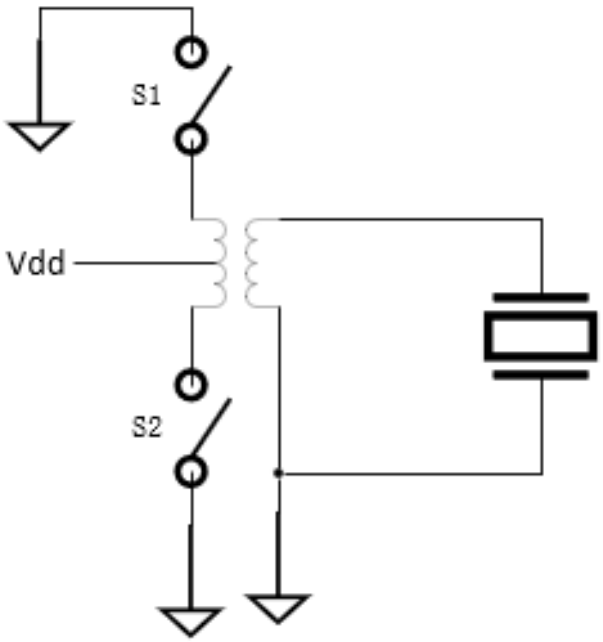

Figure 2.13: A schematic of the push-pull topology [9].

Figure 2.13 demonstrates a push-pull topology. Switches S1 and S2 are alternatively ON and OFF with a duty cycle of 0.5. The secondary winding is connected to the transducer directly. This transformer matches the power supply and transducer to enhance efficiency [9]. The major drawback is that the operating frequency is limited.

2.3 Ultrasound Transducer

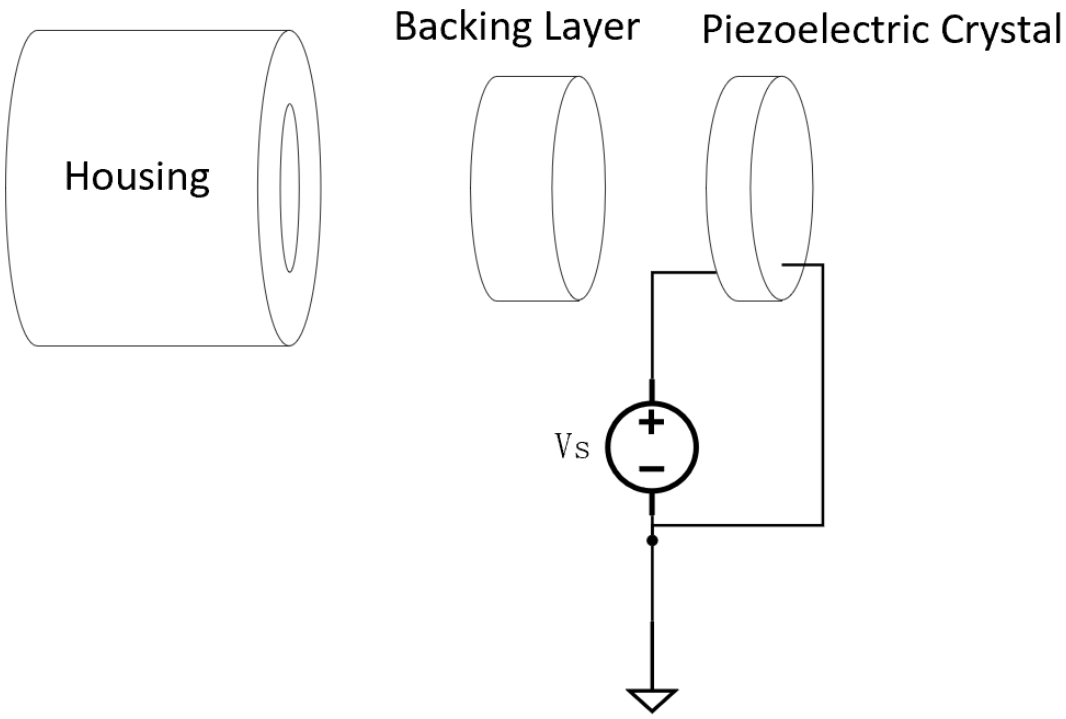

Figure 2.14: A exploded view of a transducer [6].

The ultrasonic transducer structure is composed of three parts: the housing, the backing layer, and the piezoelectric crystal called a piezoelectric resonator, as shown in Figure 2.14 [6]. The rightmost component produces ultrasound. Electrodes are connected to both sides of the resonator by coax cable in order to transmit signals. The housing is the outer case, protecting the piezoelectric resonator and providing air backing for the internal connection.

2.3.1 Electrical Model of the Piezoelectric resonator

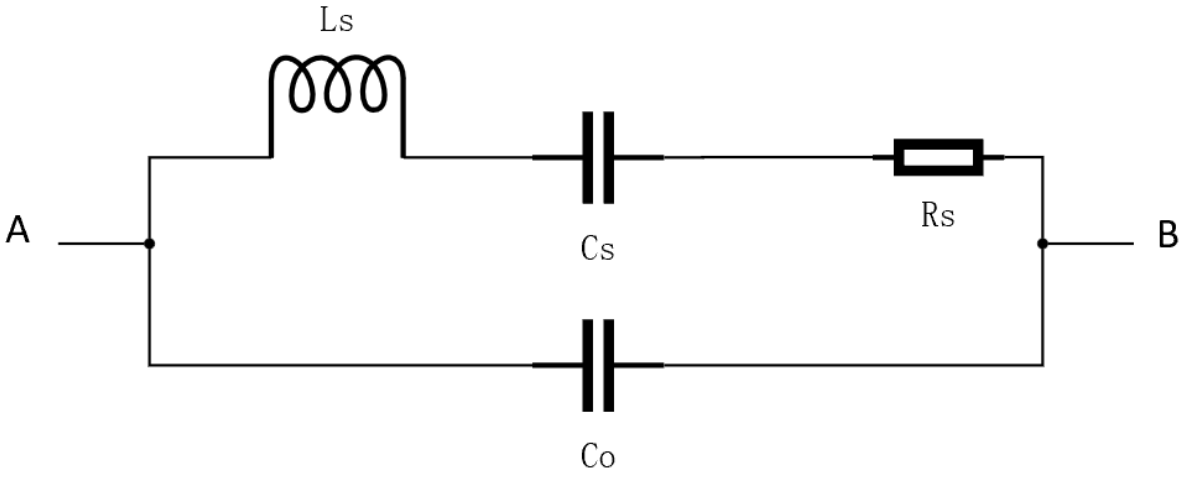

Figure 2.15: An equivalent circuit of the piezoelectric resonator [6].

The electric model of the piezoelectric resonator is represented by a Butterworth Van Dyke circuit, and the equivalent circuit is depicted in Figure 2.15. It consists of a capacitor C_o and a series branch. The impedance of the BVD circuit can be written as

$$Z = \frac{\frac{1}{j\omega C_o}(\frac{1}{j\omega C_s} + R_s + j\omega L_s)}{\frac{1}{j\omega C_o} + \frac{1}{j\omega C_s} + R_s + j\omega L_s}, \tag{2.13}$$

where ω is the angular frequency, and j is $\sqrt{-1}$. The parallel capacitor C_o illustrates the static capacitor of the resonator, which is determined by the physical characteristics. The series branch comprises L_s, C_s, and R_s components, which determined the mechanical oscillating characteristics of the resonator, such as the mechanical losses, and the mechanical power transferred to the acoustic field.

The components values of the equivalent circuit can be calculated using

the below equations [22] [23].

$$C_o = \frac{-I_m(Z_s)}{2\pi f_s |Z_s|^2} , \tag{2.14}$$

where f_s is the series frequency in which the real part of the admittance is minimum and f_p is the parallel frequency when the real part of the impedance is the maximum. The series branch components of the equivalent circuit can be obtained as the following:

$$L_s = \frac{1}{(2\pi f_s)^2 C_s} , \tag{2.15}$$

$$C_s = C_o[(\frac{f_p}{f_s})^2 - 1] , \tag{2.16}$$

and

$$R_s = \frac{|Z_s|^2}{R_e(Z_s)} . \tag{2.17}$$

2.4 Review of Previous Works

The section reviews typical published applications of different amplifiers, such as Class AB, Class B and Class D amplifiers, which are reviewed orderly, starting from current-mode to switch-mode amplifiers.

2.4.1 Class B and Class AB Amplifiers

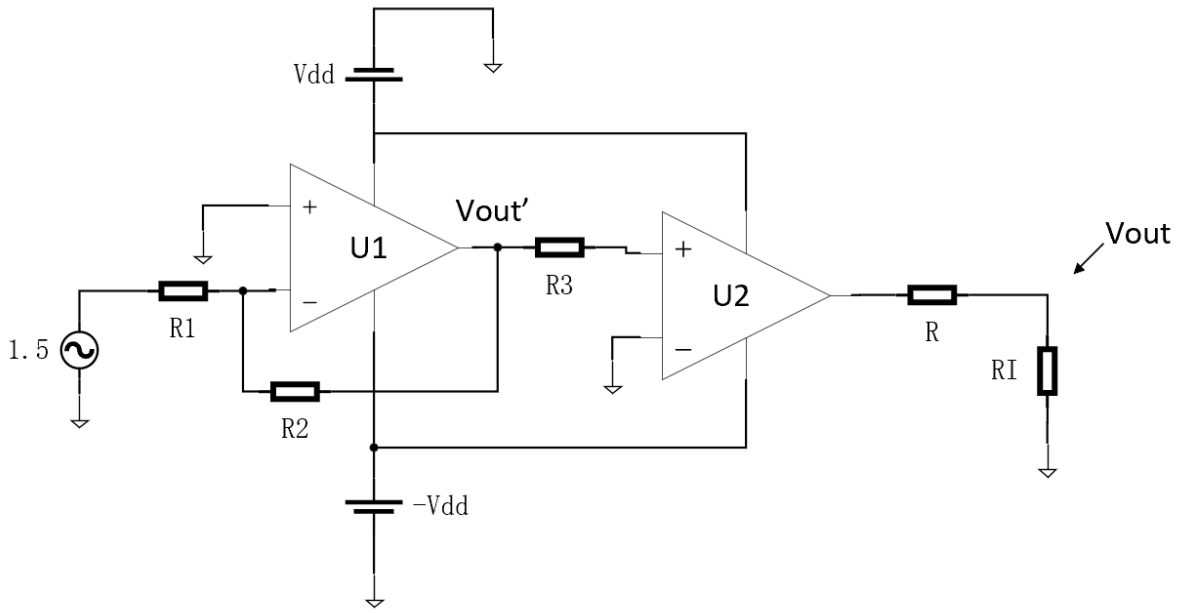

Figure 2.16: The schematic of the Class AB amplifier designed by Capineri [10].

Capineri proposed a linear Class AB amplifier used to drive low impedance ultrasonic transducers with low distortion [10]. Figure 2.16 illustrates the schematic of the amplifier module. The amplifier can provide a ± 60V output swing with a bandwidth up to 15MHz and an output current of 5A. It also offers around 60W of output power with less than 8% of the total harmonic distortion. However, it suffers from low efficiency(56%) at 1MHz. Therefore, the Class AB amplifier is not suitable for this thesis.

Ghisu *et al.* developed an integrated high voltage linear Class AB amplifier with the current feedback to generate wide closed-loop bandwidth output

signals. This Class AB amplifier can drive a load of 50 pF in parallel with 100 Ω with an output voltage of 180 V_{pp} at a frequency of up to 20MHz [11]. However, efficiency is not mentioned. In theory, the maximum efficiency of the Class AB amplifier is 78.5%.

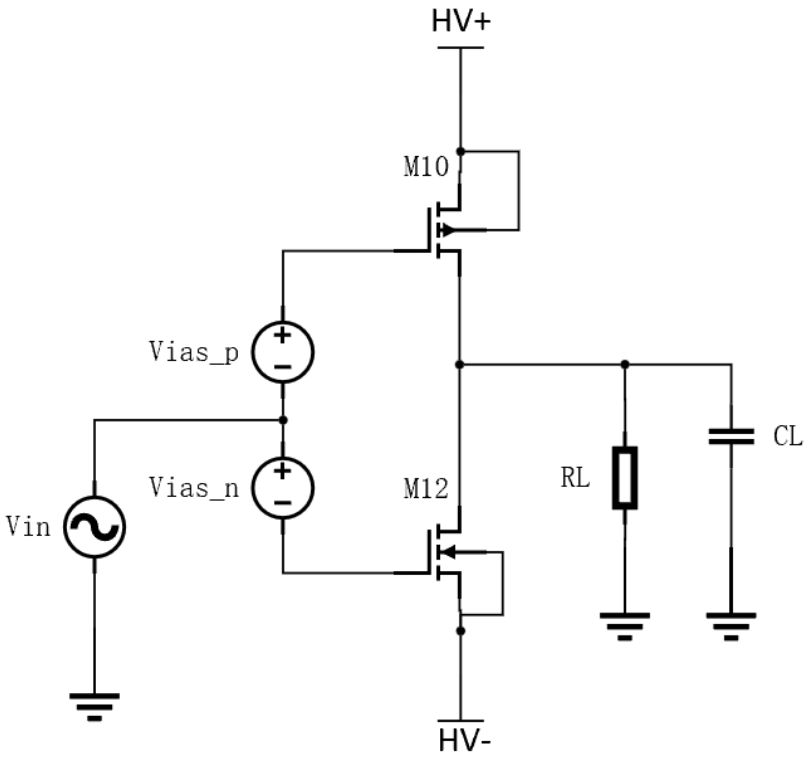

Figure 2.17: A schematic of the Class B amplifier [12].

Bianchi *et al.* designed a Class B amplifier for ultrasound transducers, which could operate at 6.5MHz bandwidth at the output swing of 90 V_{pp}, the output power of 20W and the efficiency above 60% [12]. Figure 2.17 shows the simplified circuit of the Class B module. The efficiency of this design is higher than the previous Class AB amplifier application [10]; however, the

efficiency decreases as the frequency increases. Thus, the Class B amplifier does not meet the objectives of this thesis.

2.4.2 Class D Amplifiers

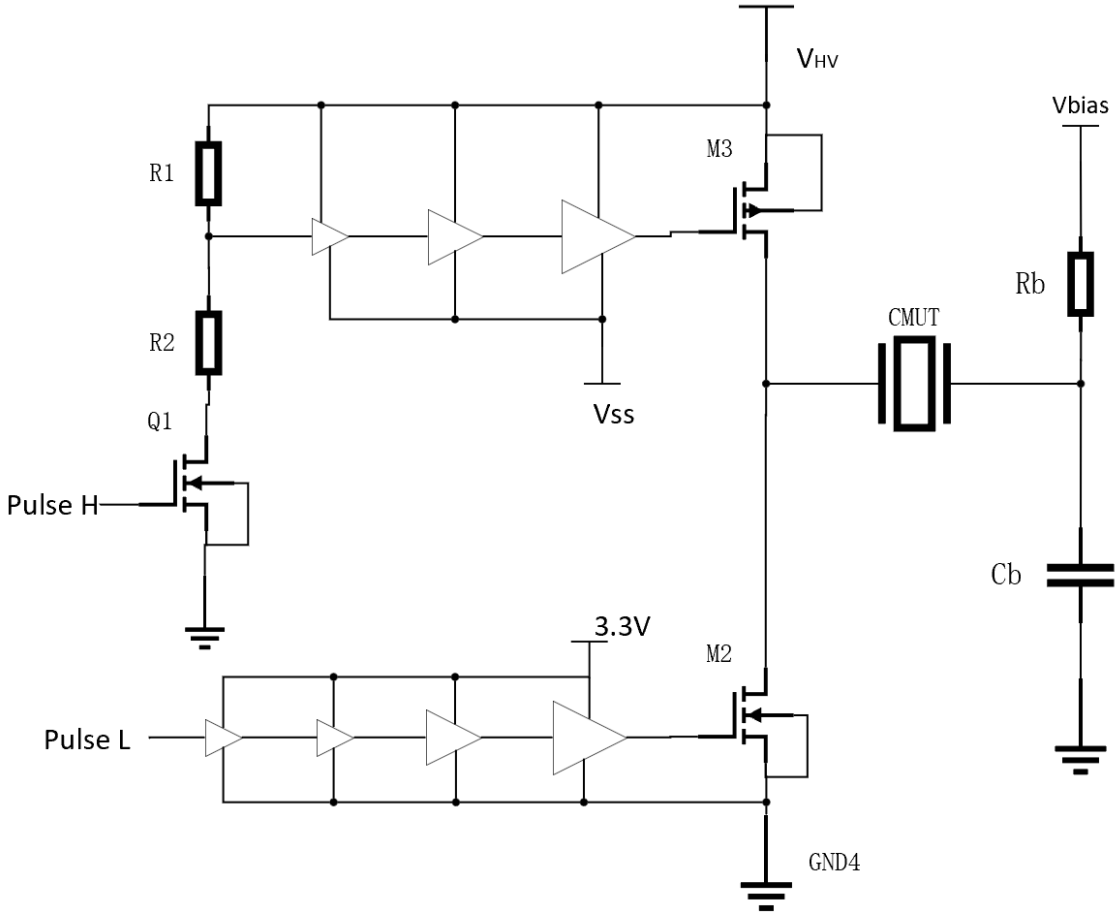

Figure 2.18: A schematic of the Class D amplifier [13].

Farhanieh *et al.* proposed a portable HIFU driving system for a Capacitive Micromachined Ultrasonic Transducers (CMUT). The amplifier provides 20 V_{pp} pulses and delivers an output power of 130mW to the transducer with a 130V DC bias, and the overall efficiency of this system is 23% [13]. Figure 2.18

shows the schematic of the designed high-voltage driver. The design uses a Class D amplifier to drive a high voltage ultrasound transducer without the filter. Since the CMUTs in the design are not connected to a matching network, the load keeps harmonics affecting the output power. Furthermore, the load impedance is capacitive. As previously discussed, the capacitive load can increase the switching losses to decrease efficiency.

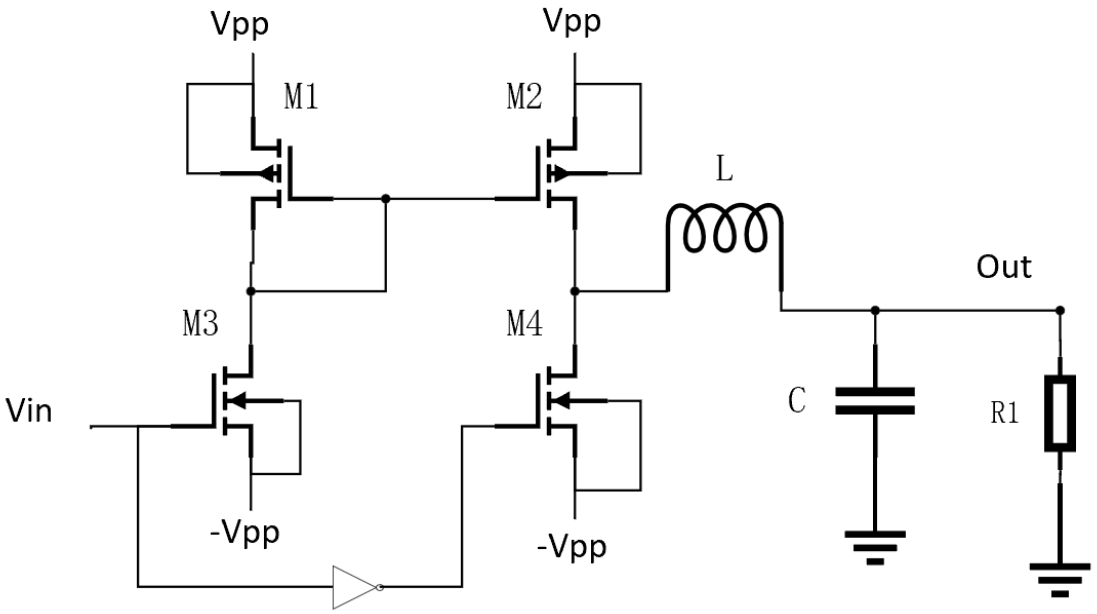

Figure 2.19: A schematic of Class D amplifier proposed by Ang et al. [14].

Ang *et al.* fabricated an integrated amplifier to produce the output power up to 800mW at 1.5MHz with an efficiency of 70% for low-intensity pulsed ultrasound (LIPUS) [14]. The schematic of this driving circuit is shown in Figure 2.19. The LIPUS driving system is comprised of a power supply, a pulse-modulated gate signal, PMOSs and NMOSs, an L-type tuning network

and a piezoelectric transducer. The author illustrated the overall efficiency is 14% for the average power consumption is approximated as 800mW. At 1.5MHz, the transducer efficiency is estimated at 20%. Therefore, the efficiency of this system is deduced to 70% ($\eta = \frac{14\%}{20\%} = 70\%$).

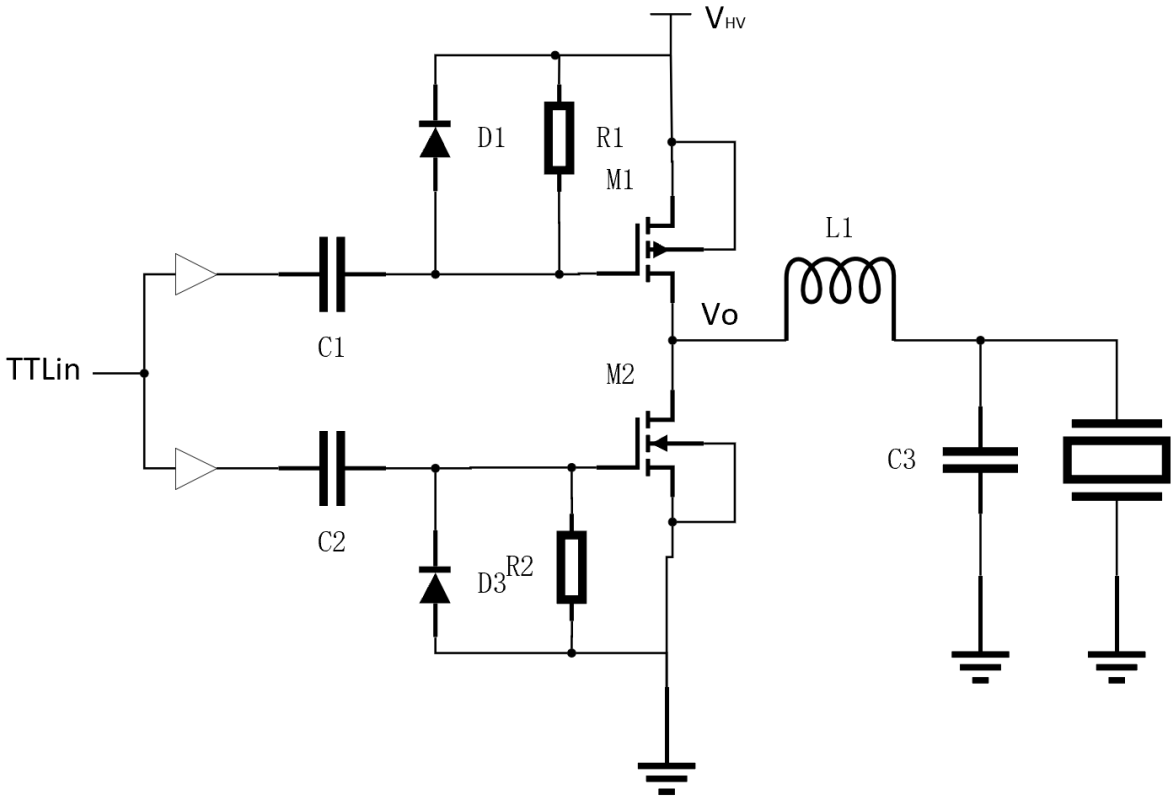

Figure 2.20: A schematic of the Class D amplifier with a filter [15].

Hall *et al.* designed a Class D amplifier to drive an ultrasound system, generating 20W output power per channel with 90% efficiency [15]. Figure 2.20 shows the schematic diagram of this design for one channel. TTL gate signals control a PMOS and an NMOS. The PMOS is connected to the high-side that needs a level shifter, consisting of capacitors C1 and C2 and resistors R1 and R2. The filter for each channel consists of an inductor and a shunt capacitor.

The filter is to eliminate harmonics at the output of the two transistors and reduce the variation between the component impedances. This article has not mentioned the details of the design method.

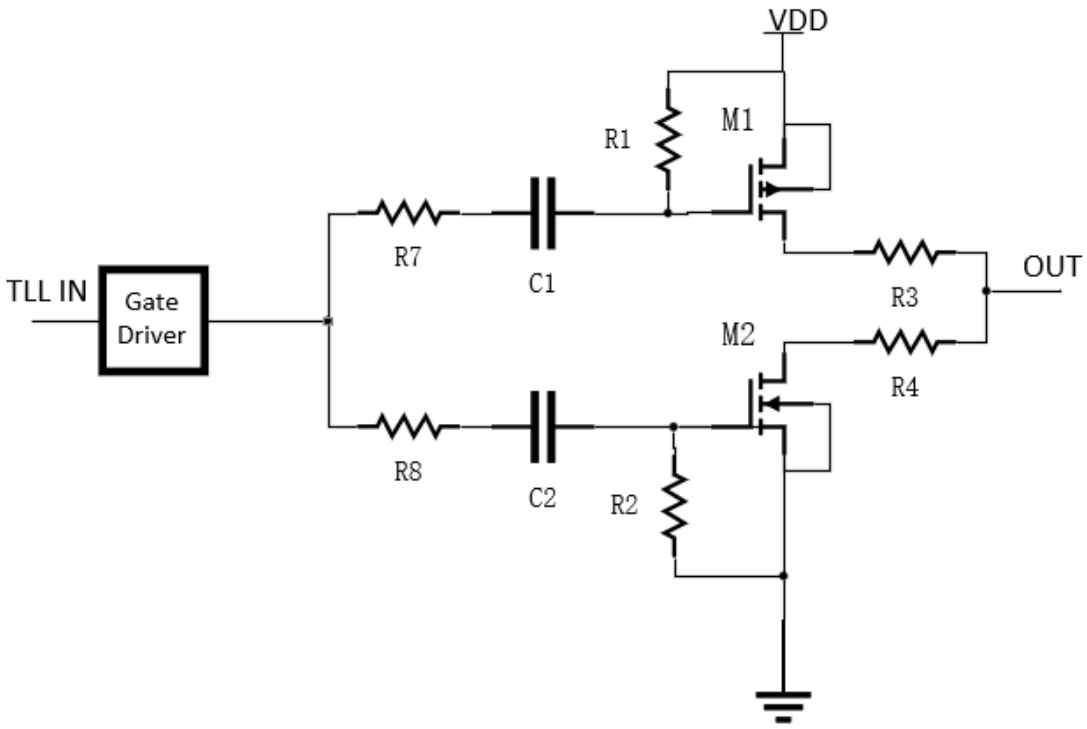

Figure 2.21: A schematic of the Class D amplifier without a matching network [16].

Lewis and Olbricht proposed a Class D amplifier providing 48W output power at 1.5MHz for a high-intensity ultrasound system [16], as shown in Figure 2.21. The authors said that the driver provides a switching voltage up to $100V_{pp}$ to the impedance that is less than 0.05Ω without an impedance tuning network. There is no matching network, and the output impedance is low, so the output power is increased. However, the output of the Class D amplifier is a square waveform. If the square wave from the output of the two switches is delivered to the ultrasound transducer, it will remain harmonics

reduced the output power. Therefore, the power efficiency decreases.

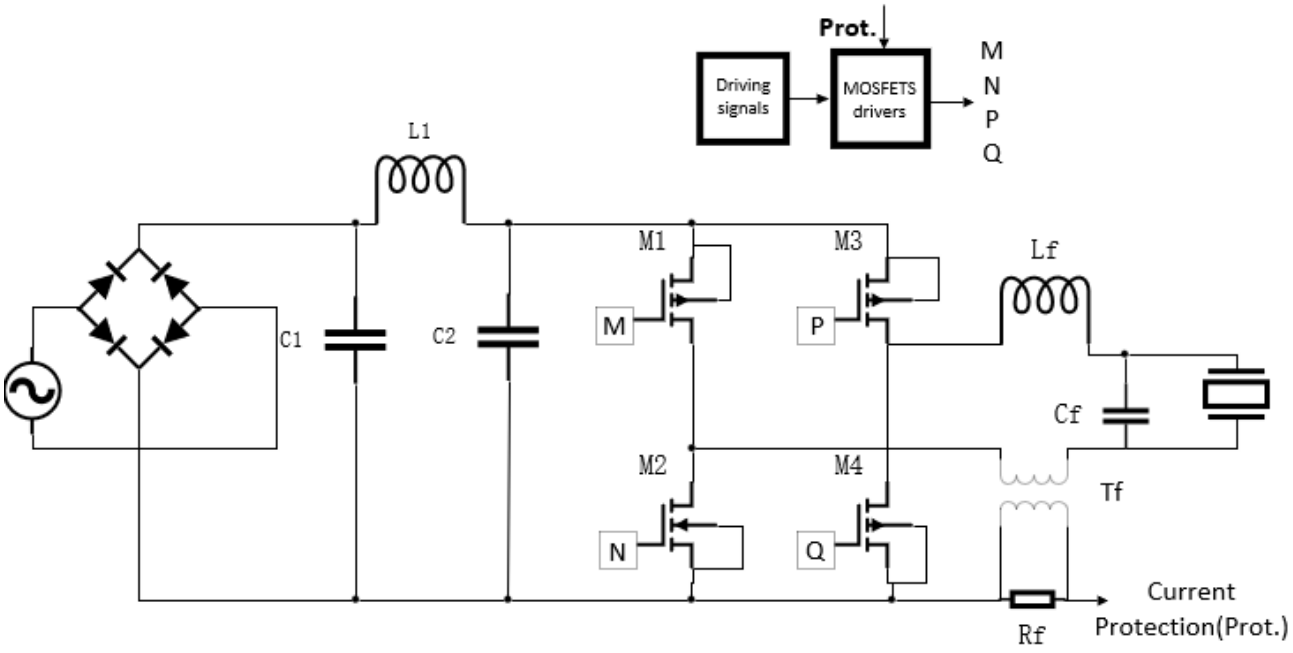

Figure 2.22: A diagram of the Class D amplifier designed by Agbossou et al. [17].

Agbossou *et al.* developed a full-bridge Class D amplifier to drive an acoustic cavitation reactor with an output power of 2kW, a high efficiency (>90%) in the operating in a range of 10kHz to 100kHz [17]. Figure 2.22 illustrates the diagram of the design. An RC snubber circuit and parallel diodes are used to protect the MOSFETs, and the pulses generated by the PWM technique are used to protect the MOSFETs. A low pass filter is used to avoid the capacitive load caused by temperature variations in the transducers. Moreover, the current spikes and overvoltage caused by the capacitive load can damage the circuit. The operating frequency of the capacitive load is at a frequency that is less than the resonant frequency. Therefore, the piezoelectric load should be resistive or inductive to operate well, and the operating frequency should

be near the series resonant frequency. The authors do not detail the low-pass filter design method, but he points out that the L-C filter is the second-order low-pass Butterworth filter for any frequency within its inductive frequency range.

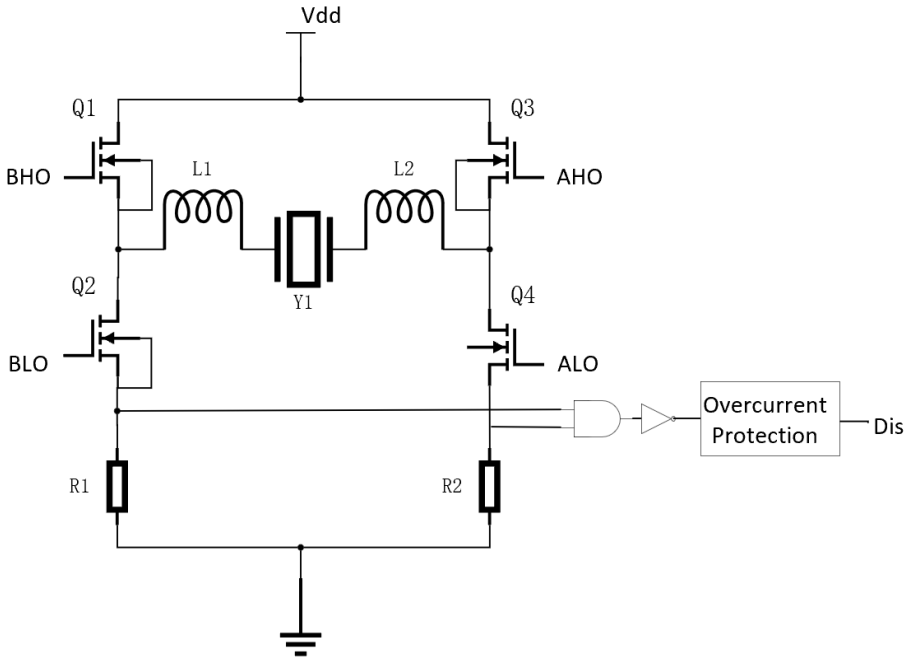

Figure 2.23: A diagram of the Class D Amplifier [18].

Yang and Xu designed a Class D amplifier for an Audio Beam system, operated between 20kHz and 60kHz [18]. Figure 2.23 shows the schematic of this design. The amplifier is composed of four transistors, two inductors, and two resistors. The two resistors, R1 and R2, are monitored by the overcurrent protection section to monitor the output. The feedback signal will be sent to the gate driving circuit to control the MOSFET. The pair of inductors L1 and L2 solves the problem caused by a capacitive load. This topology is suitable for audio frequency, but this low frequency is unsuitable for this thesis.

2.4.3 Class E Amplifiers

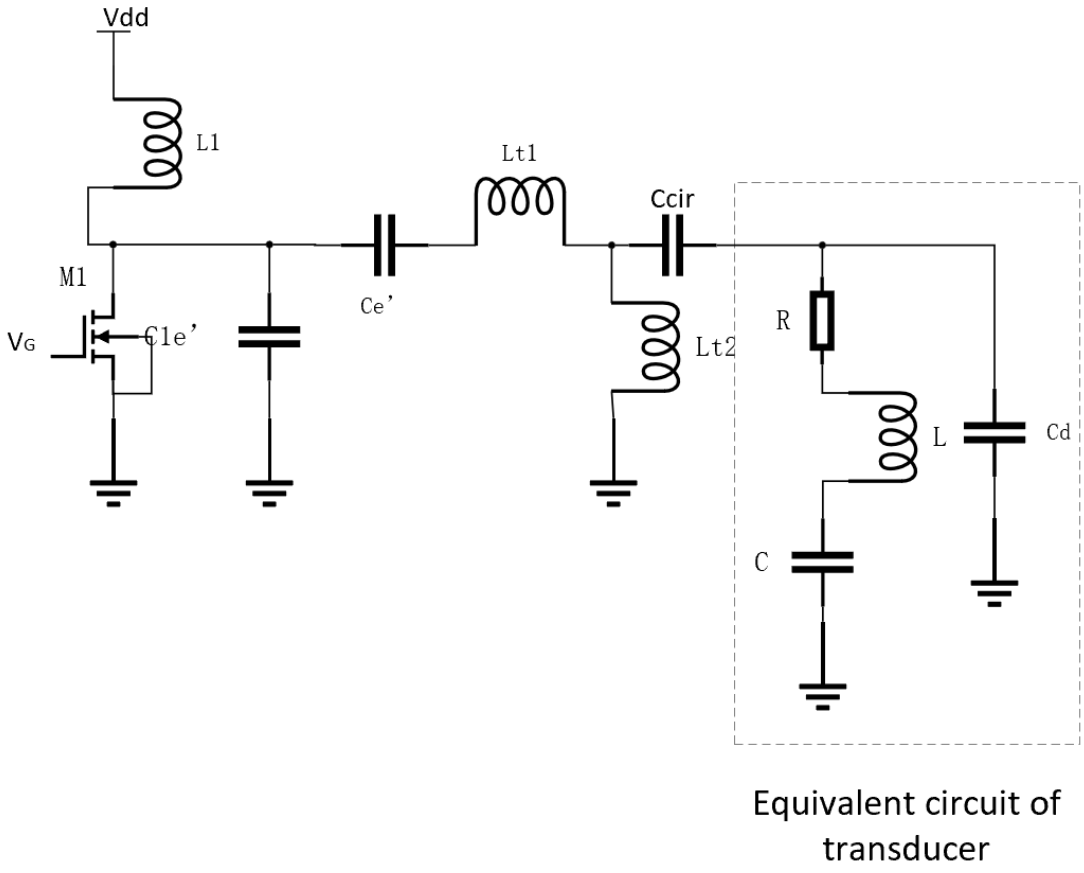

Figure 2.24: A schematic of the Class E amplifier [19].

Yuan *et al.* proposed a Class E amplifier to drive an inductive Langevin transducer at optimum frequencies [19]. Langevin transducers comprised of piezoelectric rings, front mass, back mass, acoustic horn and central bolt [20], are commonly used in ultrasonic machining and cleaning, underwater acoustics, ultrasonic motor and sonochemistry. Figure 2.24 illustrates the schematic of the Class E amplifier. The experimental results indicated that the driver had a good performance between the resonance and anti-resonance

frequency. Therefore, the proposed amplifier should operate in its inductive frequency range to get the maximum efficiency.

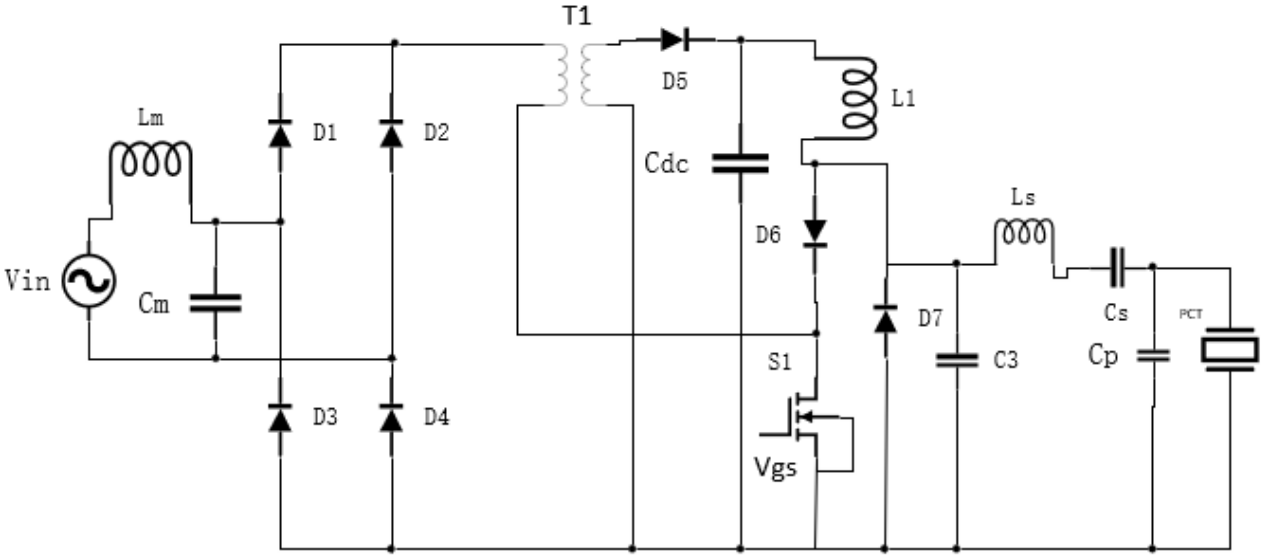

Figure 2.25: A diagram of the Class E amplifier [21].

Cheng *et al.* designed a Class E amplifier for driving a piezoelectric ceramic transducer that delivered the output power of 42W at 41kHz with an efficiency of 90% [21]. The circuit is composed of a flyback converter and a Class E resonant inverter, shown in Figure 2.25. The efficiency of the amplifier is high due to low switching loss. The Class E amplifier must operate in the suboptimum mode to achieve low-switching. The capacitor should be fully discharged before the switch is turned ON. Therefore, the power efficiency is high.

2.4.4 Class DE Amplifiers

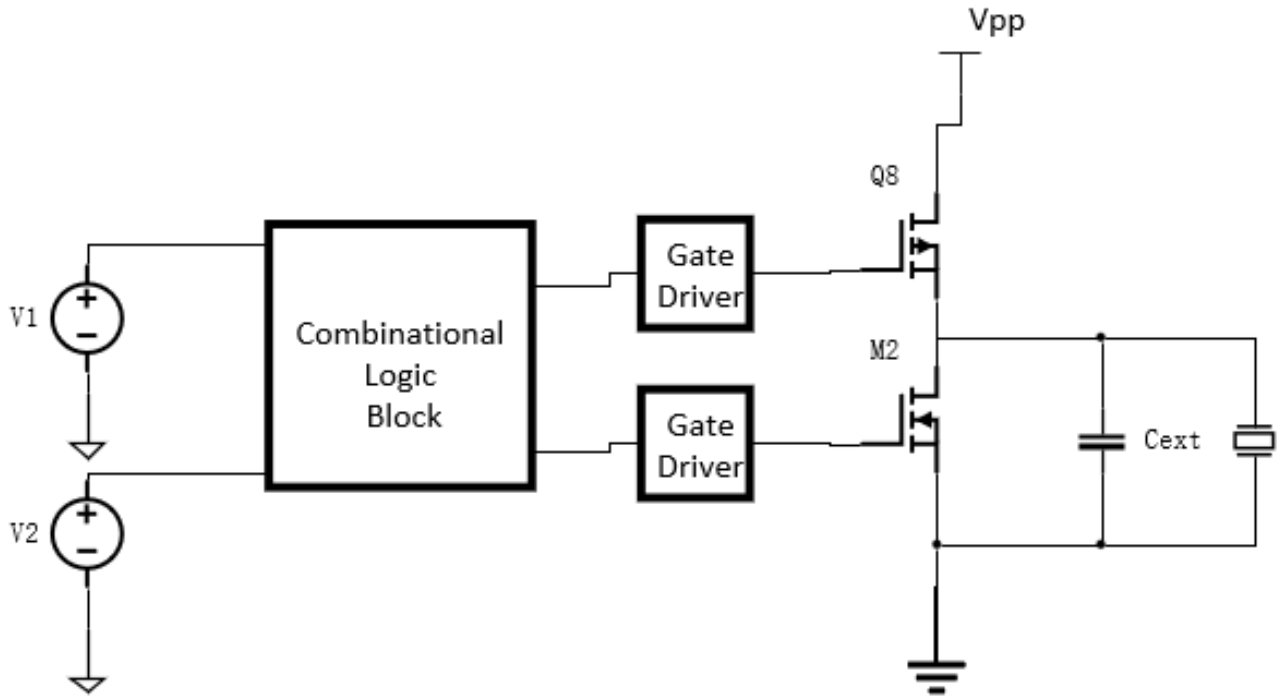

Figure 2.26: A schematic of the half-bridge Class DE Amplifier [22].

Wong proposed a Class DE amplifier without a matching network to drive ultrasonic transducers for HIFU therapy. The schematic of the class DE amplifier is illustrated in Figure 2.26. The Class DE amplifier achieved 830mW output power at 1010kHz with 90% efficiency [22]. The amplifier has to be in optimum conditions to perform an efficient operation. Compared to the Class D amplifier, the Class DE amplifier is less flexible. The Class DE amplifier has to operate for ZVS and ZDS operations that boost power efficiency.

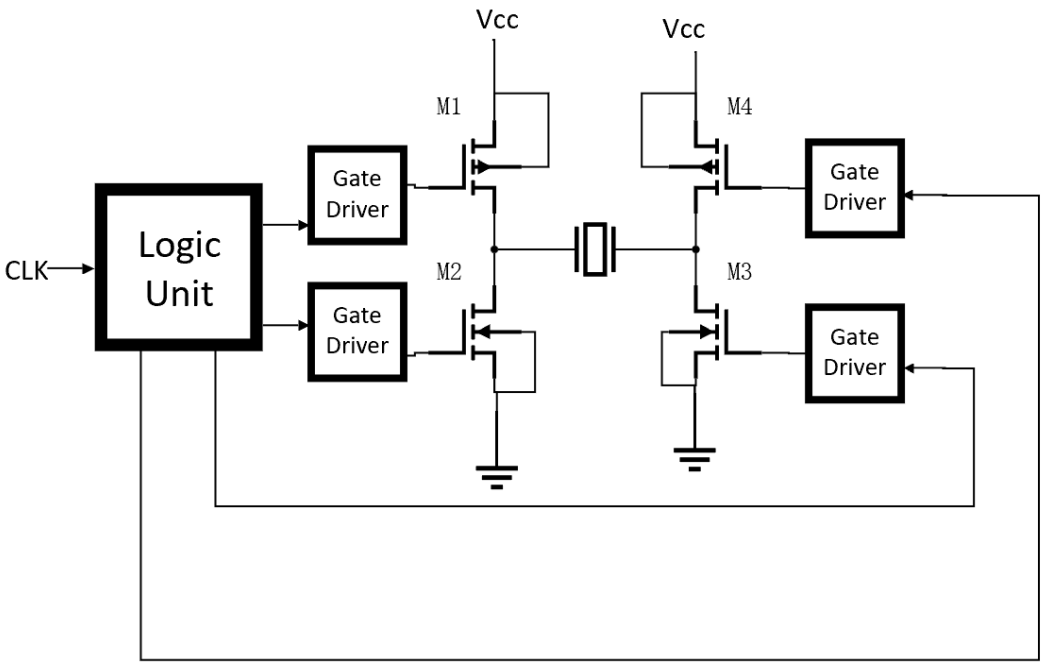

Figure 2.27: A schematic of the full-fridge Class DE amplifier [23].

Song used the same topology that Wong has used to improve a full-bridge Class DE to boost output power; the schematic is shown in Figure 2.27. This full-bridge amplifier employs four transistors fabricated in a 35μm CMOS process. This allows the power of the full-bridge amplifier to be four times greater than the half-bridge amplifier using the same supply voltage and to reach 3.6W of output power with 89.4% efficiency [23]. The Class DE amplifier is efficient to drive different transducers by adjusting the operating frequency and reprogramming the duty cycle without matching networks. However, if the Class DE amplifier is not optimum, high current spikes affect power efficiency.

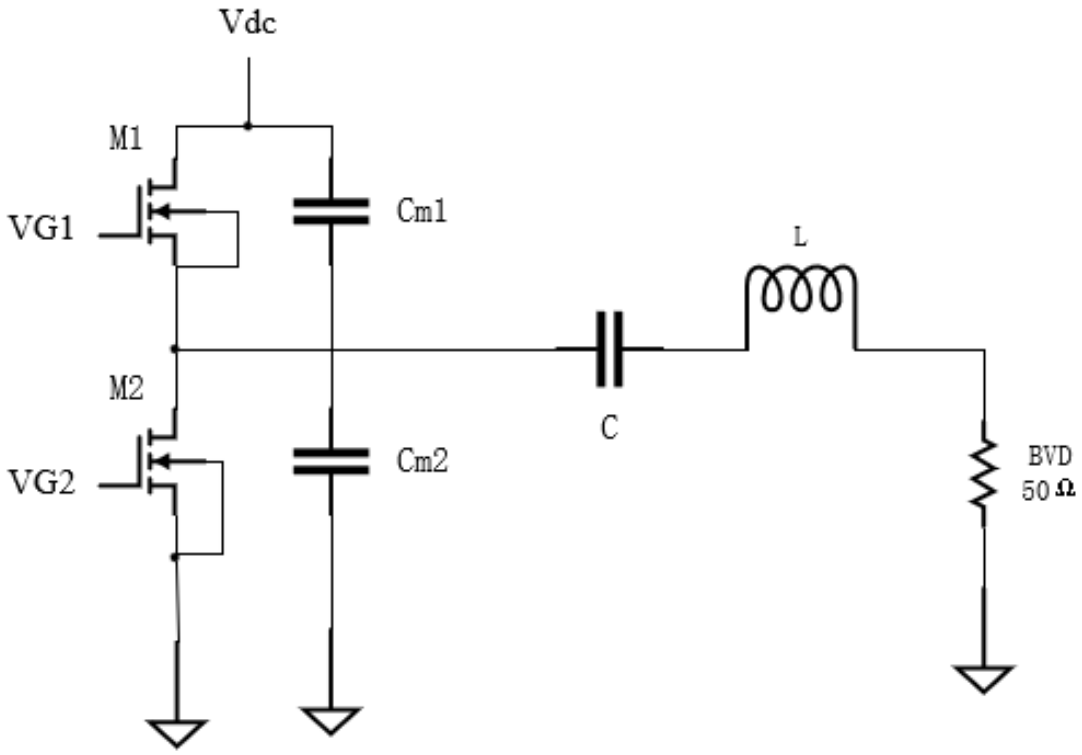

Figure 2.28: A schematic of the Class DE amplifier designed by Kivinen [4].

Kivinen designed a Class DE amplifier to drive the sonoporation device so that the amplifier can deliver 134W of output power with 90% of the overall efficiency at 1MHz [4]. Figure 2.28 shows the schematic of the Class DE amplifier. The circuit consists of two transistors, the parallel drain capacitors and the RLC circuit. The simulation shows that the voltage through the transistor is not zero in the beginning, causing a large spike in the drain current, which increases the switching losses. Moreover, the gate driver is not included in the design, and it should be implemented.

2.4.5 Summary of Amplifiers in the Literature

Table 2.2 summarizes all previous works in this chapter. The Class D amplifier will be used in this thesis because of its high operating frequency and high efficiency. The Class D amplifier is more flexible than the Class DE amplifier and the Class E amplifier.

Table 2.2: A summary of different classes of amplifiers for the literature reviews

Reference	Topology	Operating Frequency	Output Voltage	Output power	Efficiency	Comments
[4]	Class DE	1MHz	$200V_{pp}$	134W	89.5%	High efficiency Needs matching network Less flexibility
[10]	Class AB	10MHz	$60V_{pp}$	59.89W	56%	Low efficiency
[11]	Class AB	20MHz	$180V_{pp}$	266W	-	Low efficiency
[12]	Class B	6MHz	$90V_{pp}$	20W	$> 60\%$	Low efficiency Needs tuning network
[13]	Class D	10MHz	$20V_{pp}$	0.13W	23%	Low output power Low efficiency No matching network
[14]	Class D	1.5MHz	7.6V	0.8W	70%	Low output power Low efficiency Needs matching network
[15]	Class D	1MHz	-	20W	90%	High efficiency Needs matching network
[16]	Class D	1.5MHz	$100V_{pp}$	48W	90%	Low output impedance High efficiency No matching network
[17]	Class D	10kHz-100kHz	$200V_{pp}$	2000W	95%	High efficiency Needs matching network
[18]	Class D	20-60kHz	$120V_{pp}$	44W	91%	High efficiency Needs matching network
[21]	Class E	41kHz	$100V_{pp}$	42W	93%	High efficiency Needs high choke inductor
[22]	Class DE	1MHz	$20V_{pp}$	0.83W	90%	High efficiency No matching network
[23]	ClassDE	1MHz	$20V_{pp}$	3.6W	89%	High efficiency Programmable digital logic unit

Chapter 3

Proposed Power Amplifier

3.1 Introduction

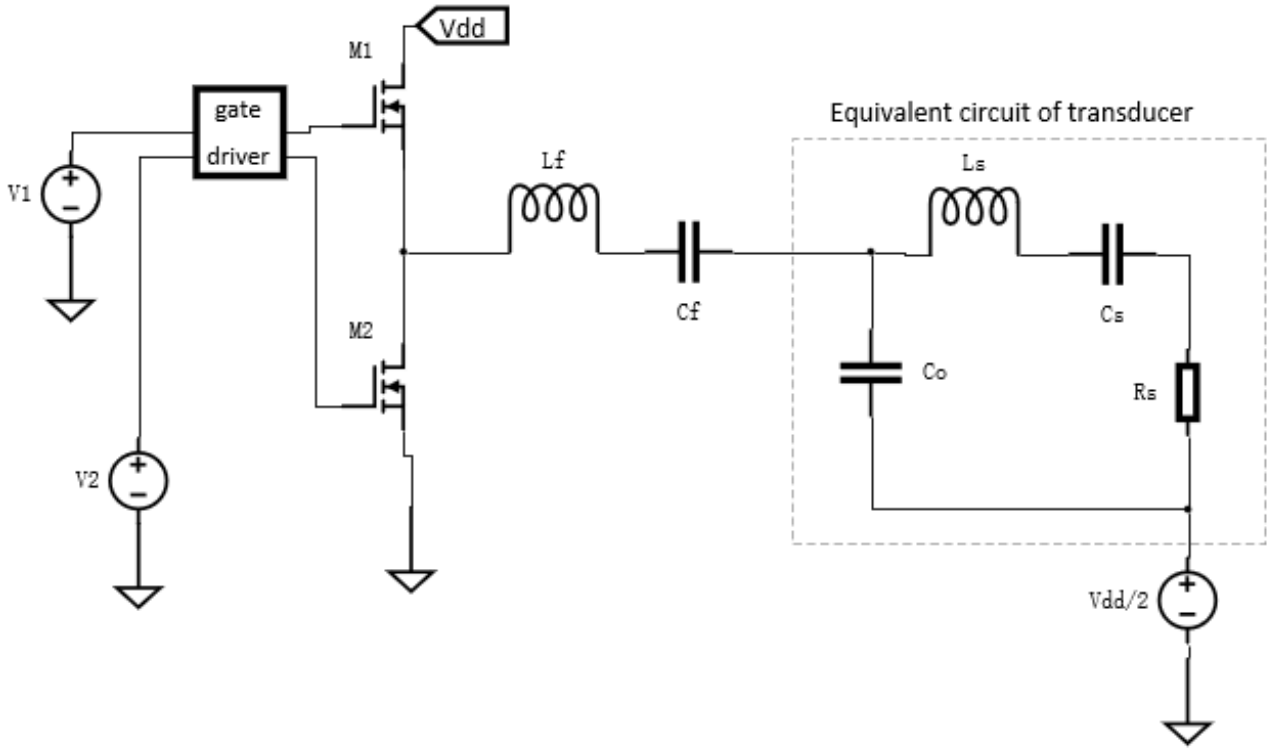

Figure 3.1: A block diagram of the design.

This chapter illustrates details of a new design methodology of a half-bridge ZVS Class D amplifier, including the L-C filter design method, and the corner analysis of matching network component variations. The block diagram of the design is depicted in Figure 3.1. This proposed amplifier is shown in Figure 3.2, which consists of a half-bridge gate driver, two NMOSs and an L-C filter.

3.2 Amplifier Analysis

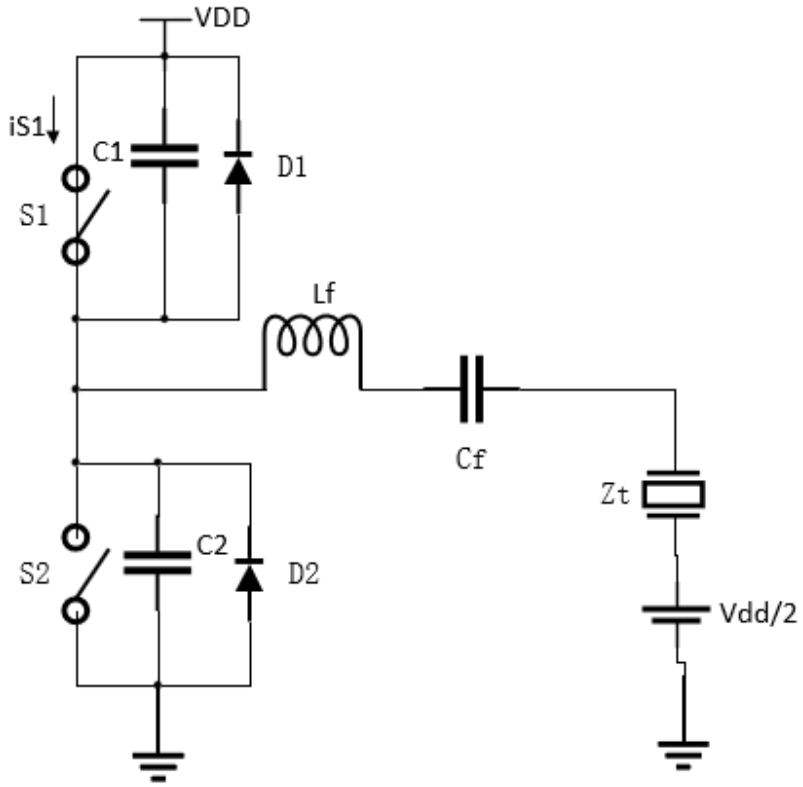

Figure 3.2: A simplified schematic of a Class D amplifier.

Figure 3.2 illustrates two NMOSs composed of two switches S1 and S2, with anti-parallel diodes D1 and D2. The filter is comprised of an inductor and a

capacitor connected in series. The analysis of this Class D power amplifier is based on the following assumptions:

1. Switches and parallel diodes are ideal, and the switches are assumed to be NMOS transistors. Initially, the drain capacitances of these switches are neglected.

2. The loaded quality factor (Q) is high enough to make the inductor current to be approximately sinusoidal.

3. The amplifier is designed and operated to produce the ideal waveforms shown in Figures 3.3 and 3.4.

3.2.1 Waveform Equations

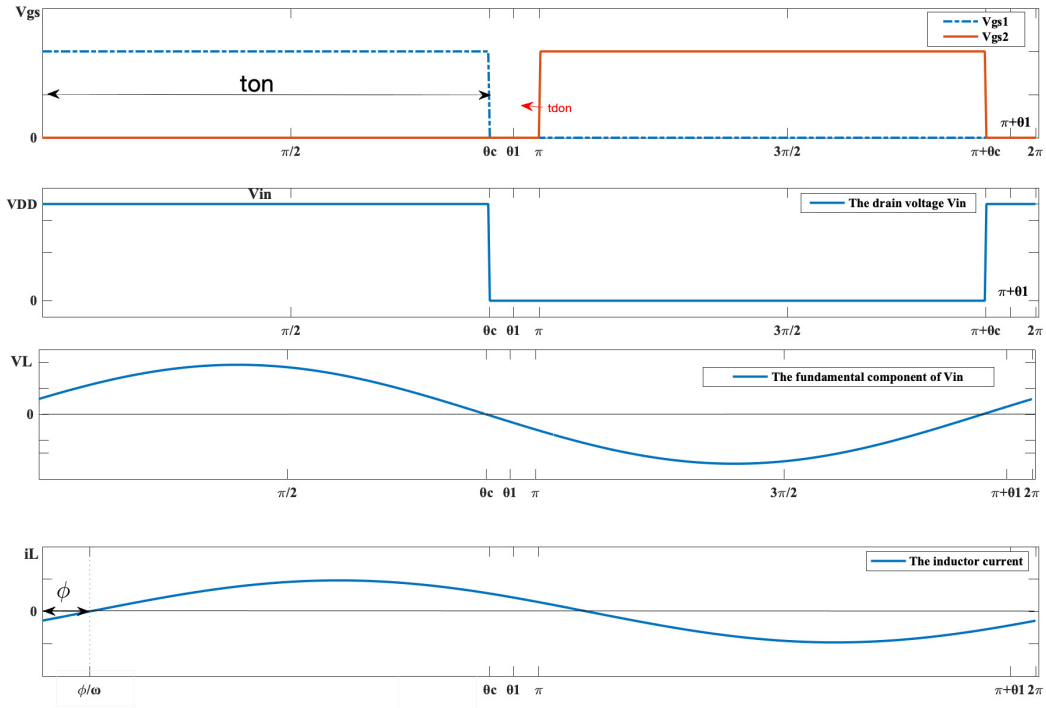

Figure 3.3: Waveforms of the gate voltage V_{gs}, the drain voltage V_{in}, the fundamental component V_1 of V_{in}, and the inductor current i_L.

Figure 3.3 shows the gate signals V_{gs}, the drain voltage V_{in}, the fundamental component of the drain voltage V_1, and the inductor current i_L waveforms. The current i_L lags behind the voltage V_1, resulting in the inductive load. The operation of the amplifier is described next.

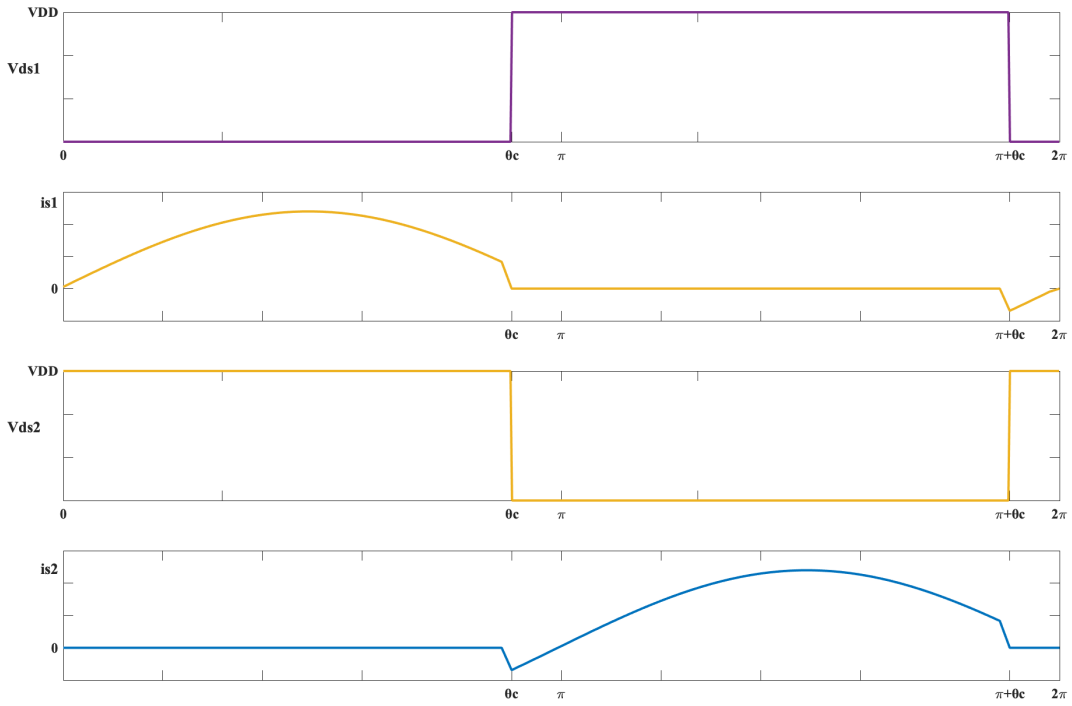

Figure 3.4: Waveforms of voltages V_{ds} and currents i_s of two switches.

The operation waveforms are shown in Figure 3.4. S1 and S2 turn ON alternatively and satisfy the ZVS condition. During the time interval [0, θ_c], switch S1 is ON, and switch S2 is OFF. The drain voltage V_{ds1} is zero. Current i_{s1} flows to S1, and no current through the drain capacitor. The series resonant circuit is charging. For $[\theta_c, \pi]$, both S1 and S2 are OFF, called dead time. During $[\theta_c, \theta_1]$, there is no current through any switches. The inductor discharges the drain capacitor. Voltage V_{ds2} across switch S2 reaches zero. During $[\theta_1, \pi]$, the diode D2 in parallel with S2 is ON. At $[\pi, \pi+\theta_c]$, the switch S2 turns ON, and S1 turns OFF. Voltage V_{ds1} remains V_{DD}, and S2 conducts at π. For $[\pi + \theta_c, \pi + \theta_1]$, this operation is identical to the first operation as the deadtime. Lastly, the anti-parallel diode D1 is ON at $[\pi + \theta_1, 2\pi]$.

Based on the above assumptions, the input voltage and current of the load and related components are written as the following equations. Note that all equations are derived according to the ideal waveforms and conditions.

The duty cycle D is the turn-on time over a period (T):

$$D = \frac{t_{on}}{T} \ , \tag{3.1}$$

where D is related to the conduction angle, as shown below:

$$\theta_c = \pi(1 - 2D) \ . \tag{3.2}$$

The drain voltage is a square wave, as expressed by

$$V_{in} = \begin{cases} V_{DD} \ for \ -\pi + \theta_c < \theta \leq \theta_c \\ \\ 0 \ for \ \theta_c < \theta \leq \pi + \theta_c \end{cases} \ . \tag{3.3}$$

The phasors corresponding to the fundamental component of the drain voltage and inductor current of the load are given by

$$V_L = \frac{2}{\pi} V_{DD} \exp j(-\frac{\pi}{2} + \theta) \tag{3.4}$$

$$I_L = I_p \exp j(-\frac{\pi}{2} - \phi) \ , \tag{3.5}$$

where I_p is the peak value of the inductor current and j is the imaginary unit. ϕ is the displacement angle between the drain voltage and the inductor current, and ϕ must be positive for the ZVS operation. The drain voltage and the inductor current are related by the input impedance of the load (Z_{in}):

$$Z_{in} = \frac{V_L}{I_L} = \frac{2V_{DD}}{\pi I_p} \exp j(\phi + \theta) \ ; \tag{3.6}$$

therefore, the real and imaginary parts of $Z_{in} = R_{in} + jX_{in}$ are given by

$$R_{in} = \frac{2V_{DD}}{\pi I_p} \cos(\phi + \theta) \tag{3.7}$$

$$X_{in} = \frac{2V_{DD}}{\pi I_p} \sin(\phi + \theta) \ . \tag{3.8}$$

As discussed, to maintain the ZVS operation, ϕ must be positive; thus, the duty cycle limit condition for a given load impedance is obtained by making $\phi = 0$ and combining Equations (3.6) and (3.2):

$$D_{min} = \frac{1}{2} - \frac{1}{2\pi} \arctan(\frac{X_{in}}{R_{in}}) \ . \tag{3.9}$$

The load factor α is defined as $\alpha = \frac{X_{in}}{R_{in}}$, so α is a factor in determining the duty cycle.

3.3 L-C Filter Design

Class D amplifiers need matching networks to achieve good performance. In this thesis, the L-C filter is designed based on the known transducers in [4]. The equivalent model of the transducer consists of a parallel capacitor C_o in parallel with a series inductor L_s, capacitor C_s, and resistor R_s. The transducer equivalent circuit is shown in Figure 3.5.

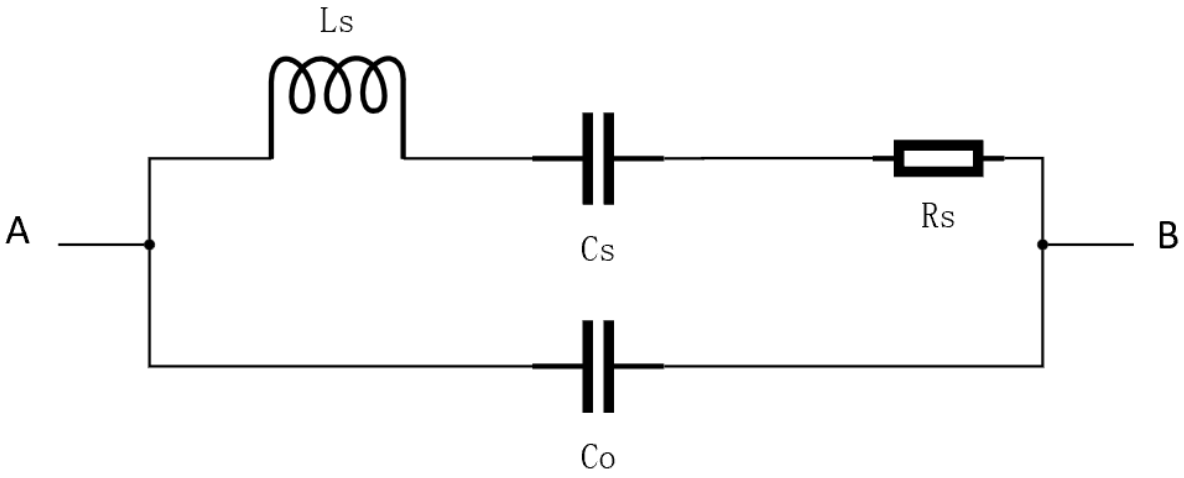

Figure 3.5: An equivalent circuit of the transducer.

The transducer equivalent impedance (Z_t) can be expressed as

$$Z_t = R_t + jX_t = \frac{1}{j\omega C_o + Y_s} = \frac{Gs}{G_s^2 + (B_s + \omega C_o)^2} - \frac{j(B_s + \omega C_o)}{G_s^2 + (B_s + \omega C_o)^2}\ , \tag{3.10}$$

where Y_s is the admittance of the series branch and Y_s expresses as $Y_s = \frac{1}{Z_s} = G_s + jB_s$. G_s and B_s are conductance and susceptance of the series branch.

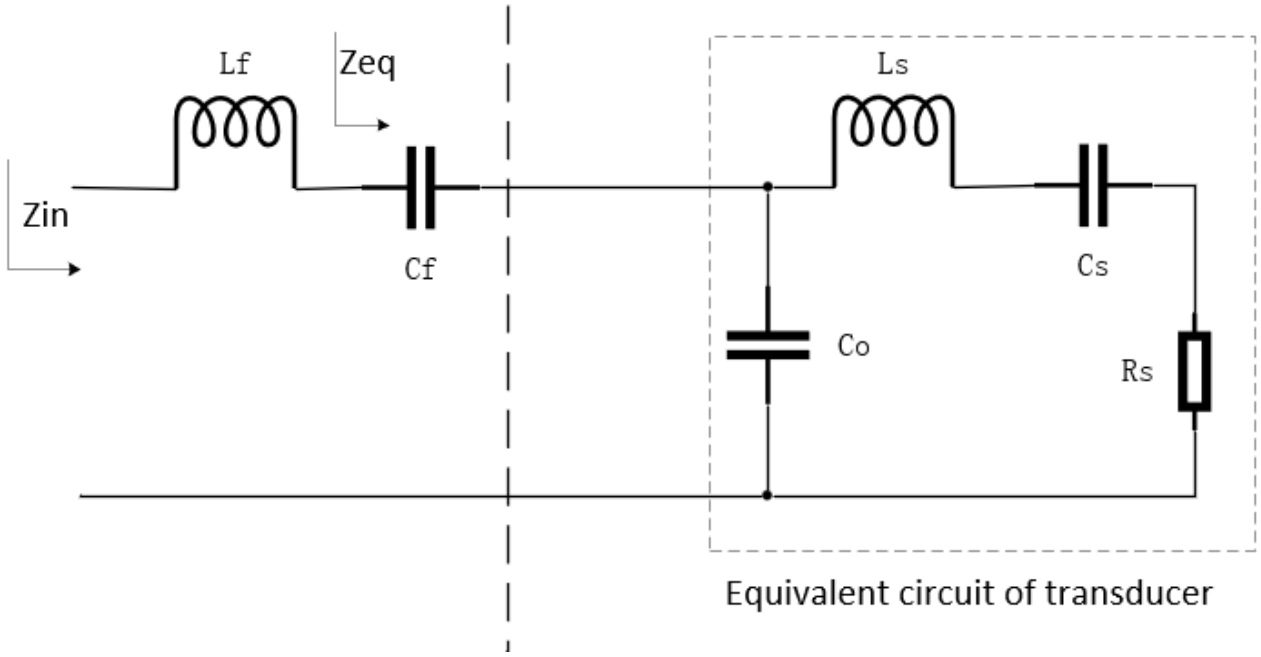

Figure 3.6: A diagram of an L-C type filter and the transducer.

The input impedance of the load is shown in Figure 3.6 and presented as

$$Z_{in} = R_{in} + jX_{in} = j\omega L_f + Z_{eq} = j\omega L_f + j(-\frac{1}{\omega C_f} + X_t) + R_t\ . \tag{3.11}$$

Z_{eq} is the impedance that consists of the filter capacitor C_f and transducer Z_t.

The design strategy is to make Z_{in} inductive and $Z_{eq} = R_{eq} + jX_{eq}$ capacitive with a quality factor that is high enough to ensure a sinusoidal current.

The quality factor of Z_{eq} is given by

$$Q = \frac{|X_{eq}|}{R_{eq}} = \frac{|-\frac{1}{\omega C_f} + X_t|}{R_t} \ . \tag{3.12}$$

Thus, the filter capacitor C_f can be estimated by setting Q to be a value near 3:

$$C_f = \frac{1}{\omega(Q \times R_t + X_t)} \ . \tag{3.13}$$

Once the filter capacitor C_f is obtained, the filter inductor L_f can be found from the ratio of the imaginary and real parts of the input impedance of the load, shown in the following derivation:

$$\alpha = \frac{X_{in}}{R_{in}} = \frac{\omega L_f - \frac{1}{\omega C_f} + X_t}{R_t} \ . \tag{3.14}$$

From equation (3.14), L_f is obtained, as shown below:

$$L_f = \frac{\alpha R_t + \frac{1}{\omega C_f} - X_t}{\omega} = \frac{(\alpha + Q)R_t}{\omega} \ . \tag{3.15}$$

For this design methodology, we propose to use Q=3; the low Q is used to both tolerate the parameter variation and ensure that the inductor current is sinusoidal. If Q is greater than 2.5, the current across the resonant circuit is a sine wave [7]. Therefore, when Q=3, the inductor is approximately a sine wave, satisfying the previous assumption.

Rearranging equation (3.11),

$$Z_{in} = R_{in} + jX_{in} = R_{in} + j\alpha R_{in} \ , \tag{3.16}$$

so the magnitude impedance $|Z_{in}| = R_t\sqrt{(1+\alpha^2)}$. Z_{in} influences the peak inductor current I_p, and I_p can be derived by

$$I_p = \frac{V_p}{|Z_{in}|} = \frac{2V_{DD}}{\pi R_t\sqrt{1+\alpha^2}} \ . \tag{3.17}$$

As shown in Eq(3.17), the peak value of the inductor current I_p may be low when R_t is large. If the inductor current is not large enough, the drain capacitor will not be entirely discharged during $[\theta_c, \theta_1]$. The inductor discharged current i_L is estimated by

$$i_L = \frac{dq_d}{dt} \ , \tag{3.18}$$

where q_d is the total drain charge.

Next, calculate the minimum value of I_p that discharges the drain capacitor entirely.

$$\begin{aligned} q_d &= \frac{T}{2\pi} \int_{\theta_c}^{\pi} I_p \sin(\theta - \phi) d\theta \\ &= \frac{I_p \cdot T}{2\pi} [-\cos(\pi - \phi) + \cos(\theta_c - \phi)] \ ; \end{aligned} \tag{3.19}$$

q_d can be expressed as a function of the drain capacitance C_{ds} using the following relation:

$$q_d = 2C_{ds} \cdot V_{DD} \tag{3.20}$$

Thus, the minimum I_p to discharge the drain capacitance fully is given by

$$I_p = \frac{4C_{ds} \cdot V_{DD} \cdot \pi}{T \cdot [-\cos(\pi - \phi) + \cos(\theta_c - \phi)]} \ . \tag{3.21}$$

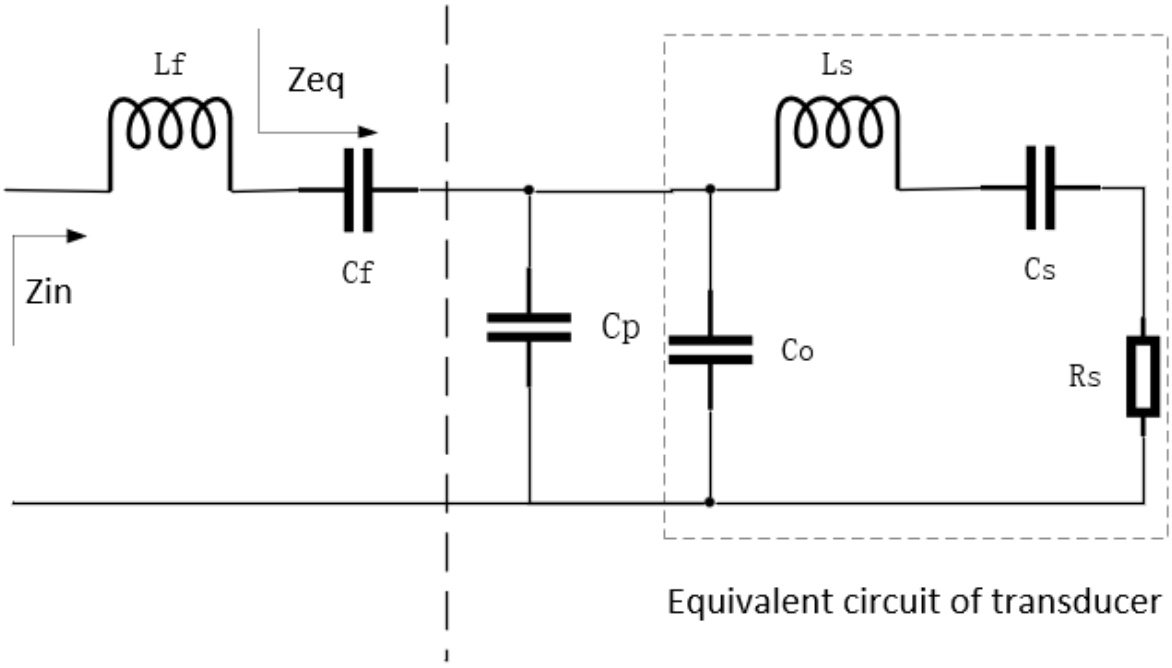

Figure 3.7: The input equivalent circuit for the load with the parallel capacitor.

If I_p is not high enough to fully discharge the drain capacitance, a capacitor C_p should be added in parallel with the transducer to increase I_p. The new equivalent circuit is shown in Figure 3.7, and the new impedance Z_t' is

$$\begin{aligned} Z_t' &= \frac{1}{j\omega(C_p + C_o) + Y_s} \\ &= R_t' + jX_t' \\ &= \frac{Gs}{G_s^2 + (B_s + \omega(C_p + C_o))^2} - \frac{j(B_s + \omega(C_p + C_o))}{G_s^2 + (B_s + \omega(C_p + C_o))^2} \,. \end{aligned} \tag{3.22}$$

The maximum acceptable R_t' is found by combining equation (3.21) with (3.17).

$$R_t' = \frac{T \cdot [-\cos(\pi - \phi) + \cos(2\pi D - \phi)]}{2C_{ds}\pi^2\sqrt{1+\alpha^2}} \,. \tag{3.23}$$

Compare R_t to R_t' can verify whether the inductor completely discharges the

drain capacitor or not. If $R_t > R'_t$, the drain capacitor will not be fully charged; else, the drain capacitor would be charged completely.

If R_t is too large, use equations (3.22) and (3.23) to obtain the parallel capacitor C_p.

$$C_p = \frac{\sqrt{(\frac{G_s}{R'_t} - G_s^2)} - B_s}{\omega} - C_o \ . \tag{3.24}$$

As previously discussed in the L-C calculation, we can use the same method to calculate the L-C filter.

3.4 Output power and power loss

The transducer impedance R_t is related to power when it is delivered to the transducer expressed as

$$P_o = \frac{I_p^2 \cdot R_t}{2} = \frac{2V_{DD}^2}{R_t(1+\alpha^2)\pi^2} \ . \tag{3.25}$$

There are a few losses when power is transferred to the load transducer, including the MOSFET loss P_m, the gate driver loss P_G, and the inductor loss P_L. All powers are average. The sum of these losses is the total power loss noted as P_{Loss}.

$$P_{Loss} = 2 \times (P_{sw} + P_D) + P_L + P_G = P_m + P_L + P_G \ . \tag{3.26}$$

When the transistor conducts, power consumption occurs. The power loss of the MOSFET (P_m) consists of the diode conduction loss (P_D) and the switch conduction loss (P_{sw}),

$$P_m = 2(P_{sw} + P_D) \ . \tag{3.27}$$

Since the two transistors operate symmetrically, both switches and both diodes have the same conduction loss. The switch average conduction loss (P_{sw}) is given as

$$\begin{aligned} P_{sw} &= \frac{1}{2\pi}\int_0^{\theta_c} r_{ds} I_p^2 \sin^2(\theta-\phi)d\theta \\ &= \frac{I_p^2 \cdot r_{ds}}{2\pi}\left(\frac{\theta_c}{2} - \frac{\sin 2(\theta_c-\phi)}{4} - \frac{\sin 2\phi}{4}\right) , \end{aligned} \tag{3.28}$$

where r_{ds} is the transistor turn-on resistance.

The diode $D2$ conduction power loss (P_{D2}) is

$$\begin{aligned} P_{D2} &= \frac{V_{D2}\cdot T}{2\pi}\int_{\theta 1}^{\pi} I_p \sin(\theta-\phi)d\theta \\ &= \frac{V_{D2}\cdot T\cdot I_p}{2\pi}\left[-\cos(\pi-\phi)+\cos(\theta_1-\phi)\right] , \end{aligned} \tag{3.29}$$

where V_{D2} is the voltage across the diode D2, and θ_1 is the start time of the diode conduction. If $\theta_1 = \pi$, there is no diode loss.

The inductor average power loss (P_L) in the series resonant inductor is

$$P_L = \frac{I_p^2 \cdot r_L}{2} , \tag{3.30}$$

where r_L is the inductor resistance.

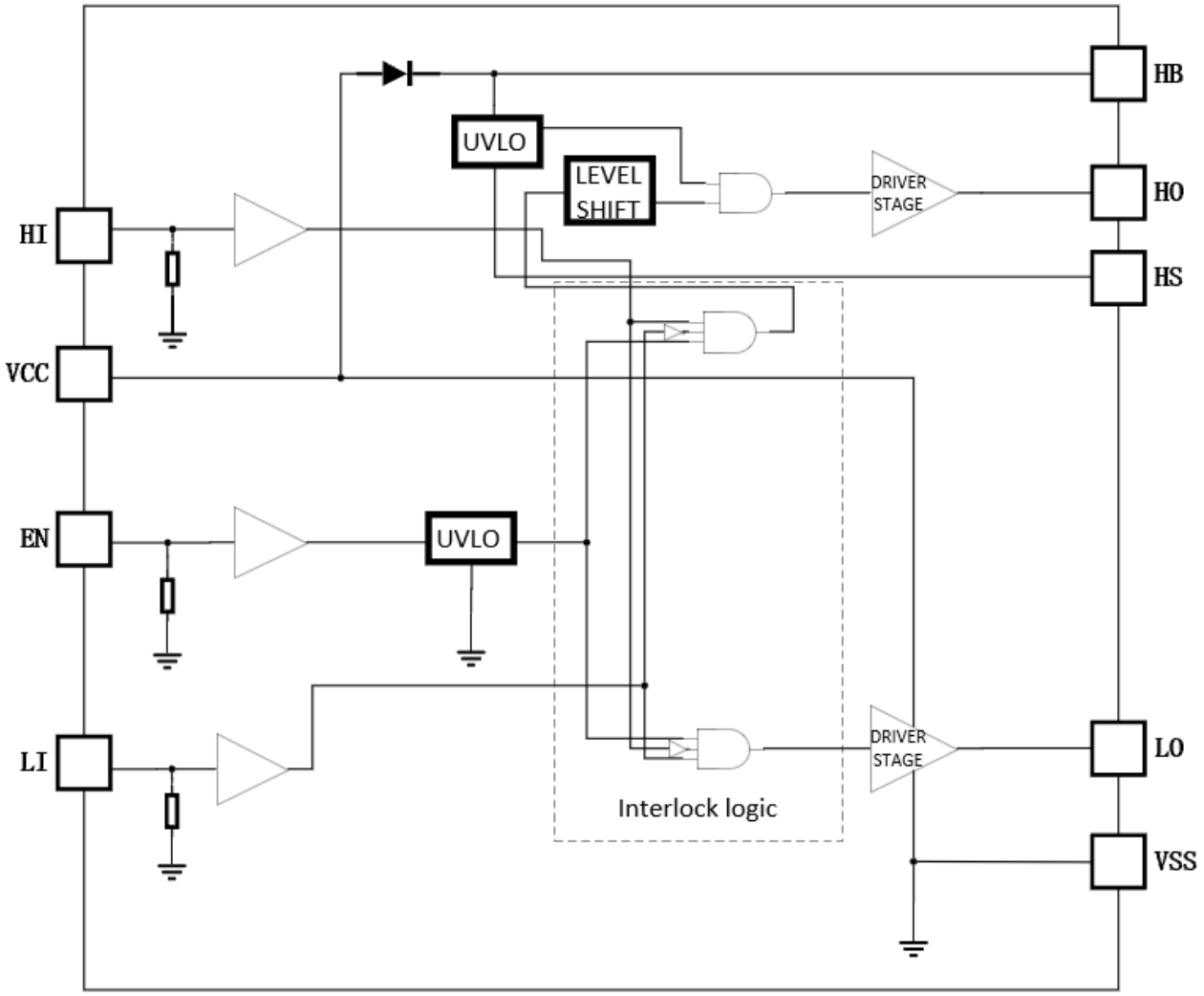

Figure 3.8: A block diagram of the gate driver.

Figure 3.8 illustrates a block diagram of the gate driver. The gate driver loss formulas and related parameters can be found from the UCC27282 datasheet; P_G consists of the static power loss (P_{QC}), the level-shifter loss (P_{IHBS}), the dynamic loss (P_{QG}), and the dynamic level-shifter loss P_{LS}.

$$P_G = P_{QC} + P_{IHBS} + P_{QG} + P_{LS} \ . \tag{3.31}$$

The static power loss (P_{QC}) is caused by the quiescent currents (I_{CC} and I_{HB}) and is described as

$$P_{QC} = (V_{CC} \times I_{CC}) + (V_{CC} - V_{DH}) \times I_{HB} \ , \tag{3.32}$$

where V_{CC} is the driver supply voltage, I_{CC} is the V_{CC} quiescent current, and the maximum value is 0.4mA. V_{DH} is the bootstrap diode forward voltage drop, I_{HB} is the HB quiescent current, and the maximum value is 0.4mA.

The high-side to low-side leakage current (I_{HBS}) generates the level-shifter loss (P_{IHBS}):

$$P_{IHBS} = (V_{CC} \times I_{HBS}) \times D \ , \tag{3.33}$$

where D is the high-side MOSFET duty cycle, and I_{HBS} is HB to VSS quiescent current. The maximum I_{HBS} is 50 μA.

The dynamic gate loss (P_{QG}) is due to the MOSFET gate charge (q_g) shown as

$$P_{QG} = 2 \times V_{CC} \times q_g \times f_{sw} \times \frac{R_{GD}}{R_{GD} + R_{GATE} + R_{GFET}} \ , \tag{3.34}$$

where q_g is the total MOSFET gate charge, and f_{sw} is the switching frequency. R_{GD} is the average value of pull-up and pull-down resistors, which is estimated as 4 Ω. R_{GATE} is the external gate drive resistor, and we assume no external gate driver resistors.

The parasitic level-shifter charge (q_p) on each switching cycle influences dynamic loss (P_{LS}) during high-side switching

$$P_{LS} = V_{HB} \times q_p \times f_{sw} \ , \tag{3.35}$$

where q_p is the parasitic charge.

As discussed before, the load factor (α) is related to the duty cycle. α is proposed to be 0.3, so the output power will not be controlled by the load factor and the duty cycle. From equation (3.9), the duty cycle is

$$D = \frac{1}{2} - \frac{1}{2\pi} \arctan(\frac{X_{in}}{R_{in}}) = 0.45 \ , \tag{3.36}$$

where ϕ is assumed to be zero.

3.5 Design Example

3.5.1 Transducer Data and Design Steps

The proposed design methodology of the Class D amplifier is

1. Determine the optimum operating frequency of transducers based on the acoustic conversion efficiency, and obtain the equivalent circuit component values.

2. Determine either the supply voltage or the desired load power of the amplifier.

3. Calculate the filter component values and select the gate drivers based on the equations presented in the previous section.

All six transducers parameters are shown in Table 3.1, and the design conditions are shown in Table 3.2.

Table 3.1: Transducer parameters

Transducer	A	B	C	D	E	F
Ls (μH)	195	203	162	175	170	208
Cs (pF)	130	125	156	145	148	121
Rs (Ω)	40	41	43	47	41	39
C_o (pF)	557	545	665	619	622	521
f_s (kHz)	998	1000	1002	999	1005	1003
f_p (kHz)	1106	1106	1109	1105	1114	1111

Table 3.2: Design parameters

Supply voltage V_{DD} (V)	30
Gate signal V_G (V)	10
Gate charge Q_g (nC)	8.3
Operating frequency (kHz)	1034
Load factor α	0.3

Substituting the above parameters into equations (3.23) and (3.24), the new load impedance R_t' and the parallel capacitor C_p can be calculated. R_t' is chosen to be 90% of the maximum value to ensure that there will be no switching losses. A lower R_t' value will result in a faster discharge of the drain capacitance and, thus, no switching losses. The calculated value of C_p from equation (3.23) and the chosen standard value C_p' are shown in Table 3.3.

Table 3.3: The parallel capacitances C_p and C_p'

Transducer	A	B	C	D	E	F
Exact C_p (nF)	2.86	2.75	3.21	2.95	3.32	3
Standard C_p' (nF)	3.3	3	3.6	3.3	3.6	3.3

Recalculate Z_t' using C_p' decremented by 5%. Using equation (3.15) with

Zt', calculate the required inductor for all transducers. Select the closest standard value that is higher than all the calculated values. The selected inductor is $L_f = 13\mu$H. Substitute $L_f = 13\mu H$ into the equation(3.15), the new Q' can be obtained. The filter capacitor C_f is found by

$$C_f = \frac{1}{\omega(Q' \times R'_t + X'_t)} , \tag{3.37}$$

which is rounded to the closest standard value. The nominal value of the input impedance Z'_{in} for the load is

$$Z'_{in} = Z'_t + j\omega L_f + \frac{1}{j\omega C_f} . \tag{3.38}$$

Using equation (3.38), the input impedance of the load Z'_{in} is found, as shown in Table 3.4.

Table 3.4: The nominal parameters results for six transducers

Transducer	A	B	C	D	E	F
Z'_{in} (Ω)	18.5+j9.3	21.3+j11.1	20.5+j9.4	20.6+j10.6	22.1+j10.3	20.8+j10.5
Q'	3.7	3.2	3.4	3.3	3.1	3.2
Exact C_f (nF)	15.31	21.76	6.29	8.13	6.2	12.51
Nominal C'_f (nF)	10	22	6.2	8.2	6.8	12

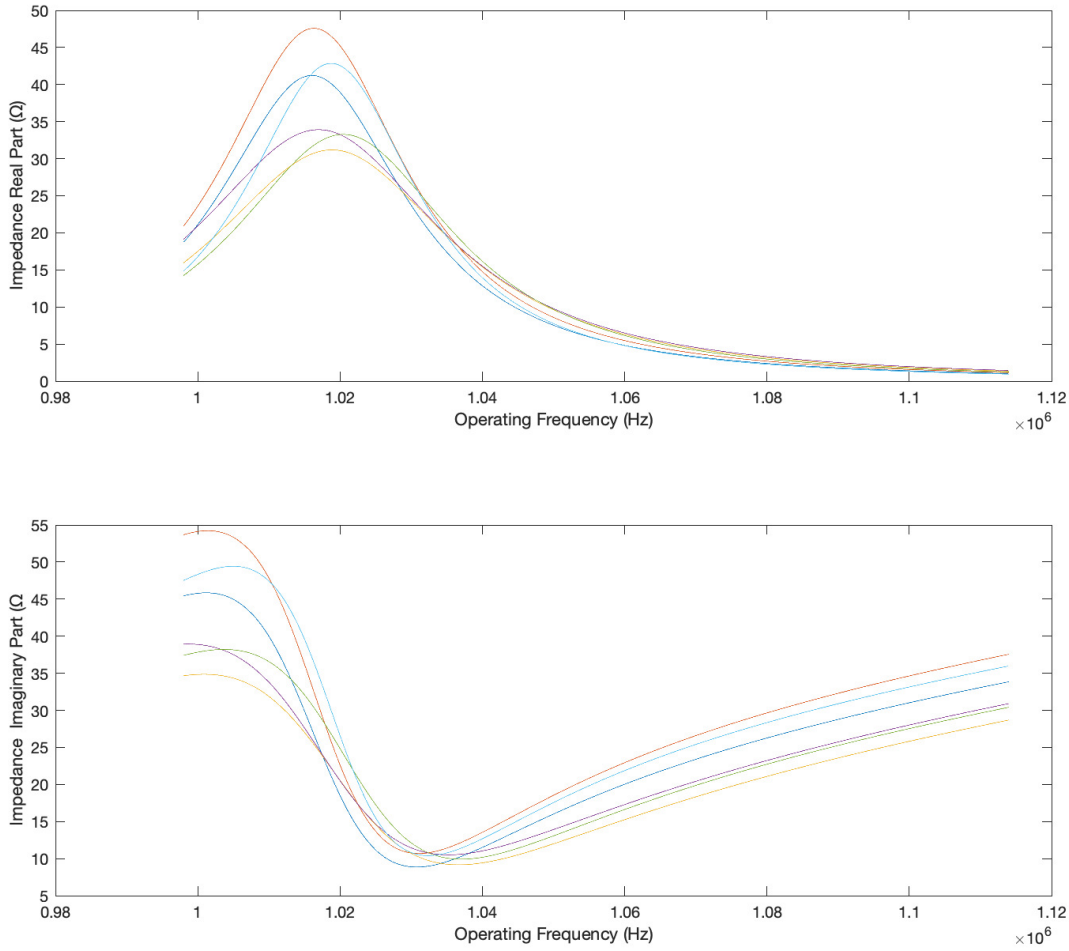

Figure 3.9: The relation between the operating frequency and the input impedance.

Figure 3.9 plots the nominal value of the input impedance of the load Z'_{in} variations versus the operating frequency. The x-axis is from the minimum series resonant frequency f_s = 998kHz to the maximum parallel resonant frequency f_p = 1114kHz. The y-axis is the nominal impedance of the load. As the frequency increases, the input impedance of the load is still inductive. At f=1034kHz, the load is inductive, as shown in Figure 3.9.

Since the L-C filter values are known, the nominal value of the input

impedance of the load Z'_{in} and the magnitude impedance of $|Z'_{in}|$ can be found. The inductor amplitude I_p, the output power P_o, the transistor loss P_m, the inductor lossP_L, and the gate loss P_G can be calculated by Eq(3.25), (3.27), (3.30), and (3.31).

3.5.2 Predicted Performance

Using the mentioned equations and parameters from Table 3.1 and Table 3.2, the exact values of C_f and C_p can be calculated for six different transducers. The calculation results are shown in Table 3.3 and Table 3.4. However, the maximum resistance for ZVS operations is the same for all transducers, and the calculated $I_p, P_o, P_m, P_L, P_G, P_{Loss}$ and η are also the same. The exact calculation results for all transducers are shown in Table 3.5 and Table 3.6.

Table 3.5: Exact calculation results for all transducers

Transducer	A	B	C	D	E	F
I_p (A)	0.68	0.68	0.68	0.68	0.68	0.68
P_o (W)	6.24	6.24	6.24	6.24	6.24	6.24

Table 3.6: Exact calculation results for all transducers

Transducer	A	B	C	D	E	F
P_m (mW)	124.9	124.9	124.9	124.9	124.9	124.9
P_G (mW)	72.9	72.9	72.9	72.9	72.9	72.9
P_L (mW)	4.7	4.7	4.7	4.7	4.7	4.7
P_{Loss} (mW)	202.4	202.4	202.4	202.4	202.4	202.4
η (%)	96.86	96.86	96.86	96.86	96.86	96.86

3.6 Simulation results

This section presents the example schematic and operation waveforms, simulation results and errors between simulation results and calculation results, showing how this designed amplifier works. The simulation aims to verify the amplifier analysis and the design methodology by testing how the amplifier responds to C_p and C_f variations. There are three sets of simulation results: the first set simulation uses the components that are identical to exact calculated values; the second set simulation employs the elements that are nominal values. The third set simulation uses 95% of nominal C_p' to verify that the amplifier still works if the components are at the lower limit of the tolerance.

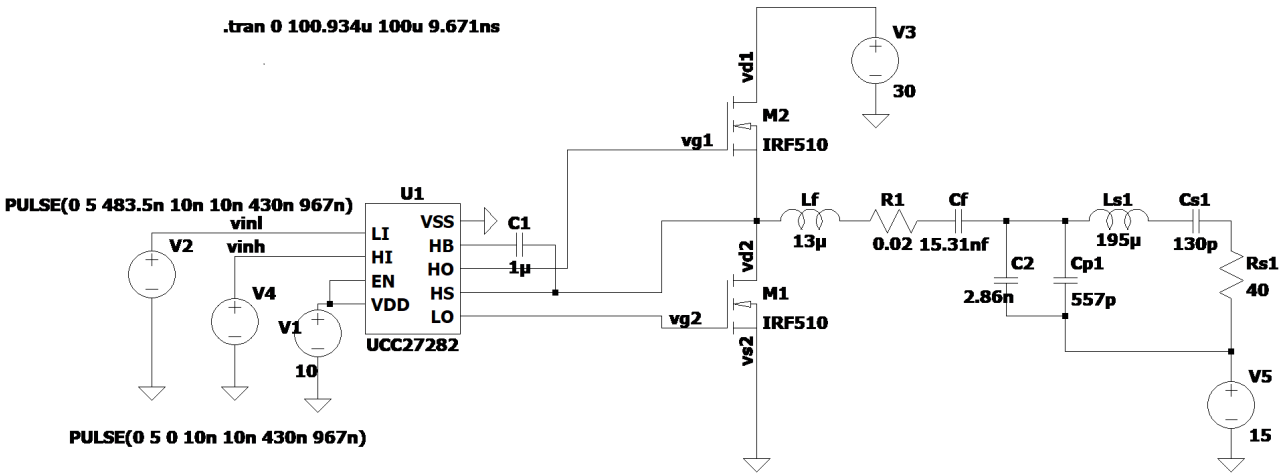

Figure 3.10: The schematic of the Class D amplifier for transducer A.

The transient simulations run for transducer A. The schematic of a Class D amplifier is shown in Figure 3.10, and the operation waveforms are shown in Figure 3.11.

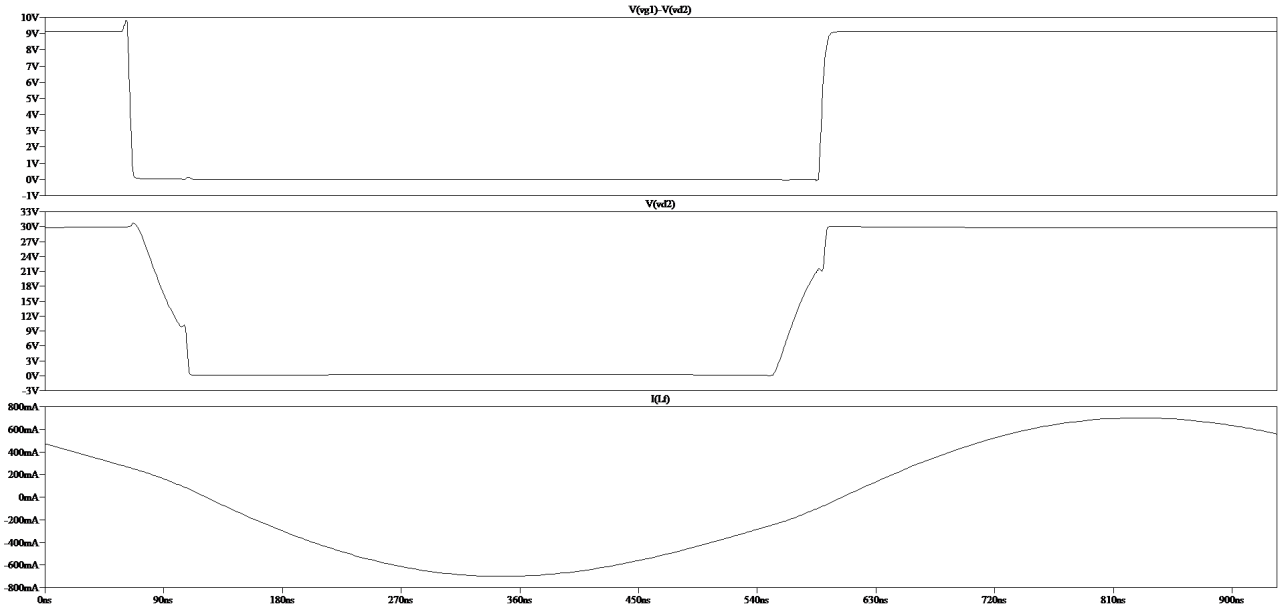

Figure 3.11: Waveforms of Vgs1,Vds1 and i_L.

Figure 3.11 plots the gate signal V_{gs}, the input voltage of the load V_{in}, and the inductor current i_L. The waveform of V_{in} shows that the switch turns ON, not at zero voltage, and there is a switching loss. The drain capacitor is not fully discharged because the parallel capacitor is not large enough. This indicates an error between analysis and practice.

Table 3.7 shows that the amplifier performances for six transducers, including inductor currents, average output power as well as average power losses of the transistor, gate driver and inductor, the total power losses, and efficiencies. The first simulation results using components of the exact calculated values are shown below.

Table 3.7: The first set of simulation results for all transducers

Transducer	A	B	C	D	E	F
I_p (A)	0.7	0.7	0.7	0.7	0.7	0.78
P_o (W)	6	6.78	6.73	6.73	6.73	7.42
P_m (mW)	167.76	167.88	170.83	171.18	172.55	159.69
P_G (mW)	60.21	60.55	60.56	60.41	60.67	60.52
P_L (mW)	5	5.02	4.93	4.91	6.03	6.19
P_{Loss} (mW)	232.97	233.45	238.41	236.5	239.25	226.4
η (%)	96.26	96.67	96.58	96.61	96.57	96.5

To check errors between the calculation and simulation using exact values, we can compare the output power, total power losses, and efficiency. Error calculations could be expressed as the following.

The output power error E_{po} is given by

$$E_{po} = \frac{P_{os} - P_{oc}}{P_{oc}} , \tag{3.39}$$

where P_{os} is the simulation value of the output power, and P_{oc} is the calculated value of the output power.

The total loss error E_{PLoss} is given by

$$E_{PLoss} = \frac{P_{Losss} - P_{Lossc}}{P_{Lossc}} , \tag{3.40}$$

where P_{Losss} is the simulation value of the total power loss, and P_{Lossc} is the value of the total power loss after calculation.

The overall efficiency error E_η is given by

$$E_\eta = \frac{\eta_s - \eta_c}{\eta_c} , \tag{3.41}$$

where η_s is the simulation value of the overall efficiency, and η_c is the computed value of the overall efficiency.

Table 3.8 shows the errors between the exact simulation and calculation. The output power differences are from -3.85% to 18.91% for E_{po}. The switching losses are assumed to be zero; however, there are switching losses in the simulation. Therefore, the power losses are different between calculation and simulation. The total power losses are from 11.86% to 18.21%. Even though power consumptions are different, the efficiency errors are close. The efficiencies are from -0.2% to -0.62%.

Table 3.8: Errors between the exact calculation and the first set simulation

Transducer	A	B	C	D	E	F
E_{po}	-3.85%	8.65%	7.85%	7.85%	7.85%	18.91%
E_{PLoss}	15.1%	15.34%	17.79%	16.85%	18.21%	11.86%
E_{η}	-0.62%	-0.2%	-0.29%	-0.26%	-0.3%	-0.37%

Table 3.9 shows the second set of simulation results for all transducers. The second simulation uses the nominal capacitances, which give tolerance to the load variations. The switch turns ON before V_{in} reaches V_{DD}, and the proposed amplifier satisfies ZVS operation so that the switching loss is zero. The simulation meets our assumptions.

Table 3.9: The second set of simulation results for all transducers

Transducer	A	B	C	D	E	F
I_p (A)	0.85	0.75	0.8	0.8	0.74	0.78
P_o (W)	7.4	6.39	7.02	6.69	6.53	6.63
P_m (mW)	182.18	145.02	159.68	152.78	141.5	158.54
P_G (mW)	65.52	63.58	62.62	63.58	62.34	63.82
P_L (mW)	8.35	6.21	7.07	6.67	6.06	6.63
$P_{Loss}(mW)$	256.05	214.81	228.67	223.03	209.9	228.99
η (%)	96.66	96.75	96.85	96.77	96.89	96.84

Table 3.10 shows the third set of simulation results. As mentioned before, the simulation uses 95 % of the nominal C_p'. The amplitudes of the inductor currents are high, so both output power and power consumptions are high. The power efficiencies among these three sets of simulations are closed to 97%.

Table 3.10: The third set of simulation results for all transducers

Transducer	A	B	C	D	E	F
I_p (A)	0.84	0.74	0.76	0.74	0.7	0.75
P_o (W)	7.66	7	6.95	6.79	6.44	6.81
P_m (mW)	170.44	141.54	145.93	140.49	131.2	147.14
P_G (mW)	62.06	62.09	62.16	61.94	61.75	61.33
P_L (mW)	7.64	5.66	6.21	5.45	5.31	6.07
P_{Loss} (mW)	239.52	209.29	214.34	207.88	198.26	213.99
η (%)	96.97	97.1	97.01	97.03	97.01	96.95

In summary, this proposed amplifier has a minimum theoretical efficiency of 96.26%, and it is relatively insensitive to changes in load impedance. Due to a low value of C_p, the load impedance also changes. If C_f and C_p have $\pm 5\%$ tolerance, there are nine combinations of C_f and C_p, as shown in Table 3.11. The calculation results are shown in TableA.1 in appendix A. Table A.1 shows the input impedance of the load Z_{in}, load factor α, maximum resistance R_t' for ZVS operation, and P_{Load} for six transducers. Resistances are from 24Ω to 30Ω, load factors are always positive, and the efficiencies are from 95.98% to 96.98%.

Table 3.11: All C_f and C_p combinations

Combination	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
C_f	nom.	+5%	-5%	nom.	nom.	+5%	+5%	-5%	- 5%
C_p	nom.	nom.	nom.	+5%	-5%	+5%	- 5%	+5%	-5%

3.7 Exploration of Proposed Amplifier Limitations

The output power could be increased by raising the supply voltage. For MOSET IRF510, the maximum drain-to-source voltage V_{DSmax} is 100V, and the maximum power dissipation is approximately 50W for all commercial-industrial applications. Given the design margin, we use 80V of supply voltage to estimate the maximum output power. Using the Eq(3.25), the output power could be estimated as 42.38W for transducer A. Simulating with the supply voltage increased to 80V, and Figure 3.12 illustrates the schematic of this Class D amplifier. The simulation use components that are nominal values and the operation waveforms are shown in Figure 3.13. Figure 3.13 shows that the amplifier operates for the ZVS operation, and the inductor current is close to a sine wave. The parallel capacitor makes the inductor fully discharge the drain capacitor. As a result, the amplifier also works if the supply voltage is elevated.

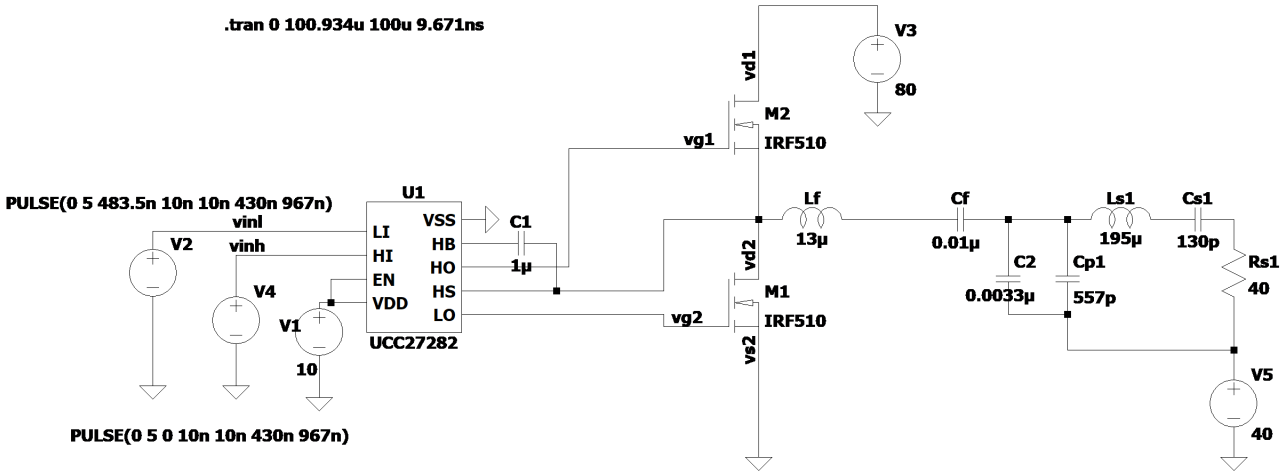

Figure 3.12: The schematic of the Class D amplifier at V_{DD}=80V

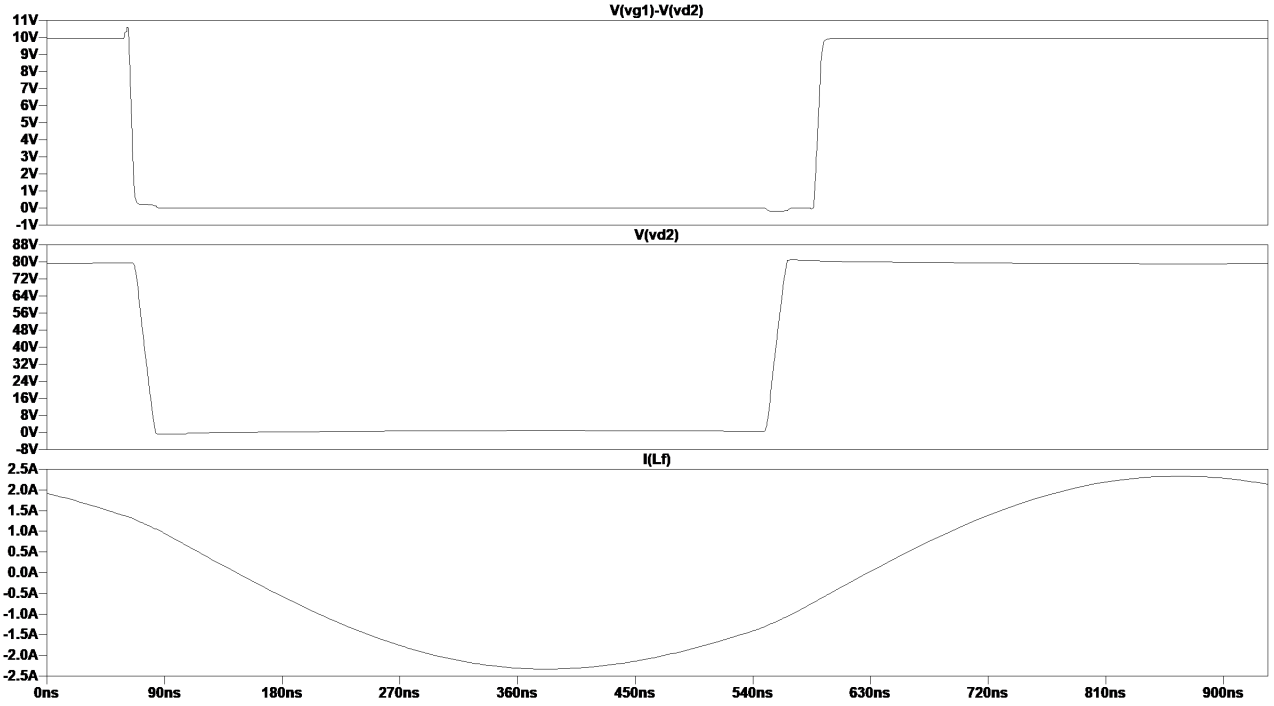

Figure 3.13: Waveforms of Class D amplifier operation at V_{DD}=80V

The simulation results for all six transducers are shown in Table 3.12. When the supply voltage is 80V, the amplifier can provide around 50W of output power with an efficiency of 97%.

Table 3.12: Simulation results at V_{DD}=80V

Transducer	A	B	C	D	E	F
I_p (A)	2.33	2.2	2.14	2.08	1.98	2.07
P_o (W)	52.61	45.53	50.03	47.66	46.49	47.29
P_m (W)	1.08	0.82	0.92	0.88	0.81	0.88
P_G (mW)	75.59	74.52	73.83	74.52	73.48	74.32
P_L (mW)	59.55	44.05	44.36	47.49	43.23	47.26
$P_{Loss}(W)$	1.23	0.97	1.09	1.04	0.95	0.99
η (%)	97.72	97.91	97.87	97.86	98	97.95

Table 3.12 shows that both output power and efficiencies for the six transducers are high. When output power increases, the power dissipation also rises. If the MOSFET power dissipation is large, the dissipated power is transferred into heat that raises the junction temperature. For safety, the junction temperature T_J should not exceed a specific maximum T_{Jmax}. Thus, if the temperature exceeds T_{Jmax}, a heat sink should be added. We can estimate the maximum power dissipation of the transistor by

$$R_{\theta JA} = \frac{T_{Jmax} - T_A}{P_D} , \tag{3.42}$$

where T_A is the ambient temperature, and P_D is the MOSFET power dissipation [25]. According to the MOSFET(IRF510) datasheet , the maximum junction temperature is $175°C$, and the maximum junction-to-ambient resistance is $62°C/W$. We assume T_A is $50°C$ for safe in this design; thus, the

maximum power dissipated without a heat sink is

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{JA}} = 2.02W \ . \tag{3.43}$$

The power consumption of the transistorcan be found in Table 3.13. P_m is the loss of two transistors, so the power consumption of each transistor is $\frac{P_m}{2}$. For transducer A, the power is consumed at 0.54W, which is less than 2.02W. Therefore, this design does not need a heat sink.

Chapter 4

Conclusions

4.1 Conclusion

This thesis presents a new design methodology of a ZVS Class D amplifier to drive ultrasound transducers. This aims to provide high output power with high efficiency. There are several advantages to this design:

1. The amplifier topology is simple, flexible, and low-cost. If this design is implemented in the lab, it requires a variable DC voltage supply, a gate driver, two NMOSs, an L-C filter, and a parallel capacitor.

2. The amplifier is tolerant within a range of loading impedance variations ($\pm 5\%$).

3. The proposed amplifier delivers up to 50W of power to the load at f=1034kHz with 97% efficiency. The switching loss of this proposed amplifier is low because of the ZVS operation.

However, the amplifier has its drawbacks:

1. The amplifier requires a variable DC supply to adjust the load power.

2. The amplifier needs to be tuned for a specific frequency.

4.2 Future work

This design is a theoretical analysis, and it still needs to be implemented in practice. The pulse generation module should be added, and it can be achieved by PWM technology.

Experimental results and simulation results may differ. In the thesis, the design methodology eliminates the switching loss at the expense of diode losses. In the future, there should be an analysis to compare the switching losses to the diode losses. Also, the mathematical sensitivity should be analyzed, which would help to understand the critical parameters.

Appendix A

Calculation Results of Nine Capacitor Combinations For Amplifiers

Table A.1: Calculation results of nine capacitor combinations for amplifiers

Transducer	Combination	Zin (Ω)	α	R_t' (Ω)	P_{Load} (W)	η (%)
A	(1)	18.5 + j9.3	0.5	27.8	7.87	96.39
	(2)	18.5 + j10	0.54	27.3	7.62	96.37
	(3)	18.5 + j8.5	0.46	28.3	8.15	96.41
	(4)	16.3 + j12.7	0.78	24.5	6.97	95.92
	(5)	21 + j5.8	0.27	30	8.07	96.74
	(6)	16.3 + j13.4	0.83	24	6.67	95.89
	(7)	21 + j6.5	0.31	29.7	7.92	96.73
	(8)	16.3 + j13.4	0.83	24	6.67	95.89
	(9)	21 + j5	0.24	30.3	8.22	96.76

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Table A.1: Calculation results of nine capacitor combinations for amplifiers

Transducer	Combination	Zin (Ω)	α	R'_t (Ω)	P_{Load} (W)	η (%)
B	(1)	21.3 + j11.1	0.52	27.6	6.72	96.65
	(2)	21.3 + j11.4	0.54	27.4	6.64	96.64
	(3)	21.3 + j10.7	0.5	27.8	6.82	96.66
	(4)	18.8 + j14.8	0.79	24.5	6	96.23
	(5)	24.4 + j7.1	0.29	29.9	6.9	96.97
	(6)	18.8 + j15.1	0.8	24.3	5.89	96.21
	(7)	24.4 + j7.4	0.3	29.8	6.85	96.97
	(8)	18.8 + j14.4	0.77	24.7	6.11	96.24
	(9)	24.4 + j6.7	0.27	30	6.96	96.23
C	(1)	20.5 + j9.4	0.46	28.3	7.36	96.62
	(2)	20.5 + j10.6	0.52	27.7	7.03	96.58
	(3)	20.5 + j8.1	0.39	29	7.7	96.65
	(4)	18.3 + j11.8	0.64	26.2	7.06	96.28
	(5)	23.1 + j6.8	0.3	29.8	7.25	96.89
	(6)	18.3 + j12.9	0.71	25.4	6.65	96.23
	(7)	23.1 + j8	0.35	29.4	7.04	96.87
	(8)	18.3 + j10.4	0.57	27	7.52	96.32
	(9)	23.1 + j5.5	0.24	30.3	7.46	96.92
D	(1)	20.6 + j10.6	0.51	27.7	7.01	96.60

Continued on next page

Table A.1: Calculation results of nine capacitor combinations for amplifiers

Transducer	Combination	Zin (Ω)	α	R'_t (Ω)	P_{Load} (W)	η (%)
	(2)	20.6 + j11.4	0.55	27.2	6.76	96.57
	(3)	20.6 + j9.6	0.46	28.2	7.28	96.62
	(4)	18.3 + j13.3	0.73	25.2	6.51	96.22
	(5)	23.2 + j7.7	0.33	29.5	7.08	96.88
	(6)	18.3 + j14.2	0.78	24.6	6.21	96.18
	(7)	23.2 + j8.6	0.37	29.2	6.91	96.86
	(8)	18.3 + j12.3	0.67	25.8	6.85	96.26
	(9)	23.2 + j6.7	0.29	29.9	7.25	96.90
E	(1)	22.1 + j10.3	0.46	28.2	6.78	96.74
	(2)	22.1 + j11.3	0.51	27.7	6.53	96.71
	(3)	22.1 + j9.1	0.41	28.8	7.06	96.77
	(4)	22.1 + j10.3	0.46	28.2	6.78	96.74
	(5)	25 + j7.7	0.31	29.9	6.67	97
	(6)	22.1 + j11.3	0.51	27.7	6.0	96.36
	(7)	25 + j8.7	0.35	29.4	6.5	96.98
	(8)	22.1 + j9.1	0.41	28.8	7.06	96.77
	(9)	25 + j6.5	0.26	30.1	6.83	97.20
F	(1)	20.8 + j10.5	0.51	27.8	6.97	96.61
	(2)	20.8 + j11.2	0.54	27.4	6.8	96.61

Continued on next page

Table A.1: Calculation results of nine capacitor combinations for amplifiers

Transducer	Combination	Zin (Ω)	α	R'_t (Ω)	P_{Load} (W)	η (%)
	(3)	20.8 + j9.9	0.47	28.1	7.15	96.60
	(4)	19 + j13	0.69	25.6	6.53	96.63
	(5)	23.7 + j7	0.29	29.9	7.08	96.87
	(6)	19 + j13.6	0.72	25.3	6.34	97.11
	(7)	23.7 + j7.6	0.32	29.6	6.98	96.29
	(8)	19 + j12.4	0.65	26.1	6.75	96.99
	(9)	23.7 + j6.3	0.26	30.1	7.18	96.94

Bibliography

[1] T. H. Gail,"Therapeutic applications of ultrasound", *Progress in biophysics and molecular biology*, Elsevier, vol. 93, no.1-3, pp.111-129, 2007.

[2] B. E. O'Neill, H. Vo, M. Angstadt, K. P. C. Li, T. Quinn, and V. Frenkel, *Pulsed High Intensity Focused Ultrasound Mediated Nanoparticle Delivery: Mechanisms and Efficacy in Murine Muscle,* Ultrasound in Medicine and Biology, vol. 35, no. 3, pp. 416–424, Mar. 2009.

[3] A. Yudina and C. Moonen, *Ultrasound-induced cell permeabilisation and hyperthermia: Strategies for local delivery of compounds with intracellular mode of action,* International Journal of Hyperthermia, vol. 28, no. 4, pp. 311–319, Jun. 2012.

[4] J. L. Kivenen, "A Device for Performing Sonoporation on Adherent Cell Cultures", *MSc Thesis Dissertation*, Lakehead University, 2014.

[5] K. Nakamura, *Ultrasonic transducer: Materials and design for sensors, actuators and medical applications,* Reference and Research Book News, vol.27, pp. 1-3, 2012.

[6] A. Arnau, "Piezoelectric Transducers and Applications. 2nd ed.", ch.1, p. 18, p. 23, ch.18, sec. 18.3, pp. 467–472, New York: Springer, 2008.

[7] M. K. Kazimierczuk, *RF Power Amplifiers, Second edition*, 2015.

[8] M. Albulet, *RF Power Amplifiers*, Noble Publishing Corporation, 2001.

[9] L. Svilainis, V. Dumbrava and G. Motiejunas, "Optimization of the ultrasonic excitation stage," *30th International Conference on Information Technology Interfaces*, ITI, pp. 791–796, 2008.

[10] L. Capineri, "A 15 MHz Bandwidth, 60 Vpp, Low Distortion Power Amplifier for Driving High Power Piezoelectric Transducers," *Review of Scientific Instruments,* Italy,2014, AIP Publishing LLC.

[11] D. Ghisu, A. Gambero, M. Terenzi, G. Ricotti, A. Moroni and S. Rossi, "180Vpp output voltage, 24MHz bandwidth, low power class AB current-feedback high voltage amplifier for ultrasound transmitters," *2018 IEEE Custom Integrated Circuits Conference (CICC),* pp. 1-4, San Diego, CA, 2018.

[12] D. Bianchi F. Quaglia, A. Mazzanti and F. Svelto, "Analysis and Design of a High Voltage Integrated Class-B Amplifier for Ultra-Sound Transducers," *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol. 61, no. 7, pp. 1942-1951, July 2014.

[13] O. Farhanieh, Shafi,R. Roy, A. Ergun, A. Bozkurt, "Integrated HIFU Drive System on a chip for CMUT-Based Catheter Ablation System," *IEEE Trans. on Biomedical Circuits and Systems,* ,vol.11, No.3, 698-7012017.

[14] W. T. Ang, C. Scurtescu, W. Wing Hoy, T. El-Bialy, Y. Y. Tsui and J. Chen, "Design and Implementation of Therapeutic Ultrasound Generating Circuit for Dental Tissue Formation and Tooth-Root Healing," *IEEE Trans. on Biomedical Circuits and Systems,* vol. 4, no. 1, pp. 49–61, Feb 2010.

[15] T.Hall and C. Cain,"A Low Cost Compact 512 Channel Therapeutic Ultrasound System For Transcutaneous Ultrasound Surgery," *AIP Conf. Proc.,* vol. 829, pp.445-449, May 8, 2006.

[16] G. Lewis and W. Olbricht,"Design and characterization of a high-power ultrasound driver with ultralow-output impedance," *Rev. Sci. Instrum,* vol. 80, p. 114704, 2009.

[17] K. Agbossou, J. Dion, S. Carignan, M. Abdelkrim and A. Cheriti, "Class D amplifier for a power piezoelectric load," *IEEE Trans. on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 47, pp. 1036-–1041, 2000.

[18] L. Yang, L. Xu, T. Yang and B. Zhang," Class D power amplifier for audio beam system," *International Conference on Mechatronics and Automation, ICMA,* pp. 3469-3474, 2007.

[19] T. Yuan, X. Dong, H. Shekhani, C. Li, Y. Maida, T. Toku, K. Uchino, "Driving an inductive piezoeletric transducer with class E inverter," *in Sensors and Actuators A: Physical,* pp.219-227, 2017.

[20] J. Kim and J. Lee, "Theoretical Resonance Analysis of Langevin Transducers with Equivalent Circuit Models for Therapeutic Ultra-

sound,"*Journal of Electrical Engineering & Technology,* vol.14, no. 6, pp. 2437-2445, 2019.

[21] H. L. Cheng, C. A. Cheng, C. C. Fang and H. C. Yen, "Single-switch high power factor inverter for driving piezoelectric ceramic transducer", *International Conference on Power Electronics and Drive Systems, PEDS, 2009* pp. 1571–1576, 2009.

[22] C. Christoffersen, W. Wong, S. Pichardo, G. Togetma and L. Curiel,"class DE Ultrasound Transducer Driver for HIFU Therapy," *IEEE Trans. on Biomedical Circuits And Systems,* vol. 10, No.2, pp. 375-382, 2016.

[23] C. Christoffersen, Samuel Pichardo, Laura Curiel,"An integrated full-bridge class DE ultrasound transducer driver for HIFU applications," *Proceedings of the 2016 IEEE NEWCAS Conference, Vancouver,* pp.1-4, June 2016.

[24] T. Ngo, R. Song, Y. Zhou, S. Pichardo, and L. Curiel, "Quasi Class-DE Driving of HIFU Transducer Arrays," *IEEE Trans. on Biomedical Circuits And Systems,*vol. 13, No. 1, pp. 214–224, 2019.

[25] Adel.S Sedra and Kenneth C. Smith, " Microelectronics Circuits. 8th ed.", ch.12, p. , New York, 2020.

[26] Niyomthai, Saransak, et al. "Operation Region of Class E Resonant Inverter for Ultrasonic Transducer," *International Conference on Electrical*

Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 14th, pp. 435–38, IEEE, 2017.

[27] Harvey, Gerald, et al. "Review of High-Power Ultrasound-Industrial Applications and Measurement Methods," *IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control,* vol. 61, no. 3, pp. 481–95, Mar. 2014.