Gallium Nitride on Low Temperature Cofired Ceramic Templates for Schottky Junctions

Jonny Tot

Presented to the faculty of Electrical and Computer Engineering in partial fulfillment for a Ph.D. degree

Lakehead University
Thunder Bay, Ontario
April 2021

Acknowledgments

I would like to acknowledge the help I received throughout my research by my lab partners, supervisor, friends, and family. My time spent in the semiconductor lab was a great period of learning and growth that could not have been done without the people there. Each of them is not just a colleague but a friend who helped this research progress through meaningful discussion and debate. I would like to thank Dr. Dimiter Alexandrov for giving me the opportunity to join the lab and for the endless encouragement I received to try new ideas from him. He truly helped me understand that even undesirable results are still results and are meaningful in forming a complete understanding. I would also like to thank my family for putting up with my seemingly endless journey through academia from kindergarten to now. They have always believed in me and supported my ambitions, even when I may have felt aimless. I wish to dedicate this work to my father who could not be with me to see its completion, I know he would be proud and is sorely missed.

Abstract

In this work aluminum, silicon and zinc oxide were used as intermediate layers for thin film growth on cofired glass ceramic substrates. The motivation behind this work is a direct deposition of nitride thin films on the surface of the ceramic substrate, eliminating the die and attach techniques. Ceramics have unique applications due too the nature of their mechanical processing, and their physical resilience and chemical inertness. The low melting of the glass ceramics from a device processing perspective and their rough, inhomogeneous surface presents a challenge for device fabrication. Oxide materials can be applied by a variety of techniques compatible with large device areas and arbitrary shapes to apply a surface texture to improve thin film properties for device fabrication. Ideally these techniques could be applied to any substrate that meets the thermal budget of the thin film process.

Solution coating was found to be a good candidate for applying coatings since it can deposit many different oxide materials over large areas, for relatively low cost, and surface tension of the liquid phase helps to planarize the surface. Several (>7) microns of coating materials were found to be needed to reduce the appearance of the ceramic surface features.

Deposition of GaN on the surface of the oxide coatings was performed using a Flow Modulation Epitaxy (FME) style deposition in conjunction with a unique hollow cathode plasma source. These features are designed to lower the overall temperature requirements for GaN growth by providing additional Ga migration time during growth and by using nitrogen plasma as an alternative to thermal decomposition of ammonia. Ni/Au Schottky junctions fabricated on sapphire using ceramic compatible temperatures and FME show leaky characteristics with high ideality factors, indicating tunneling is a significant contributor to carrier transport through the junction.

The same Ni/Au GaN devices fabricated on ZnO coated ceramics was found to produce ohmic junctions. The density of surface states is a likely candidate for this behaviour.

Contents

List of Figures

List of Tables

List of Publications

1. Tot, J., R. Dubreuil, B. Kadikoff, M. Nagorski, and D. Alexandrov. "Energy Bandgap of InN," In Press.

2. J. M. Mánuel, J. J. Jiménez, F. M. Morales, B. Lacroix, A. J. Santos, R. García, E. Blanco, M. Domínguez, M. Ramírez, A. M. Beltrán, D. Alexandrov, J. Tot, R. Dubreuil, V. Videkov, S. Andreev, B. Tzaneva, H. Bartsch, J. Breiling, J. Pezoldt, M. Fischer, and J. Müller, "Engineering of III-Nitride Semiconductors on Low Temperature Co-fired Ceramics," Sci. Rep., vol. 8, no. 1, p. 6879, May 2018, https://doi.org/10.1038/s41598-018-25416-6.

3. D. Alexandrov, J. Tot, R. Dubreuil, F. M. Morales, J. M. Mánuel, J. J. Jiménez, B. Lacroix, R. García, V. Videkov, S. Andreev, B. Tzaneva, H. Bartsch, J. Pezoldt, M. Fischer, and J. Mueller, "Low Temperature Epitaxial Deposition of GaN on LTCC Substrates," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2017, pp. 48–54, https://doi.org/10.1109/WiPDA.2017.8170501.

4. Kadikoff, B., R. Dubreuil, J. Tot, and D. Alexandrov. "Investigation into the Characteristics of DC Nitrogen Plasma Used for Group III-N Semiconductor Thin-Film Growths." In *2018 41st International Spring Seminar on Electronics Technology (ISSE)*, 1–5, 2018. https://doi.org/10.1109/ISSE.2018.8443696.

5. Tot, J., R. Dubreuil, and D. Alexandrov. "Low Temperature Growth of InAlN on Epitaxially Grown SiC/Si (111) Wafers." In *2017 40th International Spring Seminar on Electronics Technology (ISSE)*, 1–5, 2017. https://doi.org/10.1109/ISSE.2017.8000892.

Posters Presented

R. Dubreuil, J. Tot, and D. Alexandrov, "GaN Growth on ceramics by Low Temperature RP-MOCVD", poster presented at the 13th annual International Conference on Nitride Semiconductors (ICNS-13), July 9, 2019.

J. Tot, A. Kakanakova-Georgieva, and D. Alexandrov, "Low-temperature deposition of InN layers on high-temperature MOCVD grown AlN layers", poster presented at the International Workshop on Nitride Semiconductors (IWN) 2016.

Oral presentations

"Low Temperature Growth of InAlN on Epitaxially Grown SiC/Si (111) Wafers." In 2017 40th International Spring Seminar on Electronics Technology (ISSE)

1. Background Information

1.1 Nitride History

Group III-V semiconductors are binary semiconductor compounds used in many electro-optic and high frequency applications within electronics used as alternatives to silicon. This is often due to a direct bandgap, meaning they can efficiently absorb or emit radiation at or above their bandgap energy, or they exhibit improved electron mobility and or breakdown characteristics compared to silicon.

Table 1: Comparison of some III-V materials properties and silicon [1], [2]

Material	Mobility (cm^2/Vs)	Critical field (V/cm)	Bandgap (eV)	Type
Si	1400	300000	1.12	indirect
GaAs	8500	500000	1.424	direct
GaP	250	100000	2.26	indirect
GaSb	3000	50000	0.726	direct
InAs	44000	40000	0.354	direct
InP	5400	500000	1.344	direct
InSb	77000	1000	0.17	direct
GaN	1400	$3.0\text{-}5.0 \times 10^6$	3.42	direct

Historically the group III materials have consisted of aluminum, gallium, and indium, while the group V materials have been phosphorus, arsenic, and antimony. Binary (GaAs, InP), ternary (e.g. $Al_xGa_{1-x}As$) and even quaternary ($In_xAl_yGa_{1-x-y}As$) alloys have been studied for several decades due too the ability to produce closely matched bulk wafers through a liquid phase growth process such as Czochralski or Bridgman processes. This allows for relatively cheap substrates to be produced with low defect densities ($<10^5\ cm^{-3}$) and high purity.

Group III (Al, Ga, In) -Nitride based materials however were hindered because they cannot be grown with these techniques due to the high vapour pressure of nitrogen and high melting point

of nitrides, leading to dissociation of nitrogen from the material well before melting. Without the ability to produce wafers through liquid melt techniques, native substrates relied on vapour deposition techniques which are comparatively slow and expensive, causing wafers greater than 2" to be unavailable at a commercial scale. While bulk production of GaN wafers offers the highest quality materials for devices, it is not at a point to commercially compete with crystal growth of nitrides on foreign substrates (heteroepitaxy on Al_2O_3, 6H-SiC and more recently Si). Heteroepitaxy has seen commercial success since the 90's with the blue LED, however heteroepitaxial growth inevitably leads to a high degree of threading defects ($>10^9$ cm^{-2}) extending from the interface of the two materials due too the mismatches involved. A variety of techniques such as AlN interface buffer layers [3], low temperature nucleation layers [4], and selective area growth [5] techniques have lowered dislocation densities in device epilayers to $<10^7$ cm^{-2} [6].

Many different growth techniques have been developed for GaN epitaxy specifically, since most devices only use low alloy content AlGaN or InGaN for junctions/quantum wells. Most techniques rely on the thermal decomposition of ammonia (NH_3) as a source of nitrogen for the growth, requiring temperatures of at least 600 °C to begin efficient production of atomic ammonia (Figure 2) and high V/III ratios to help prevent nitrogen desorption [2].

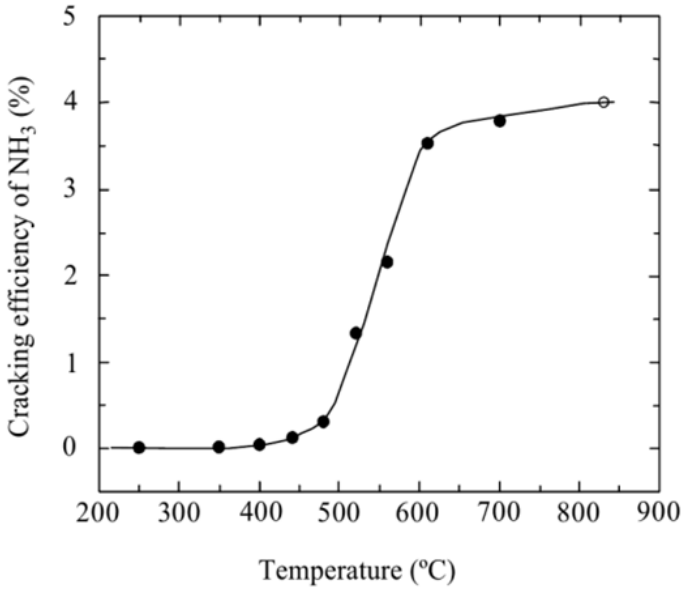

Figure 1:Decomposition efficiency of ammonia as a function of temperature. The lower limit of atomic nitrogen production using ammonia is shown to be 600 ˚C from the characteristics of this curve [5].

Temperatures higher than 600 °C are used to enhance surface migration of the metal species during growth, a typical growth temperature is 1050 °C using chemical vapour deposition (CVD) [7]. In the absence of additional energy input (plasma, laser excitation), the thermal energy largely determines the surface morphology by limiting the migration of deposition species on the surface, controlling the grain size and growth rate of different crystal planes. Figure 2 illustrates how the relative growth rate of the crystal planes changes with temperature and pressure [5].

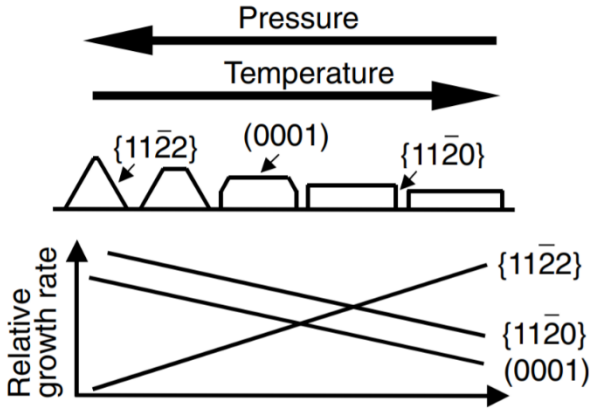

Figure 2: The effect of temperature and pressure on controlling the relative growth rate of different hexagonal planes [5].

In the interest of transparent and flexible illumination/display technology more advanced processing technologies have been used to deposit crystalline InN, GaN, AlN and ternary alloys at temperatures well below 1050 °C [8]–[12]. Plasma based techniques are effective in lowering the overall thermal budget, with crystalline GaN being deposited between 400 °C and 500 °C on a range of substrates including glasses [13]–[16]. Much of the underlying defects are still largely unavoidable however due too the lattice and thermal mismatch with the substrate material and dislocations are still prone to appear in these low temperature techniques.

1.2 Motivation

A growing field of research in nitride materials is their application to extreme environment electronics. These include exposure to corrosive environments, various forms of radiation, and high temperatures [17]. The high temperature stability of wide bandgap semiconductors an attractive feature for aerospace and space exploration, engine monitoring, flame detection and deep well drilling where bulk silicon technologies face fundamental material challenges [18]. In many of these applications the use of passive or active cooling is not feasible or may add unwanted cost and weight to designs. While wide bandgap materials enable device operation, there are many other challenges associated with device level design in these environments that extend past the active material. Contact metallization, die attach mechanisms and device packaging are also significant challenges to consider.

The die packaging is critical to device reliability and in extreme environments. Conventional FR4 PCB's have a glass transition of 130-170 °C and should not be operated close to this temperature. At temperatures beyond this, inorganic ceramics or metals are used due too their thermal stability and high thermal conductivity compared to organic materials. Low

temperature cofired ceramics (LTCC) or glass-ceramic composites, are low-cost materials that are resilient enough for these applications with a wide range of electrical/physical properties available by their composition [19]–[22]. The nature of ceramic processing also allows these materials to be shaped, cut, and folded much like a plastic prior to firing. Embedded cavities and conductors can also be created for a wide range of novel applications, such as fluidics, that extend beyond a mechanically rigid planar substrate material [23]–[25].

Die attach solutions currently involve using metals and organic materials as intermediates between the ceramic and the semiconductor die. Die attach and contact metals are points of failure in high temperature operation where their thermal mismatch can cause lift off. The motivation of this work is to use oxide materials to coat the surface of the LTCC for direct CVD film growth, eliminating the die attach process by a direct growth on the ceramic. The benefit of this would be a higher thermal stability of the attaching layer compared to metals and organics, along with removing the size and shape limitations associated with the attaching substrate. Oxide materials have the added benefit of being readily deposited by solution at room temperature with melting points <1000 °C. In this work Plasma Enhanced Chemical Vapour Deposition (PECVD) and solution processed silicon, zinc and aluminum oxides were used to enable low temperature crystalline films to be deposited on LTCC substrates. The surface characteristics of the oxide buffer and the PECVD films are characterized using X-ray and electron microscopy/spectroscopy techniques. The electronic properties of the LTCC/ZnO/GaN structure are tested by attempting to fabricate a Schottky diode structure on a deposited thin film.

2. Materials

2.1 III-V Nitride Semiconductors

One of the fundamental challenges of heteroepitaxy of III-N semiconductors comes from their crystal structure. All group IV elemental (Si, Ge) semiconductors and non-nitride group III-V materials have a cubic zincblende (ZB) structure, while the most stable phase of the III-Nitrides is hexagonal wurtzite (WZ). Figure 3 shows the relationship between bandgap and lattice constant for many different semiconductors. All materials seen on the right-hand side of Figure 3 share a ZB structure whereas the left hand side shows the WZ structure of the nitride family. The bandgap of InN is typically given as 0.7-0.8 eV, which has been strongly debated over the last 20 years. The value of ~0.7 eV is accepted based on strong room temperature photoluminescence peaks, however this is debatably due too Mie resonance with metallic In clusters [26]. On the contrary, a larger bandgap (>1.5 eV) has been shown to be strongly dependent on oxygen content [27]. Recent work in the Lakehead semiconductor research lab in conjunction with the Canadian Light Source (CLS) at the University of Saskatchewan has demonstrated a bandgap of ~1.8 eV through X-ray absorption/emission spectra to directly probe the band structure of different InN samples of varying morphologies [28].

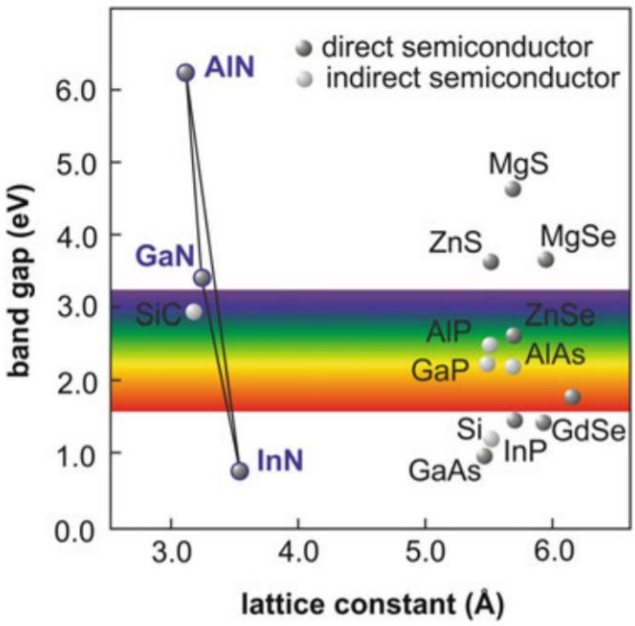

Figure 3: Bandgap and lattice constant of many common semiconductors [29].

Although significant research on their cubic structures has been performed since it can be grown metastably on cubic substrates such as (100) GaAs, more mismatch exists on cubic templates than with existing hexagonal systems and it has proved challenging to avoid hexagonal inclusions in the metastable cubic structure. Motivation in this field stems from several advantages of the cubic system due too the additional crystal symmetry , such as the lack of polarization fields, increased carrier mobilities, and lower dopant activation energies [30]–[32].

While both WZ and ZB structures share a tetrahedral unit cell due too the sp^3 hybrid bond shape they differ in how these unit cells stack. As seen in Figure 4, a ZB structure (left) will have an AaBbCc ordering along the [111] crystal direction, while the WZ crystal (right) has an AaBb order along to [0001] direction where A and a represent the cation (positive species) and anion (negative species) respectively. The difference in the stable structure comes from the ionicity of the bond III- N, where electrostatic attraction between III-N dipoles makes alignment along the c-axis more favorable (dotted lines in Figure 4).

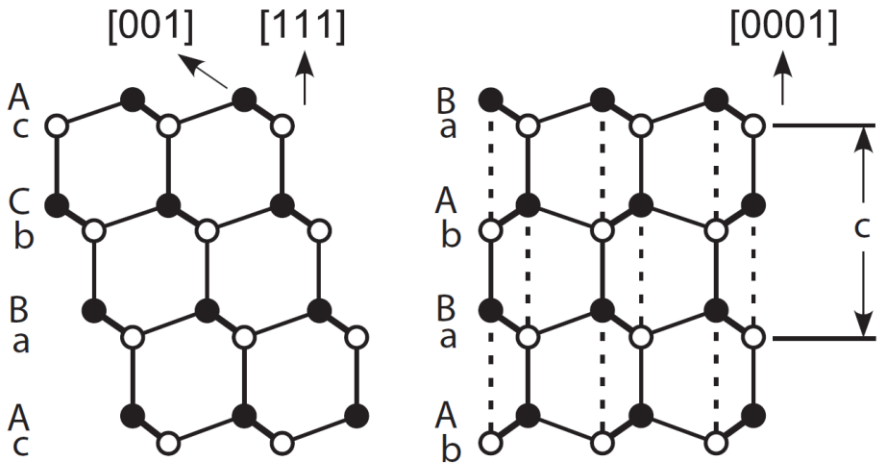

Figure 4: ZB structure (left) with AaBbCc ordering along the [111] crystal direction. The WZ crystal (right) with AaBb stacking along the [0001] direction [33].

This attraction is relatively weak and can be overcome by depositing these materials on cubic templates. The wurtzite (WZ) structure does not have complete charge symmetry, due too the alignment of the bonds along the c-axis. This induces a spontaneous (P_{sp}) and piezoelectric (P_z) polarization effect in the crystal, which are both aligned either into or away from the (0001) surface along the c-axis depending on the stacking order (cation to anion AaBb, or vice versa, aAbB). Piezoelectric polarization induces a voltage on the c-axis of the crystal as a restoring force in response to strain in the crystal along that direction, whereas spontaneous polarization comes from the charge difference between the Ga and N in the crystal.

The direction of the polarization is determined by the substrate material, with the ordering being continued from the substrate into the nitride. Since III-Nitrides are usually grown on sapphire or (111) silicon, both of which have no polarization, the polarity is determined by the nitridation process. Epitaxy begins in both cases by depositing a thin interface layer of AlN to minimize lattice mismatch with the substrate and avoid Ga diffusion [34]. The growth conditions during this phase will dictate the polarity of all subsequent epilayers, with two possibilities seen in Figure 5 [35], [36]. Ga facing surfaces have triple co-ordinated gallium facing the surface and are generally found to be smoother than N facing surfaces. In Ga-facing surfaces the polarization vector is pointing up from the surface, while surfaces ending with triple co-ordinated nitrogen will be the opposite.

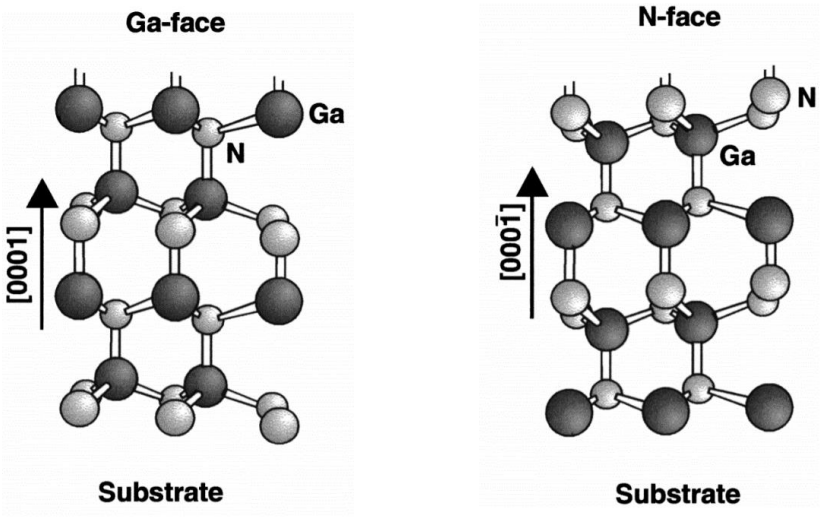

Figure 5: Two possible stacking orders in III-Nitrides that lead to polarization facing the substrate (left) and facing the surface (right). The magnitude of the spontaneous (P_{sp}) and piezoelectric (P_z) polarization is the same, but the direction is opposite [37].

The direction of this vector is useful in the polarization engineering of nitride structures, where charge accumulation can occur without doping and independent of temperature. From Gauss' law $\left(\rho = \nabla \cdot \left(P_{sp} + P_z\right)\right)$, a charge density (ρ) will appear due to changes in polarization, such as in heterojunctions, and will generate a bound charge at the surface as illustrated in Figure 6.

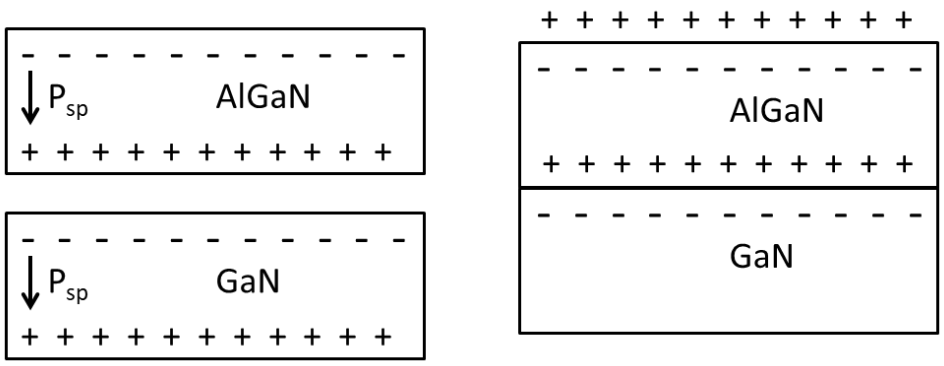

Figure 6: High electron mobility channel formation from spontaneous polarization vectors in a Ga facing GaN/AlGaN heterostructure. The Ga facing crystal has P_{sp} facing the surface while N facing crystal has it facing the substrate.

This effect can be desirable such as in the case of electron channel accumulation in high electron mobility transistors (HEMTs). High electron sheet densities (>10^{13} cm^{-2}) can be achieved without introducing donor dopant materials in the barrier layers that act as ionized scattering centres, degrading channel mobility. These channels are localized to the interface and can be well modelled by a triangular quantum in the device band structure [38]. This same polarization effect can also be detrimental, biasing quantum well structures in the well known quantum confined stark effect (QCSE). Polarization works separates holes and electrons in quantum well structures, thereby causing a reduction in the overlap of their wavefunctions and reduces recombination efficiency. Since the dipoles face along the c-axis in the wurtzite structure, the effects of polarization depend on the degree of c-axis orientation to the surface. shows how the degree of piezoelectric polarization changes between from the c, r, and m planes in GaN.

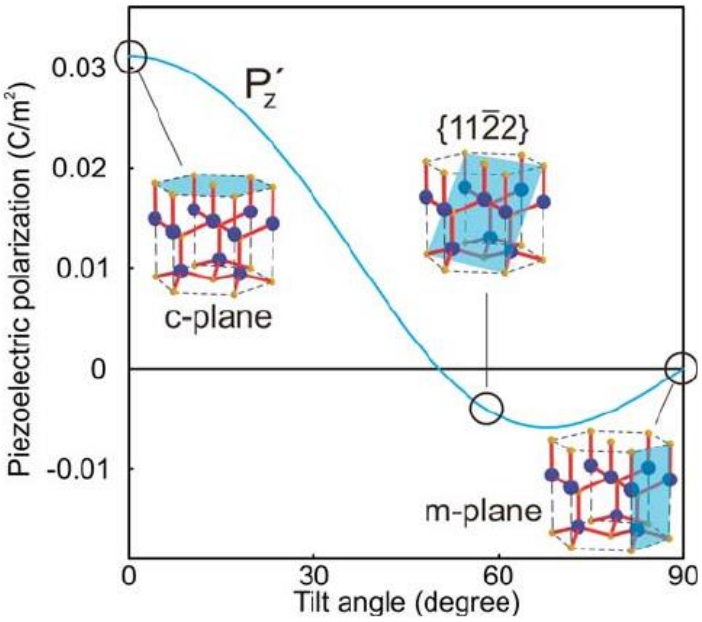

Figure 7: Change in piezoelectric polarization constant between from the c, r and m planes in GaN [39].

Polarization effects are useful in nitride-based sensors since they are not induced by ionized dopants or significantly dependant on the bandgap and are therefore stable over a wide range of

temperatures. The electron density at the GaN surface in is however dependant on the positive charges induced on the upper surface of the AlGaN for charge neutrality, therefore any source of negative charge on the surface will deplete the charge density in the buried AlGaN-GaN interface. Transistors based on these junctions are typically passivated for device stability, but a wide range of sensors operate by functionalizing this surface to selectively supply negative charges [40]–[43].

The piezoelectric polarization can also be utilized to measure mechanical strain. Changes in the strain state of the upper AlGaN layer will either reduce or enhance the channel carrier density depending on direction of the strain. This reverse effect can be used in nanogenerator structures, where paired with a rectifying junction, can produce nanoscale direct current generators [44]. The polarization coefficients are relatively independent of temperature, however internal strain created by mismatch can affect charge accumulation and tends to increase with temperature. In lattice matched structures the high temperature stability of nitrides makes them valuable for high temperature sensor design [45].

2.2 Oxide Materials

The choice of oxides to coat LTCC comes from the composition of the ceramics themselves. To form a good bond with the substrate, a component oxide is desirable, which will easily bond into the glass network. Three oxide materials were chosen as buffers, silicon dioxide deposited through spin coating, alumina deposited by anodization of metallic aluminum and zinc oxide deposited through dip coating.

2.2.1 Zinc Oxide

ZnO is a group II-VI semiconductor with many similar properties to GaN. As in the III-N, the ionicity of the bonding gives rise to the WZ crystal structure as the most stable phase. ZnO itself has been the subject of a significant amount of research owing too its wide energy bandgap

(3.437 eV [33]) allocating it many of the advantages associated with a large bandgap such as high temperature and high-power operation, low noise generation, and high breakdown voltage.

The relatively close size of the zinc/gallium atoms and oxygen/nitrogen atoms gives ZnO a closely sized crystal lattice to GaN. Similar to the III-N system, bandgap engineering is possible by alloying. This is typically done with MgO and BeO for larger bandgap alloys and CdO for lower bandgaps, although a full compositional range is not possible due too the cubic rocksalt structure of MgO and CdO [46].

Table 2: Unit cell properties of silicon, nitrides, and various oxide materials

Material	**Lattice constant (Å)**	
	a-axis	**c-axis**
InN [47]	3.537	5.703
GaN [47]	3.189	5.185
AlN [47]	3.110	4.980
ZnO [48]	3.249	5.205
CdO [48]	4.689	-
MgO [48]	4.216	-
BeO [49]	2.718	4.409
Al_2O_3 [50]	4.765	12.982
Si [50]	5.431	-

The hexagonal shape of the ZnO crystal introduces similar challenges as seen in III-Nitride materials. Heteroepitaxy on substrates such as sapphire produce large lattice mismatches (18.4%) resulting in similar densities of threading dislocations on the surface (10^{-7} – 10^{-9} cm^{-2}).

Metal oxides such as ZnO, SiO_2 and Al_2O_3 can uniquely produced in chemical solution using the sol-gel technique. Sol-gel relies on hydrolysis and condensation reactions to exchange alkyl ligands on the metal with bridging oxygen atoms to produce metal oxide colloids at room temperature. Using this technique, oxide materials can be produced as nano scale particles in

solution and thin films can be applied using wet chemical deposition techniques such as dip coating and spray coating. These versatile techniques can apply these coatings to many organic and nonplanar substrates. The relatively high surface area of nanoparticles lowers sintering temperatures and dense crystalline films can be produced at temperatures <600 °C. Compared to other oxide deposition techniques such as sputtering, it is simpler and more flexible in the choice of substrates. Solution chemistry can be controlled to introduce dopants [51]–[53], and controlling nanoparticle morphology is also possible with a variety of shapes with crystalline structure demonstrated [54]–[57].

The relative ease at which oxides can be wet etched compared to nitrides makes chemical wet etching highly selective in a III-Nitride/ZnO structure. Several reports of wet etching of ZnO have shown that a variety of acids including dilute mixtures of hydrochloric acid [58], [59] can etch ZnO at rates of 120 nm/min at 0.25%, increasing linearly with concentration [60]. The reported etch rates in this case are for RF sputtered layers, therefore even higher rates can be expected in sol-gel produced layers due too the increased porosity. This however may be a disadvantage in this work since wet cleaning processes for contact preparation can be destructive on the ZnO buffer.

A lack of reliable p-type doping of ZnO has been its most significant drawback to commercial device production. ZnO is normally found to be n-type because interstitial donor states from Zn (Zn_i) and O vacancies (V_O) are the most stable point defects [61], as well as unintentional hydrogen donor incorporation from the growth process [62]. The low formation energies of these defects tends to lead to high background electron concentrations in grown layers. The ability to easily produce highly n-type ZnO and its wide bandgap make it an attractive alternative to ITO as a transparent conductive oxide (TCO), but limits its application in homojunction structures [63].

The general strategy in choosing a p-type dopant is a substitutional group IA element on a zinc site, codoping of donors and acceptors, or substitution of group VA elements on an oxygen site. The main issues that are usually encountered are the long-term stability of the p-type dopant, the activation energy required and its solubility.

2.2.1.1 Zinc Contamination

While ZnO has a high melting temperature of 1,975 °C [64], in vacuum conditions the direct sublimation of ZnO to Zn and O gas is known to occur at temperatures as low as 700 °C [65]. Zinc and zinc containing alloys such as brass are avoided in vacuum technology due too the high vapour pressure of zinc, causing sublimation at low temperatures which can coat the reactor interior. Figure 8 shows the Θ-2Θ X-ray diffraction (XRD) results of a single crystal sapphire wafer heated in the contaminated system. Peaks at 42.01˚ and 91.00˚ are expected from the sapphire wafer, while all other are re-evaporated metal from the contaminant in the system.

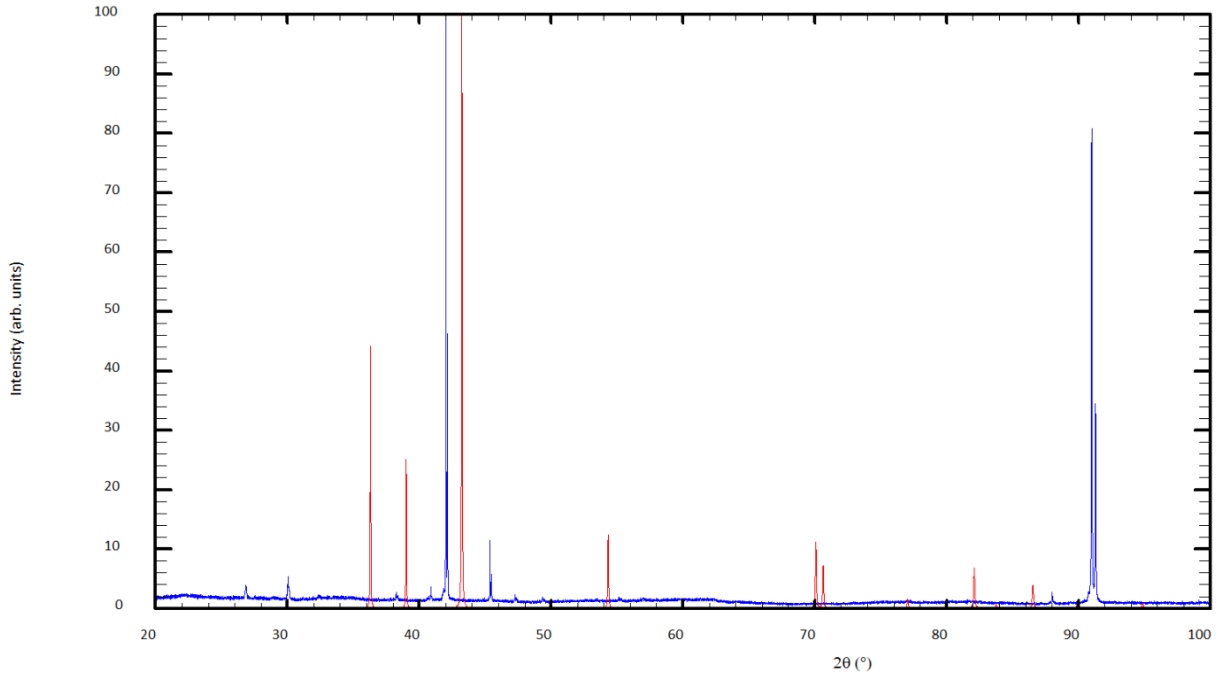

Figure 8: Normalized Θ-2Θ XRD plot of the sapphire wafer after ZnO contamination (blue). A theoretical spectrum from Zn metal (red) is included, calculated from the HCP structure with a=2.6648 Å and c=4.9467 Å [66]. Major peaks related to the (0006) and (00012) peaks of sapphire (blue) are at 42.01˚ and 91.00˚ respectively. All other peaks in blue correspond to reactor contamination.

The contamination appeared on all subsequent growths and drastically reduced the quality of the epitaxial layers. In our system we found the temperature limit to be 650 °C, depositing GaN at 700 °C and a pressure of 1400 mTorr resulted in the characteristic peaks in Figure 8 (blue) on all samples. This is indicative of a deposition from the reactor walls, which could likely be a zinc contamination, however a comparison of the contaminated sapphire and the HCP zinc structure in Figure 8 shows the contaminant does not match the XRD pattern of pure zinc metal and were only found to present after heating ZnO samples in vacuum. A mechanical cleaning of the system was required to remove it. The exact nature of the contaminants is unclear, but regardless it sets a limit on the temperatures used in the ZnO experiments at 650 °C.

2.2.2 Silicon Oxide

Sol-gel SiO_2 (or spin-on glass) has been used as insulating passivation layers, optical waveguides, a precursor to doped silica nanoparticles and has been used to produce several novel products such as Aero/Xero gels [67]–[70]. For LTCC it has been demonstrated as a planarization layer and a low cost planar optical waveguides [71], [72]. A hybrid sol-gel approach has been demonstrated as effective in reducing cracking by applying a mixture of silica nanoparticles with the coating solution to increase the volume fraction of silica in the drying solution, thus lowering shrinkage and strain in the layer. These layers did not demonstrate cracking even as thicknesses >1 μm were deposited and baked at 500 °C for 1hr. Samples used in this work were prepared by partners at TU-Ilmenau using the methods outlined in [72].

2.2.3 Anodized Alumina (AAO)

Alumina is the non-crystalline version of sapphire, which is normally used in nitride growth, and is a large constituent of many ceramic mixtures. It can be produced through the anodic oxidation of metallic aluminum at room temperature. This process is used in many industrial

applications where the oxide material serves as a productive coating on the relatively soft metal. The structure of the produced film depends on the acid used as an electrolyte in the process and is the result of a balance between oxide dissolution at the acid-oxide interface and production of new alumina at the metal-oxide interface.

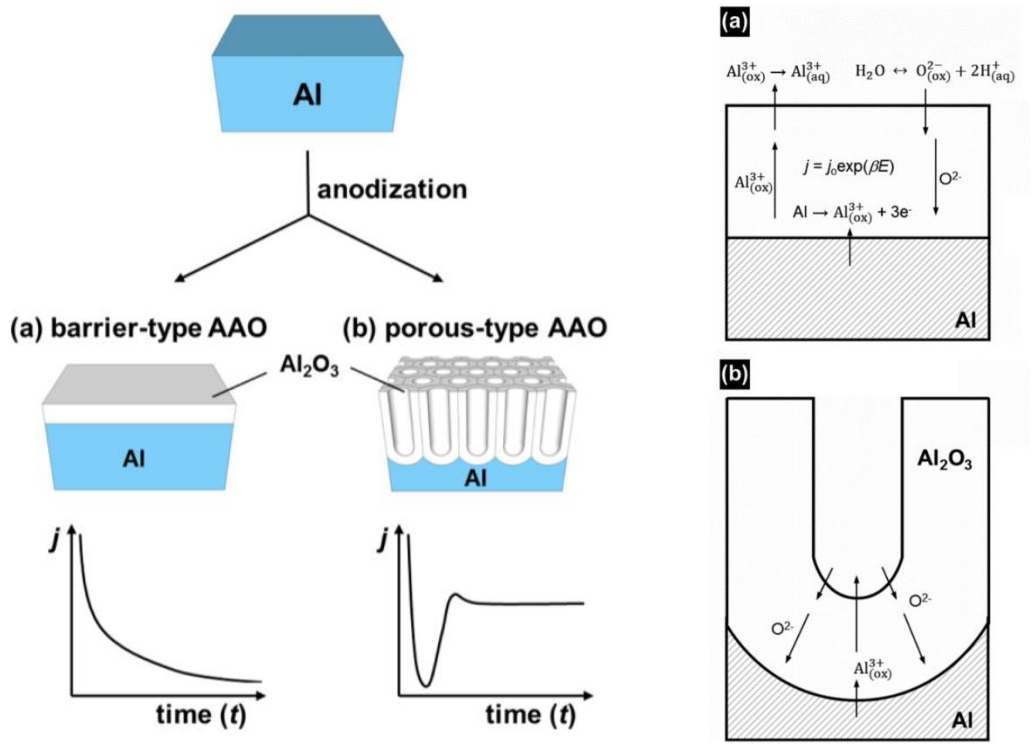

Figure 9: Anodized alumina production for a) low pH electrolytes resulting in a self-limiting barrier type and b) high pH resulting in a continuous pore etching or porous type material [73].

For weakly acidic solutions (pH 5-7) the oxide anodization current will quickly drop as the barrier becomes thick, as the field driven oxidation decays exponentially with thickness. The produced oxide is insoluble in these solutions so the process self limits and the oxide production will essentially go to zero at a thickness dependant on the applied voltage.

In low pH (<5) solutions the anodization will initially generate an oxide layer, however upon reaching a critical thickness (the minima in the anodization current in Figure 9b), random

stress fractures will occur in the oxide due too the large volume difference between aluminum and its oxide. This may also occur in weakly acidic solution if the thickness is too high but is undesirable in a protective coating. The fracture sites allow the oxidation to continue at the aluminum-oxide interface and the anodization current increases as the pores are created. Once the pore formation begins the volume expansion of the metal to oxide transition cause a mutual stress between adjacent pores and will help align them. The pore production can continue in the high field region at the bottom of the pore and thick, well aligned porous arrays can be produced from metal films at constant anodization current. This is done in a two-step process where an initial random pore array is allowed to reach steady state and removed, leaving a well aligned, dimpled template for a second anodization [73].

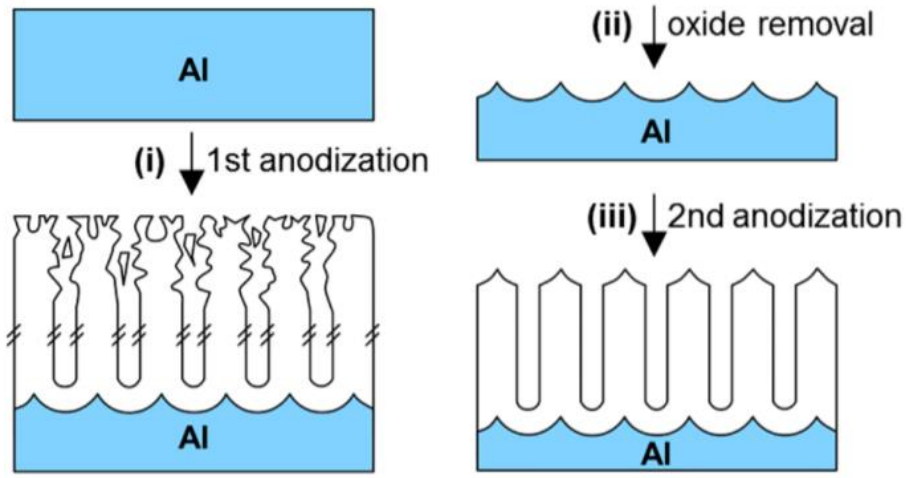

Figure 10: Two stage AAO template showing the initial random pore initiation and the dimpled template for the second anodization [73].

The pore structure can be controlled through the pH value of the electrolyte, which mainly defines the pore radius and the applied voltage, which controls the interpore distance. The lower the pH value of the solution, the smaller the pore and the higher the applied voltage the larger the interpore distance. It has been empirically found that in order to maintain an ordered array the porosity should be approximately 10% [74]. It is proposed that any interpore distance and size is

possible, so long as this 10% rule is obeyed the mutual interpore stress maintains order. Attempts to use the well ordered arrays in research have been as low cost, large area alternatives to lithographic patterning [75]–[77], templates for plasmonics and metamaterials [78]–[80], and templates for high aspect ratio nanorods [81]–[83].

A common experimental setup seen is 0.3 M oxalic acid ($H_2C_2O_4$) solution and constant DC voltage of 40 V. The pore structure reported in these conditions varies based on the exact experimental conditions such as temperature and purity of the aluminum used, but using these values we can expect a pore diameter on the order of 30 nm and a spacing of 100 nm [74], [78], [84]–[87]. Given the stable nature of alumina, no oxygen contamination from the layer was observed in the experiments. The onset of glass vitrification in the ceramics therefore sets the temperature limit for the entire process [88]. The limiting temperature in this work using AAO/Heratape CT700 was determined to be 700 °C by observed rounding of edges at >700 °C.

2.3 Cofired Ceramics

The application of ceramics in electronics dates to the 1950's where it was realized that ceramic processing techniques combined with screen printed conductors could not only significantly miniaturize circuit technology, but also integrate passive components in a durable monolithic structure suitable for mass production [89]. They posed several advantages over FRx organic circuit boards in applications where heat, environmental chemistry or dielectric loss is too high for reliable operation. They can be roughly divided into two major categories, high and low temperature cofired (HTCC and LTCC respectively), depending on the temperature used in the

final sintering process in the ceramic production. A typical ceramic production process can be seen in Figure 11.

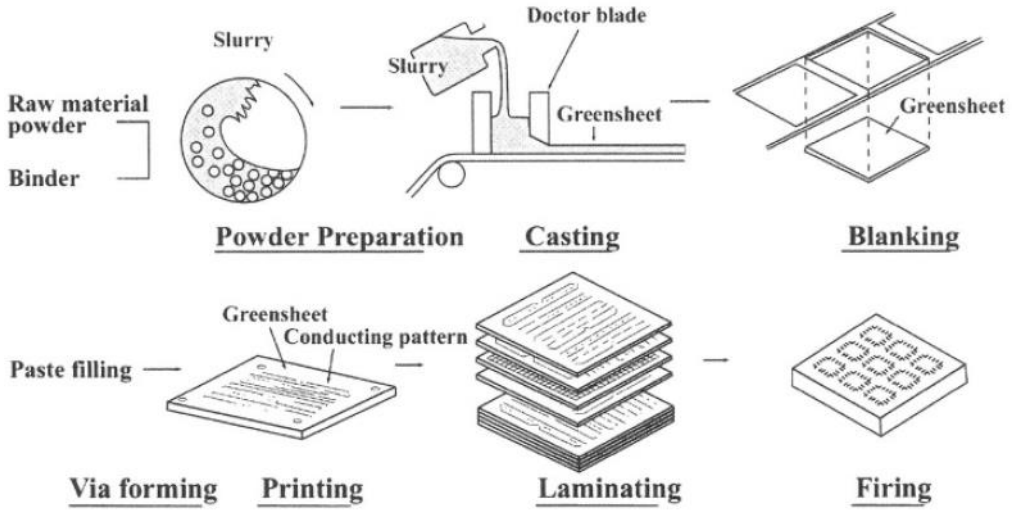

Figure 11: LTCC production flow diagram from initial slurry mixture to a final laminated multilayer stack [90].

The slurry is a mixture of oxide particles of representing the final composition of the sintered ceramic, with the addition of an organic binder, solvent, and plasticizers. For LTCC most of these oxides are a mixture of silica (SiO_2) and alumina (Al_2O_3) with differing amounts of modifier oxides (B_2O_3, PbO, Na_2O, CaO, BaO, ZnO, Li_2O). The mixture is designed to change various parameters of the ceramic, such as melting point, thermal conductivity/expansion, and dielectric loss by introducing mobile/non-mobile ionic species and non-bridging oxides in the silica-alumina amorphous network. LTCC and HTCC differ in that HTCC ceramics are least 96% alumina.

The layers are processed on a continuous reel poured from the slurry, shaped by a doctor blade, and prebaked to remove solvents. The green (pre-fired) paper-like ceramics are cast on mylar reels and patterned using laser and micromachining processes. Via holes can be formed either by punching or laser machining of the substrate to diameters as low as 150 μm [91], reaching

as low as 30 μm in current research and trace widths as narrow as 20 μm [92]. These features are filled with metallic frit paste by screen printing that bonds to the ceramic on firing, allowing for strong adhesion to the surface. Surface passives such as thick film resistors can be tested prior to final lamination and trimmed for high accuracy (+/- 2%). Much of this processing can be done in parallel with high volume, allowing for low cost with fine features. The final sintered thickness of the layers can be anywhere from 100 μm to 200 μm in thickness with as many as 30 layers [93].

The temperature of the final firing limits the materials used for conductors in these substrates. Since the highest conductivity metals have melting points below 1000 °C, processing temperatures are typically limited to 900 °C at the risk of deforming embedded line structures.

Table 3: Melting point of various conductors used in ceramic technology [90].

Material	Electrical Resistance (μΩ·cm)	Melting Point (°C)
Cu	1.7	1083
Au	2.3	1063
Ag	1.6	960
Pd	10.3	1552
Pt	10.6	1769
Ni	6.9	1455
W	5.5	3410
Mo	5.8	2610

For HTCC the solution is to use high conductivity refractory metals (W, Mo) as conductors. Since the signal delay and resistive power loss is proportional to the wire resistance, there is significant motivation to use higher conductivity metals (Au, Ag, Cu), and LTCC substrates are preferred in most applications.

Vacuum deposition of crystalline materials on LTCC surfaces has been limited primarily to RF sputtering, where many materials such as $Pb(ZrTi)O_3$ (PZT) , ZnO [94], and AlN [95]–[98] have been demonstrated. Sputtering has the added advantage of supplying kinetic energy to the depositing material through the plasma in the sputtering process rather than substrate heating. This allows for crystalline deposition at relatively low substrate temperatures. Crystalline orientation in these films is desired for applications as heat spreading dielectrics, electroacoustic devices, and epitaxial templates. In each of these applications it is more favorable to have a smooth, highly oriented substrate to improve performance.

2.3.1 Ceramic Applications

Beyond its application as a multilayer interconnect structure, LTCC can be shaped and processed into unique Microelectromechanical systems (MEMS). MEMS has predominantly been done using Silicon as a mechanical material because it has a long history in microelectronics where a library of fabrication techniques have been developed along with well documented material properties. It is well adapted to produce structures such as cantilevers and dense interdigitated combs on the order a single micron or lower, which is greatly beneficial in shrinking sensors and lowering their power consumption. Scaling of some devices this small may not be beneficial to their use or cost effective. This is true when considering devices focusing on power generation, millimeter and micrometer RF, chemical synthesis, and fluidics where larger surface areas may be needed. Silicon may also chemically reactive with fluids used microfluidic applications and has significant expense related to the fabrication and production technology needed to produce submicron scale features, making it suitable only in large volumes.

An example of an application where silicon may not be applicable is seen in Figure 12, where two coils are shown from a multilayer coil structure used in a microgenerator built from

LTCC. In their work 28 coils were fabricated on a 50 mm disc using 2, 8, 10 and 12-layer designs with 200 µm linewidths. Their best results (8 layer design) generated 589.91 mW at 11827 rpm [99]. To fabricate this device using silicon would be significantly more expensive not only due too the large area of crystalline material needed, but more complicated patterning and bonding techniques would be needed.

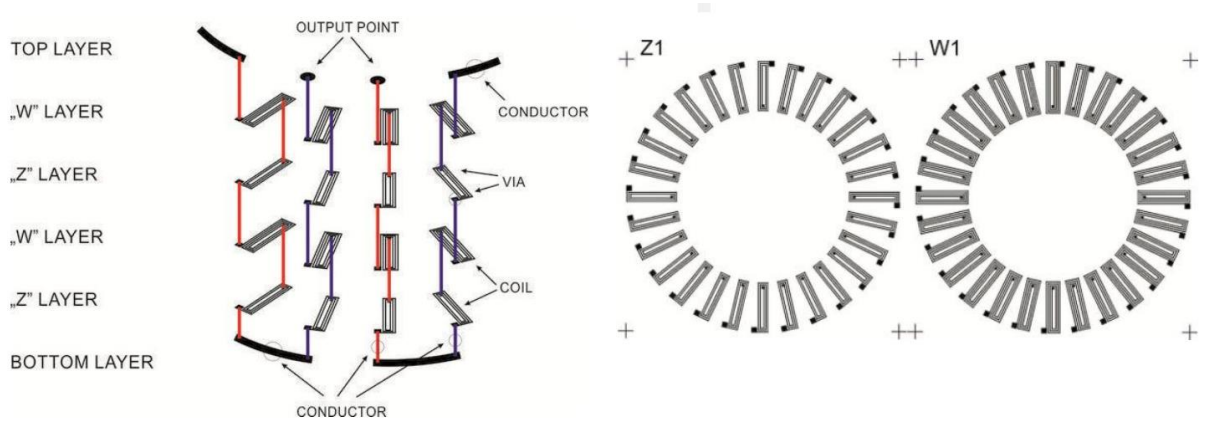

Figure 12: 2 coils from a 28-coil structure using in an LTCC micro generator device fabricated at Wrocław University of Technology. The linewidths shown are 200 µm with up to 12 layers laminated in a single 50 mm diameter disc [99].

LTCC has also been used as a MEMS material in a variety of microfluidic applications. The integration of microfluidic channels in a planar device can be done using graphitic sacrificial fill materials that are fully decomposed upon final lamination, leaving a hollow cavity within the sintered structure. A recent article showing several examples of microfluidic devices can be seen in [100], where 3D serpentine paths and passive hydrodynamic structures are fabricated from multilayer ceramic processing techniques. The channels can be designed using CAD software to produce novel fluidic mixer and filter elements. These paths can be located very close, and even sandwiched between embedded heaters/sensors along their path.

3. Applications

In this chapter the operation of the Schottky diode will be discussed as well as the effects of high temperature operation with an emphasis on the fundamental limits that are faced by silicon. The Schottky junction is a fundamental device that used in many different diodes and transistors, and the ability to fabricate and characterize these junctions is critical in understanding device performance.

Section 3.1 will cover the Schottky diode using band theory to describe the current voltage characteristics of the device. This model can be used to explain carrier transport through the barrier and how device parameters such as threshold voltage and leakage current can be affected by surface states. Temperature has significant effects on the current voltage characteristics of all electronic devices due too its effect on the fermi level in materials. This can lead to changes in important device parameters such as series resistance and junction capacitance, covered in section 3.2. Diffusion of point defects and dislocation movement can occur at elevated temperatures leading to irreversible changes in device properties. Diffusion can also occur at metal-semiconductor and metal-oxide junctions leading to contact failures. Permanent failure modes caused by thermal expansion mismatch are a major contribution to device failure at high temperatures. Section 3.3 briefly covers device packaging with ceramic substrates used in thermally robust package design.

3.1. Schottky Diode

The simplest device that could be fabricated using the LTCC/GaN system an n-GaN Schottky diode. A lateral diode structure is achievable using two different metal contacts on the surface of the GaN. The formation of back contacts through the LTCC itself can be fabricated

during the green tape stage of its processing. A vertical device is generally more desirable since vertical devices can utilize their entire surface, scaling of drift regions does not change the surface area of the device, and the ohmic contact can be internally connected in the LTCC stack.

A Schottky diode consists of an ohmic and rectifying metal semiconductor junction. The device acts analogously to a p-n junction diode. When the metal contact and the semiconductor are brought into electrical contact a built-in field arises from the diffusion of electrons across the metal-semiconductor junction, which may then form the rectifying energy barrier. The height of this barrier is determined by the electron affinity of the semiconductor and the metal work function as seen in Figure 13. Thermodynamic equilibrium establishes a constant Fermi level (E_f) through the device.

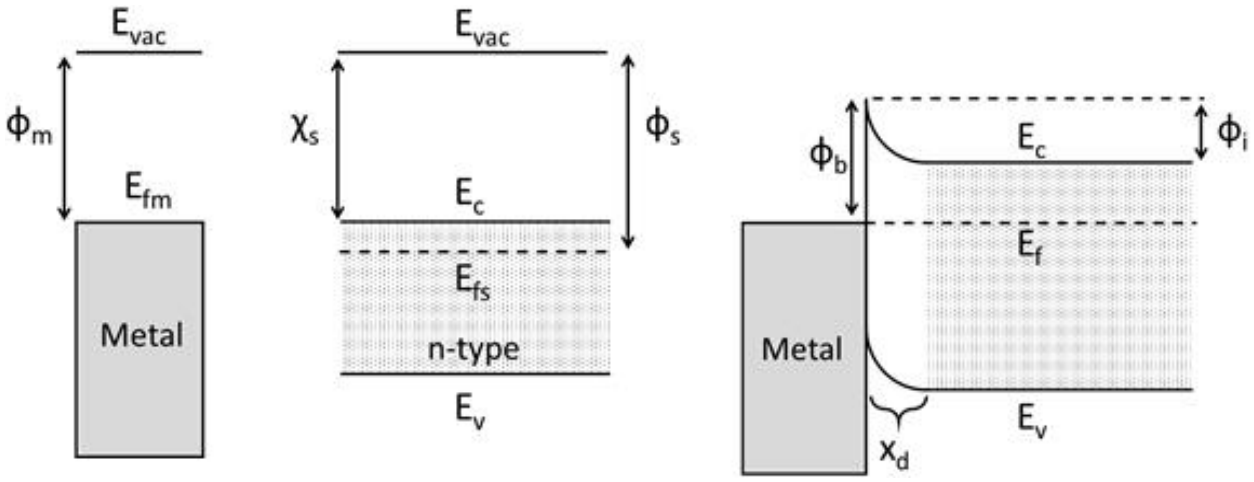

Figure 13: Energy levels in two isolated metal and n-type semiconductor materials and after contact with electron diffusion.

The built-in potential ($q\phi_i$) from the alignment of the Fermi levels can be expressed as the difference in the two work functions of the materials:

$$q\phi_i = q(\phi_m - \phi_s) \tag{3-1}$$

The energy barrier at the interface (ϕ_B) can be determined by the difference between the work function energy in the metal and the Fermi level of the semiconductor:

$$\phi_B = \phi_m - \chi_s \tag{3-2}$$

Where q is the electron charge constant, ϕ_m is the work function of the metal, ϕ_s is the semiconductor work function and χ_s is the semiconductor electron affinity ($\chi_{GaN} = 4.1$ eV) [2]. From Figure 13 this can be rewritten in term of the conduction band (E_c) and the Fermi level (E_f).

$$\chi_s = \phi_s + \left(E_c - E_{fs}\right) \tag{3-3}$$

Combining equations (3-1), (3-2) and (3-3)

$$\phi_B = \phi_m - \phi_s + (E_{fs} - E_c)$$

$$\phi_B = \phi_i + (E_{fs} - E_c) \tag{3-4}$$

To demonstrate rectification this barrier energy (ϕ_B) must > 0, which is accomplished by choosing a metal contact with a higher work function higher than GaN ($\phi_m > \phi_s$). If a lower work function metal is chosen, electrons will diffuse from the metal into the semiconductor, accumulating at the interface and the contact will be ohmic. Some examples of Schottky metal contacts used are Au ($\phi_{Au} = 5.1\ eV$), Pd ($\phi_{Pd} = 5.12\ eV$), Ni ($\phi_{Ni} = 5.15\ eV$) and Pt ($\phi_{Pt} = 5.65\ eV$) [101], whereas a common ohmic contact metal Ti ($\phi_{Ti} = 4.33\ eV$) or Al ($\phi_{Al} = 4.28\ eV$) [102].

A high work function metal is desired for Schottky contacts to increase ϕ_B and a low work function metal is ideal for ohmic contacts. A metal stack is often used to decrease undesirable effects such as intermetal diffusion which can result in non conducting alloys (Au-Al purple plague), and oxidation where non conducting oxides can be produced (Al-O). A common ohmic metal stack for GaN is Ti/Al/W/Au, where the Au cap removes the possibility of oxidation of Al, and W provides a diffusion barrier against the Al-Au [103]. Titanium contacts the GaN surface and upon annealing, causes nitrogen to diffuse into the metal, creating TiN near the interface and nitrogen vacancies in the GaN. Nitrogen vacancies are known shallow electron donors and pin the

Fermi level near the surface, thinning the energy barrier on the surface so it acts as a tunnel junction, while the Al limits this diffusion to only the Ti layer. Variations of this may change metals within the stack, but their purpose is the same. Though less thermally stable and oxidation resistant, a significantly simpler ohmic contact can be formed from an indium dot which shows ohmic behavior with no annealing necessary [104]. The contact resistance can be lowered from a 300 °C anneal, attributed to a thin InN interfacial layer [105].

When the two materials are initially in contact the concentration gradient drives diffusion currents to equalize the Fermi levels, and a field is built up from the positive charges left over from the electron removal in the semiconductor. The built-in field opposes the diffusion current and continues to grow until an equilibrium is reached. When a positive voltage is applied to the metal (V_a) with respect to the semiconductor in the diode structure, the built-in field is compensated. As the voltage is increased from zero, the barrier height seen for the electrons in the semiconductor will continue to decrease. When $V_a = \phi_i$ the flat band condition is reached and there is no barrier to electrons from the semiconductor to the metal, diffusion current can continue, and macroscopic current can be observed through the diode. When a positive voltage is applied to the semiconductor (reverse bias voltage V_r) the built-in field is enhanced, and no current can flow. This blocked is ideally effective we reach the critical field value for GaN (3.0 MV/cm) where impact ionization and avalanche breakdown can occur. These two scenarios can be seen in Figure 14.

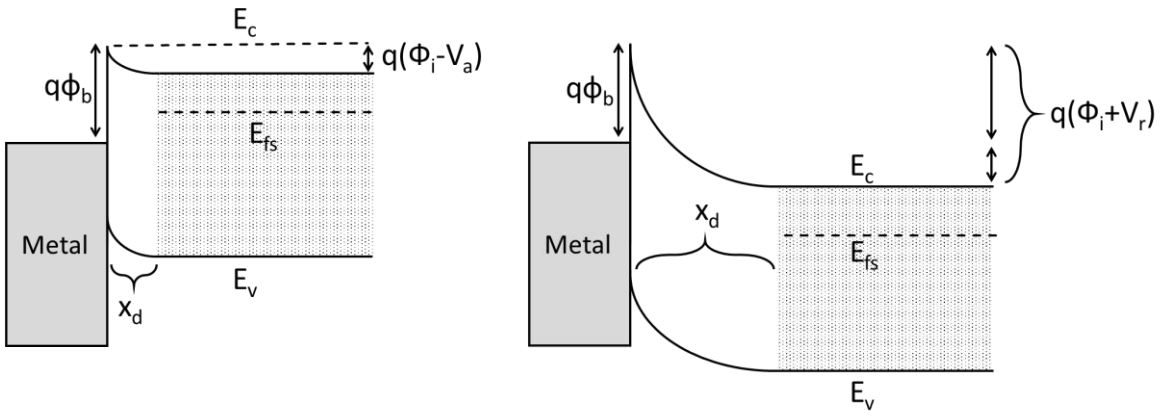

Figure 14: Band diagrams of the Schottky junction in forward (left) and reverse (right) bias. In forward bias the barrier shrinks, and the fermi level slowly returns to its isolated position. Once $V_a = \phi_i$ we return the isolated material scenario seen in Figure 13 (right) and the diffusion current is free to flow. In the reverse bias the applied voltage V_a is the same direction as the built-in potential ϕ_i and only adds to the current blocking field, depleting more carriers from the surface and extending the depletion region. Only carriers with enough energy to jump the barrier (ϕ_b) and thermally/optically generated currents can flow.

An idealized diode with a series resistance (R_s) can be modelled using the Shockley diode equation.

$$I = I_s\left(e^{\left(\frac{q(V-IR_s)}{nkT}\right)} - 1\right) \tag{3-5}$$

$$I_s = SA^{**}T^2 e^{-\left(\frac{q\phi_B}{kT}\right)}$$

$$A^{**} = \frac{4\pi m^* k^2 q}{h^3}$$

Where k is the Boltzmann constant, T is the temperature, n is the diode ideality factor, S is contact area, A^{**} is the effective Richardson constant (24 A cm^{-2} K^{-2} assuming $m^* = 0.2m_e$ [106]) and ϕ_B is the potential barrier and the junction. This equation assumes that all the current is from thermionic emission (TE) over the barrier, but in the case of high carrier concentrations there may be additional components due too tunneling through the barrier or tunneling itself may be the dominant transport mechanism in the extreme cases of high doping or high temperature.

3.1.1 Surface States

Surface states in semiconductors can differ from the bulk due too the free bonds at a surface and the minimizing of their energy. The minimization can introduce states in the bandgap, oxides can often grow due too ambient exposure, point defects such as vacancies can be present, dislocations can reach the open surface and terminate, and contaminant atoms such as carbon can be present. Each of these can introduce interface states that can dominate the interface properties, effectively pinning the Fermi level near the surface.

The effect of the surface states can be reduced by a post deposition annealing of the contacts on an oxygen environment. For Ni and Ni/Au contacts a post deposition annealing performed 500 °C for 10 mins can allow for effective passivation of states by diffusion of Ni into the interface, significantly reducing the reverse leakage current [107]. The Au capping is helpful in preventing the formation of NiO on the surface of the contact but annealing should be kept below 600 °C where Ni-Ga formation occurs and a possible migration of the gold contact to the surface occurs, replacing the nickel [108].

3.1.2. Thermionic Field Emission (TFE) and Field Emission (FE)

The Shockley diode equation assumes a thick enough barrier that tunneling through the barrier can be neglected. This is not the case when the depletion depth (x_d) is in the range of single nm thickness. The depletion depth can be found from:

$$x_d = \sqrt{\frac{2\epsilon_s \phi_B}{qN_D}} \tag{3-6}$$

As the doping density N_D becomes high the barrier becomes thin and less effective at blocking the tunneling of electrons at room temperature. High temperatures increase the tunneling current component as more electrons are thermally excited to regions where the barrier becomes

thin. More donor states may also become ionized, increasing N_D at higher temperatures. Eventually as temperature or donor concentration increases, the Shockley TE model cannot fit the forward or reverse current and a combination of field emission (tunneling) and thermally excited carrier must be considered. This is generally observed as a slower ramp of the current in the I-V curves (an increase in the measured ideality factor (n) to > 2). The Thermionic Field Emission (TFE) model is given by:

$$J = J_0\left(e^{\frac{q(V-IR_s)}{E_0}} - 1\right) \tag{3-7}$$

$$J_0 = \frac{A^{**}T\sqrt{\pi E_{00}q(\phi_b - V - \xi)}}{k\cosh\left(\frac{E_{00}}{kT}\right)}\, e^{\left(-\frac{q\xi}{kT}-\frac{q}{E_0}(\phi_b-\xi)\right)}$$

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right)$$

$$E_{00} = \left(\frac{qh}{4\pi}\right)\sqrt{\frac{N_D}{m^*\varepsilon_s}}$$

Where J represents current density (A/m), $q\xi$ is the energy difference between the Fermi level and the conduction band ($E_{fs} - E_c$), m^* is the effective mass of electrons (0.2m_e [106]) and ε_s is the electric permittivity (8.9 in GaN, 8.5 for AlN, 15.3 for InN [106]). For even higher donor concentrations (>10^{18}) the current can be dominated by the tunneling which can be approximated by [109]:

$$J = e^{\left(\frac{-q\phi_b}{E_{00}}\right)} \tag{3-8}$$

3.1.3 IV Curves

The analysis of a diode's performance is determined by examining its current-voltage (I-V) relationship on a graph. The ideal IV curve behaviour is given by the Shockley Diode equation

(3-5)) as previously covered with $n = 1$. A commonly used graphical analysis technique to determine the device parameters is outlined in [110]. Assuming the voltage drop across the diode $V_D > 3\frac{kT}{q}$ (reasonable given $\frac{kT}{q} = 0.025eV$) the ideal diode equation can be written as

$$I = I_s\left(e^{\left(\frac{q(V-IR_s)}{nkT}\right)}\right)$$

Rearranging and considering the current density $J = \frac{I}{A}$ and $\beta = \frac{kt}{q}$

$$V = R_sAJ + n\phi_b + \left(\frac{n}{\beta}\right)\ln\left(\frac{JA^{**}}{T^2}\right) \tag{3-9}$$

Differentiating this voltage with respect to the log current density gives

$$\frac{dV}{d(\ln(J))} = R_sAJ + \left(\frac{n}{\beta}\right) \tag{3-10}$$

A plot of $\frac{dV}{d(\ln(J))}$ vs J can then be used to determine the series resistance (R_s) from the slope of the linear regions and the ideality factor (n) from the y intercept. These values can be used to determine the barrier height (ϕ_b) from equation (3-9).

$$H(J) = V - \left(\frac{n}{\beta}\right)\ln\left(\frac{JA^{**}}{T^2}\right) = R_sAJ + n\phi_b \tag{3-11}$$

A plot of the function $H(J)$ vs J will have a y-intercept giving ϕ_b and the slope can be used to double check the consistency of the series resistance previously found.

3.2 High Temperature Materials

The wide bandgap and thermal stability of III-nitrides (particularly GaN and AlN) offers several advantages compared to silicon in terms of temperature, in addition to the relative chemical inertness and a resistance to ionizing radiation due too the strength of the III-nitride bond. The

fundamental thermal limit of silicon-based electronics comes from its background carrier concentration. At a given temperature any semiconductor material has a certain number of thermally excited carriers given by:

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_g}{2kT}} \tag{3-12}$$

Where E_g is the bandgap of the semiconductor (1.11 eV for Si), N_c is the density of conduction band states and N_v is the density of valence band states. As temperature is increased the number of background carriers is increased, which lowers the energy barriers in p-n junctions given by:

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_a N_d}{{n_i}^2}\right) \tag{3-13}$$

Here ϕ_B is the barrier height in eV, N_a is the acceptor doping level and N_d is the donor dopant levels typically given in cm^{-3}. Equations (3-12) and (3-13) show an inherent decrease of the bandgap due too background carrier which is unavoidable and not material specific. P-n junctions are often used for device isolation in silicon devices, and a reduction of the barrier results in signal leakage between devices. The increase in temperature will also minorly lower the bandgap due too the expansion of the lattice. This has been described through the Varshni expression through empirical fitting parameters α and β [1], [111], [112]:

$$E_g = E_{g0} - \frac{\alpha T^2}{(T + \beta)} \tag{3-14}$$

Table 4: Varshni parameters for several semiconducting materials.

Material	E_{g0} **(eV)**	α **(eV/K)**	β **(K)**
Si	1.17	4.73×10^{-4}	636
Ge	0.7437	4.77×10^{-4}	235
GaAs	1.519	5.41×10^{-4}	204
GaN	3.507	9.09×10^{-4}	830

AlN	6.230	1.799×10^{-3}	1462
InN	0.690	4.14×10^{-4}	454

These isolation junctions are critical to reliable device operation, and lowering energetic barriers causes an exponentially increasing leakage through them. Increased temperature also generates hotter carriers that can jump these lowered barriers, leading to increased thermionic emission (TE) current.

These effects limit bulk silicon device operation to around 150 °C [113], where thermally generated carriers are significant compared to doping levels and lowered barriers can increase junction leakage to the point of device failure. More advanced silicon technologies such as silicon on insulator (SOI) and silicon-germanium (SiGe) have been developed to address these limits in silicon. SOI and SiGe can alleviate the electrical isolation issues encountered with bulk silicon using buried oxides, trench isolation, and Si-Ge heterojunctions and are compatible with CMOS processing but devices are still limited to below 300 °C due too fundamental bandgap limitations in silicon [114]. Simpler designs such as junction free piezoresistive devices have been demonstrated up to 600 °C using SOI isolation technology [115].

It is clear from equations (3-13) and (3-14) the wide bandgap of nitride materials gives them better isolation than Si as temperature increases. Operation of nitride based transistors has been demonstrated at temperatures up to 1000 °C for short periods in vacuum for lattice matched InAlN/GaN devices [116]. Study of the failure mechanisms in these HEMT structures shows high temperature instabilities are related to stability of the Schottky contact metals. The thermal limits of various metals commonly used are reported to be 300 °C for Pd, 400 °C for Pt, 575 °C for Au and 600 °C for Ni [117]. Interfacial reactions with GaN can result in the diffusion of the contact

into the GaN structure, forming an ohmic junction such as with Au [118], of the diffusion of Ga into the metal contact as with Ni [119], [120]. To avoid undesirable diffusion effects, annealing is usually done in a rapid thermal annealing (RTA) oven for short periods [121].

3.3 Device Packaging

Die attach for LTCC includes metallization of the attaching die using a sputtering or electrochemical plating processes. Metallization of the LTCC is performed with screen printing of metal and glass frit mixtures. During firing the glass mixed with the metal can penetrate the metal and mechanically anchor it to the surface. Flip chip solutions can also be used with LTCC substrates where organic underfills add mechanical strength. Direct glass bonds with or without metal inclusions can also be employed with ceramic-silicon and ceramic-ceramic bonding due too the oxide nature of the substrate [122].

Bonding of the two metallized surfaces is done with eutectic metal solder alloys of lead, tin, bismuth, zinc, silicon, and germanium, however most of these alloy liquidus points are < 300 °C. Silver and gold can be alloyed to increase the liquidus point and thermal conductivity. Silver offers the best electrical conductivity of all materials and second-best thermal conductivity, along with lower cost than gold, so it is favored for high temperature and high-power applications [18], [114]. However even with high temperature alloys, such as 82Au-18In solders, the solidus point only reaches 488 °C [123].

A good die attach material has a melting point (solidus point for alloys) higher than the operating temperature, good thermal conductivity, low toxicity, thermal expansion comparable to the substrate and active die, and low thermomechanical fatigue. From a packaged device perspective, the contacts and the die attach metals are crucial aspects of reliability as the

temperature is increased [124]. A common thermal device failure occurs by lift off of the contacts and die attach, related to thermo-mechanical fatigue at their interfaces. The high conductivity metals used in LTCC (Cu, Ag, Al) as well as different solder alloys and many organic materials tend to have higher thermal expansion coefficients than crystalline materials and the difference generates shear stresses that can lead to cracking. Organic attach materials also have lower overall temperature limits compared to metals and glasses.

Device packaging for semiconductors serves as electrical, mechanical, and thermal interfaces, as well as providing environmental protection. For applications where extreme temperatures (-55 °C>T>300 °C) may be encountered, packaging becomes more of a challenge and many factors such as thermal expansion, thermal conductivity, melting points, and thermal fatigue become more important to device reliability. Thermal expansion difference between the substrate and die can results in delamination or cracking of the die as temperatures are increased. A list of different materials relevant to packaging can be seen in Table 5 [90], [125]–[127].

Table 5: Coefficient of Thermal Expansion (CTE) for several materials related to electronics and packaging [90], [125]–[127].

Metals	**CTE (10^6/°C)**	**Ceramics**	**CTE (10^6/°C)**	**Semiconductors**	**CTE (10^6/°C)**
304 stainless steel	17.8	AlN	4.3	GaAs	5.8
Ag	19.7	Alumina (96%)	6.4	Si	2.7
Al	23.5	Alumina (99%)	6.5	GaN (a-axis, 300K)	3.43
Alloy 42	4.9	BeO	7.8	AlN (a-axis, 300K)	4.35
Au	14.2	BN	3.7	InN (a-axis, 300K)	3.83

Cu	16.8	Fused Silica	0.56	ZnO (a-axis, 300K)	4.31
Invar	1.6	Quartz	13		
Kovar	5.5	SiC	3.8		
Mo	5.1	SiN	3		
Ni	13-15	LTCC	3.0-11.6		
63Sn-37Pb	25				
95Pb-5Sn	28				
Ti	10				
W	4.5				

Organics	**CTE (10^6/°C)**
Epoxy Resin	50-80
FR-4(x-y)	14.8
FR-4(z)	80-90
Polycarbonate	50-70
Polyimide Glass (x-y)	12-14
Polyimide Glass (z)	60
Polyimides	40-50
Polyurethanes	180-250
RTV	800

Mechanical failures may be prone to occur at higher temperatures due to die package melting and failure of die attach mechanisms due too differences in thermal expansion. Metallic contacts may also experience their own failure mechanisms due too diffusion into the device,

Kirkendall void generation, or unintentional alloying of metal contacts in the stack or the device itself.

Part of the motivation for this work is to avoid the die attach process, since it is a point of failure in high temperature operation due too the fact that most metals have high thermal expansion coefficients compared to crystalline materials and lower melting points. From this perspective it would be beneficial to have an inorganic material with a closer TCE match and higher melting point. Metal oxides fit this description however, they have lower thermal and electrical conductivity than metals and should be as thin as possible. Wet chemistry coating techniques such as dip coating can produce nanoscale thin films with crystalline quality and will be used in this work to apply oxide coatings on LTCC.

4. Deposition Technology

4.1 Dip Coating

The solution-based deposition can be applied in a variety of ways including spray coating, spin coating, dip coating, and even inkjet printing depending on the size, shape and thickness of the coated layer. Of these techniques, dip coating represents the oldest commercially applied process. It can be used with a large variety of solutions and non-planar geometries in a simple experimental setup. The process can be divided into three distinct steps:

1. An initial immersion and dwell in the sol-gel solution. The dwell time in this step allows for the solution to fully wet the surface and ensures the substrate and solution are the same temperature.
2. Withdraw at constant speed. The hydrodynamics of this stage determine the thickness of the final coating. There is a delicate balance between solution drainage, capillary pressure and solvent evaporation that determines the coating thickness.
3. Evaporation rate. The solvent and undesirable organic by-products can fully evaporate, leaving behind the metal oxide gel network on the surface of the substrate. This is usually done at elevated temperatures to ensure evaporation before subsequent coatings, however too high of a temperature will rapidly evaporate many by-products at once and disturb the layer.

These three steps are relatively easy to implement, as all that is needed is a solution bath and a mean of constant withdraw from the bath. The evaporation should take place in an open furnace to allow removal of vaporised organics.

A mathematical treatment of the process was first developed in 1965 by L. Landau and B. Levich in order to predict the thickness of photosensitive layers in film reel production (A republication of their work can be seen in [128]). In their work they showed that the thickness of the wet deposited layer (h_0) is dependant on the gravity induced drainage and viscous solution drag, which can be determined by the aptly named Landau-Levich equation:

$$h_0 = \left(\frac{\eta U_0}{\rho g}\right)^{\frac{1}{2}} \cdot f\left(\frac{\eta U_0}{\gamma}\right) \tag{4-1}$$

Where η is the liquid viscosity, γ is the liquid vapour surface tension, ρ is the liquid density, g is the gravitational constant and U_0 is the withdraw speed from the bath. The $\frac{\eta U_0}{\gamma}$ term is known as the capillary number and is used to describe the effect of surface tension on the layer thickness. If the capillary number is $< 10^{-2}$ we can consider $f\left(\frac{\eta U_0}{\gamma}\right) = c\left(\frac{\eta U_0}{\gamma}\right)^{\frac{1}{6}}$ where c is a solution dependant constant of ~ 0.9 that is found empirically. In this case we can consider [129]:

$$h_0 = c\frac{(\eta U_0)^{\frac{2}{3}}}{\gamma^{\frac{1}{6}}(\rho g)^{\frac{1}{2}}} \tag{4-2}$$

As the speed is further increase the viscous drag becomes much more significant than the surface tension and $f\left(\frac{\eta U_0}{\gamma}\right) \approx c$. In this case we consider:

$$h_0 = c\left(\frac{\eta U_0}{\rho g}\right)^{\frac{1}{2}} \tag{4-3}$$

Where c is typically found to be of ~ 0.8 [130]. The important thing to consider here is the power dependence of the layer thickness changes from $\frac{2}{3}$ to $\frac{1}{2}$ when the withdraw speed is high and

surface tension becomes less significant. The rest of the values can be considered constant process properties and can be lumped into a single constant D to give:

$$h_0 = DU_0^{\frac{2}{3}} \tag{4-4}$$

To relate this to the dried film thickness (h_f) an additional material dependant proportionality constant k can be included:

$$h_f = k\left(DU_0^{\frac{2}{3}}\right) \tag{4-5}$$

These results are valid only until very low withdraw rates where additional effects due to evaporation come into play. When the withdraw rate is very low the solvent may evaporate faster than it is withdrawn from the bath, resulting in capillary feeding towards the drying line on the substrate. In this case the thickness can be determined from [131]:

$$h_f = \left(\frac{CM}{\alpha\rho}\right)\frac{E}{LU_0} \tag{4-6}$$

Where C is the solute concentration, M is the molar mass, α is the volume fraction or porosity of the film, E is the evaporation rate and L is the width of the substrate. The material dependant parameters in equation 4-5 can again be grouped into a single constant k.

$$h_f = \frac{kE}{LU_0} \tag{4-7}$$

The combination of these two equations gives a full description of the dry film thickness.

$$h_f = k\left(\frac{E}{LU_0} + DU_0^{\frac{2}{3}}\right) \tag{4-8}$$

The film thickness vs. withdraw speed curve defined by equation 4-8 is characteristic of all dip coating experiments and a plot can be seen in Figure 15 [132].

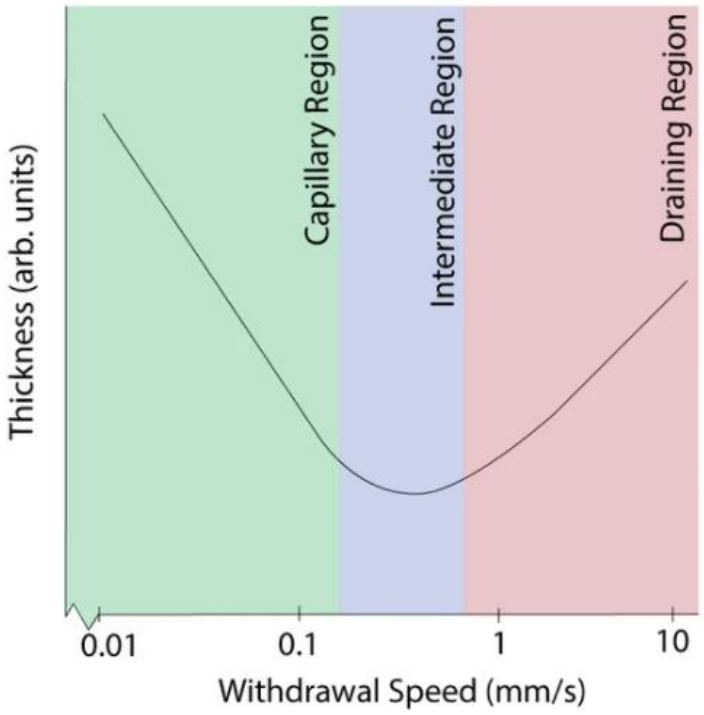

Figure 15: Film thickness vs withdrawal speed from the bath. The drainage and capillary region are comminated by different mechanisms [133].

This analysis only considers the steady state scenario where an infinite plate or continuous roll is withdrawn from a bath. One important consideration is the uniformity of the coatings across larger wafers. Surface tension will cause a curvature to arise at the edges of the film, causing a thinning of the film along edges parallel to the pull direction. Samples are also assumed to be at constant pull velocity, and therefore at initial acceleration of the samples out of the bath the viscous drag is lower than the steady state condition. Surface features large enough to disrupt the flow of draining solution can also cause additional solution to accumulate and cause and unwanted swelling of the film. Additional effects such as premature evaporation of the solvent can cause also cause variations in the thickness which may lead the undesirable sacrificial areas on the wafer.

4.1.2 Dip Coater

The dip coater used in this setup was designed in the lab for this application. In basic principle all that is needed to perform dip coating is a method to pull a sample from the liquid bath at a controlled rate. Within the last decade many advances in the field of 3D printing have emerged and now a low cost setup can be found for only a few hundred dollars. In fact, the dipping arm and case for the dop coater itself were printed using ABS in the one of the newly acquired makerspaces at Lakehead University. The wide adoption of 3D printing on a hobby level has driven cost down and a wide range of solutions exist for motor control. A basic overview of the dip coater design can be seen in Figure 16.

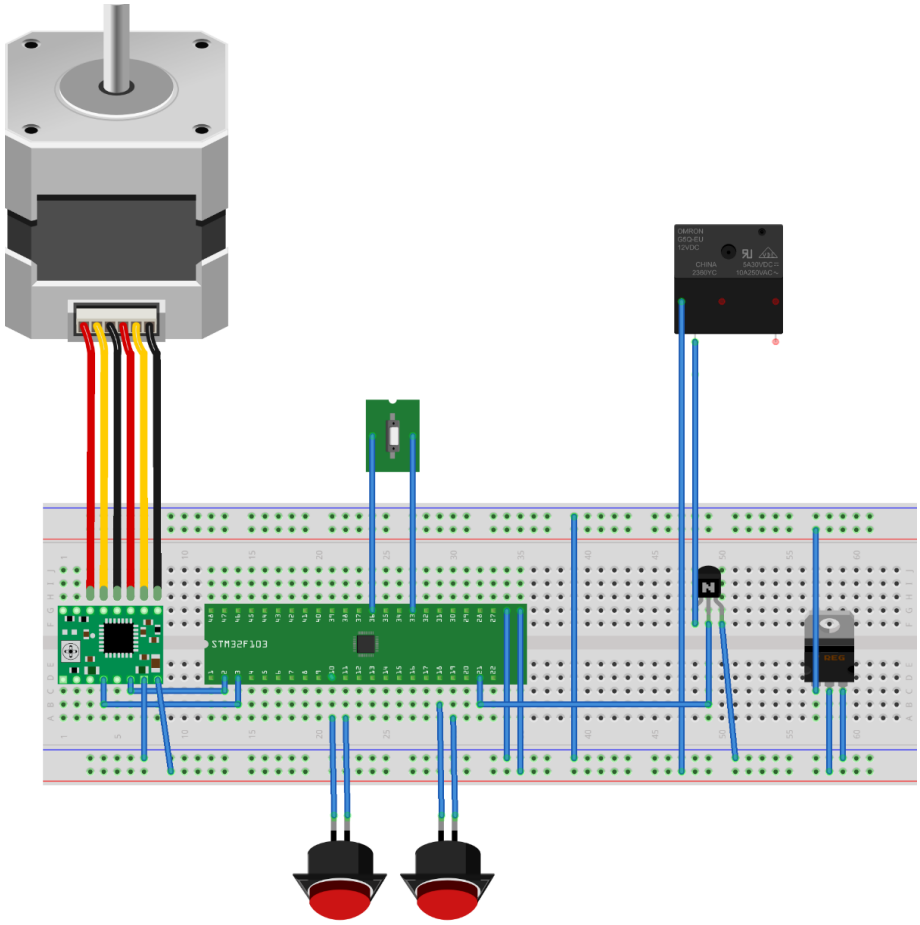

Figure 16: Basic schematic of dip coater.

The dip coater is controlled using STM32FC103 “blue pill” microcontroller, TMC2208 stepper drivers and a 30A logic level relay. With dip doating it is simple to integrate a heating element into the process that can achieve the temperatures required. The sample is lightly clipped the main arm of the dip coater, which rides two guide rails and the main 400 mm leadscrew. The stepper motor moves the sample fully into the bath (distance set by user push button) and fully withdraws it to the top end stop where the heater is located. In this design the heater is located above the bath so samples can be dipped and pulled into the heater without intervention.

While spin coating is a viable alternative and was explored, however the process requires a baking at temperatures upward of 300 °C every dip followed by a higher temperature anneal. The spin coater is already a closed system in order to prevent spraying of the spin off material and leaves no room to include a heating element in the setup. Spin coating would therefore require constant attention and manual handling of the sample every dip, which may introduce random errors between samples. The appeal of complete automation made dip coating the method of choice.

The heating power is controlled using an external Variac rated for 2HP, with temperature calibration performed using type a K thermocouple inserted bottom up into the heater. The board is supplied with 28V from a linear bench supply for the motors and an LM7805 provides a 5V rail for the logic. Two user inputs are possible, one for setting a predetermined dip depth and one for initiating the program. A limit switch is used to set the upper limit of the dip withdraw.

The stepper motor in Figure 16 coupled to a 400 mm long leadscrew (8mm pitch) and is controlled using 16 micro stepping. This gives a z-step resolution of $\frac{8}{16\times200} = 0.0025\,mm$. A typical withdraw speed used in these experiments ranges from 1-10 mm/s. A simple to use program

was made in the lab to control the dwell time, withdraw speed, number of dips, heating duration and the velocity profile of the sample after withdrawing from the bath.

Several iterations of design were performed on the dip coater by changing the heating element and modifying sample holder design to be reliable when heated to ~300 °C without cracking the sample or dropping it. Several heating elements were attempted including a commercial heat gun, Inconel stove elements, IR heating elements and nichrome wire. The layers were found to be extremely sensitive to ambient conditions and excessive air flow was found to lead to amorphous layers.

All dips were performed in the closed fume hood housed in the research lab. An open tube style furnace was found to give the best results with a nichrome coil providing radially uniform heating to the sample. The initial design and testing was performed on soda-lime glass slide samples using ZnO recipes derived from literature. The best results for this work were determined from XRD profiles and AFM scans.

4.2 Sol-Gel

Sol-gel is a relatively low-cost, powderless, wet chemical process for producing nano-scale metal oxides such as Al_2O_3, SiO_2, Yr_2O_3, and ZnO in solution. It is a two-step process wherein a metal alkoxide (a metal bonded to an alkyl group through oxygen) or metal salt is dissolved in water or a polar solvent (such as alcohols). Within the solvent the precursor undergoes hydrolysis and condensation to generate nanoparticles of metal oxides.

The wet chemical nature of the metal oxide nanoparticle solution gives large flexibility in how it can be further processed. Because the metal oxides are formed as colloids suspended in the solution, they can be applied through coating methods such as spin coating, dip coating or spray

coating for thin, uniform layers. This is attractive as it avoids the use vacuum systems, has a low thermal budget, is cost effective and can easily be scaled to large areas and nonplanar surfaces.

The thermal requirements for the process are determined by the evaporation of organic additives and solvents from the final product, and in some cases a final sintering. The temperature required for these steps is lower than in VPE techniques since we are not required to break metal-oxide bonds, thus allowing a large flexibility in the choice of substrate from low melting point glasses and ceramics to organic polymers. A wide range of powders, fibres, films, and dense ceramic structures have been demonstrated by controlled solution chemistry.

There are several significant parameters that effect the final product of the sol-gel process [134]. These properties of the sol determine the layer thickness when dip coating through the liquid viscosity and its density. By controlling the amount of material deposited per dip in the process we determine the influence of particle-particle and particle substrate interactions in the layer formation, which in turn determine the crystallinity of the film upon annealing. The controlling factors include the nature of the precursor and its concentration, the used solvent and additive species used, the method of coating of substrates and its speed, the nature of the substrate, and heat treatment procedure. Each of these factors needs to be considered in the rational design of the coating solution and the process parameters used.

4.2.1 ZnO Sol Chemistry

For the sol-gel synthesis of ZnO the most common precursor used is Zinc Acetate Dihydrate (ZAD) ($Zn(CH_3CO_2)_2 \cdot 2H_2O$). ZAD is used because of its relatively high solubility in alcohols, additionally the acetate ions produced can act as chelating ligands in the gel formation process and acetic acid produced as a result of the hydrolysis can easily be removed by thermal

treatment [135]. Alternatives such as Zinc Nitrate Hexahydrate ($Zn(NO_3)_2 \cdot 6H_2O$) produce more difficult to remove anionic species [136].

The concentration of the zinc precursor used will influence the viscosity, density and the volume fraction of solvent which will remain after the preheating after every dip. The solubility of ZAD in alcoholic solutions depends on the dielectric constant of the alcohol and will therefore be more soluble in shorter chain alcohols. The most common alcohols in literature are methanol and 2-methoxyethanol. While the choice of solvent varies over published literature, in most cases it is a short chain alcohol. A list of alcohols commonly used can be seen in Table 6 [137].

Table 6: Various alcohols used in sol-gel ZnO synthesis [137].

Alcohol	**Formula**	**Dielectric constant**	**Boiling point (°C)**	**Viscosity (cp, 20(°C))**
Methanol	CH_3OH	32.6	64.7	0.55
Ethanol	CH_3CH_2OH	24.55	78	1.10
Propanol	$CH_3CH_2CH_2OH$	20.1	97	2.26
Butanol	$CH_3CH_2CH_2CH_2OH$	17.80	117.7	2.95
Methoxyethanol	$CH_3OCH_2CH_2OH$	16.90	124.5	1.72

The general trend is a longer alcohol chain leads to a lower dielectric constant, higher boiling points, and higher viscosity. For enhanced crystallinity in the deposited layers it is important that the disruption of the layer by the evaporation process is minimized, however a minimum temperature of 275°C is required to remove the acetate species from the layer [135]. Considering this, longer chain alcohols are beneficial because they will evaporate at a slower rate and maintain crystalline ordering.

A review of ZnO sol-gel chemistry by Znadi [134] shows two primary clusters that lead to the formation of ZnO upon condensation. One is the zinc oxo-acetato species $ZnO_{1-x}(AcO)_{2x}$ which takes the form of Sierpiński pyramid clusters formed by $(Zn_4O)^{6+}$ tetrahedra with acetate serving as a bridging ligand on each edge [138].

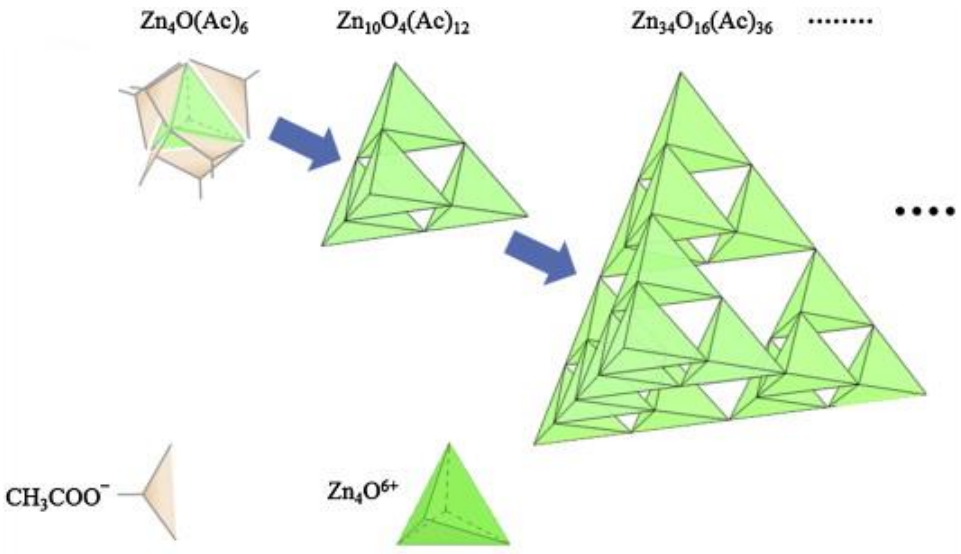

Figure 17: Zinc oxo-acetato species formed from the zinc salt in the sol-gel process. The Zn_4O clusters are charge balanced by accommodating an acetate ion on each external edge of the tetrahedra [139].

These are formed from initial salt by following reaction [140]:

$$4\ Zn(Ac)_2 \cdot 2\ H_2O \rightarrow Zn_4O(Ac)_6 + 7\ H_2O + 2\ HAc$$

These pyramids can further aggregate into larger structures with an increase in ageing time of the precursor solution, releasing zinc acetate:

$$4\ Zn_4O(Ac)_6 \rightarrow Zn_{10}O_4(Ac)_{12} + 6\ Zn(Ac)_2$$

The presence of these clusters has been used an explanation for an observed discrete blueshift in the UV absorption spectra of aging solutions, resulting from the quantum confinement within the nanoparticles.

The released water molecules lead to an $H_2O/OH-$ induced reorganization of these tetrahedral structures, resulting in a second primary cluster through these proposed routes [140]:

$$Zn_4O(Ac)_6 + Zn(Ac)_2 + 9\ H_2O \rightarrow Zn_5(OH)_8(Ac)_2(H_2O)_2 + 6\ HAc$$

$$Zn_{10}O_4(Ac)_{12} + 16\ H_2O \rightarrow 2\ Zn_5(OH)_8(Ac)_2(H_2O)_2 + 8\ HAc$$

$$Zn_{10}O_4(Ac)_{12} + 8\ H_2O + 8\ OH^- \rightarrow 2\ Zn_5(OH)_8(Ac)_2(H_2O)_2 + 8\ Ac^-$$

$Zn_5(OH)_8(Ac)_2(H_2O)_2$ is sometimes referred to as layered hydroxide zinc acetate (LHZA) or zinc double salt (ZDS) due too its sheet-like structure with zinc hydroxide octahedra layers intercalated with water and acetate ions. The rate of these production of the hydroxide species is presumed to be slow due too the low amount of water supplied by the ZAD [141].

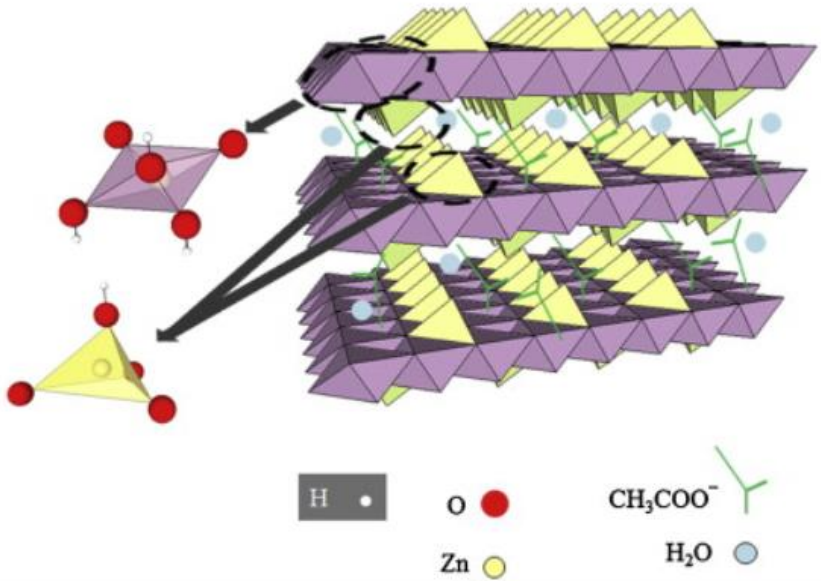

Figure 18: Layered hydroxide zinc acetate (LHZA) or zinc double salt seen in sol-gel zinc oxide synthesis [139].

Upon heating, the acetate and water evaporate leaving any hydroxide and oxide species behind. The hydroxide species present undergo condensation to form ZnO and water which is also then evaporated to leave the ZnO network.

The Sierpiński pyramid structures are more desirable for ZnO crystalline layers since the tetrahedral unit cell is already formed, lowering the energy required to form ZnO crystallites. The initial production these pyramid structures releases water into the solution, which inevitably contributes to the formation of the LHZA species. In the interest of growing dense, crystalline films additional water should therefore be avoided and care should be taken to remove water from experiment. Samples were always subjected to a bakeout prior to their initial dip and solution baths were dried in vacuum after cleaning to help remove water from the surface.

4.2.1.1 Stabilizing Agents

Due too the low solubility of ZAD in an alcohol solution, a stabilizing agent is usually added to the sol gel mixture. These stabilizers can form complexes with the dissolved zinc and acetate ions, significantly increasing the solubility in the non-polar alcohol used as a solvent.

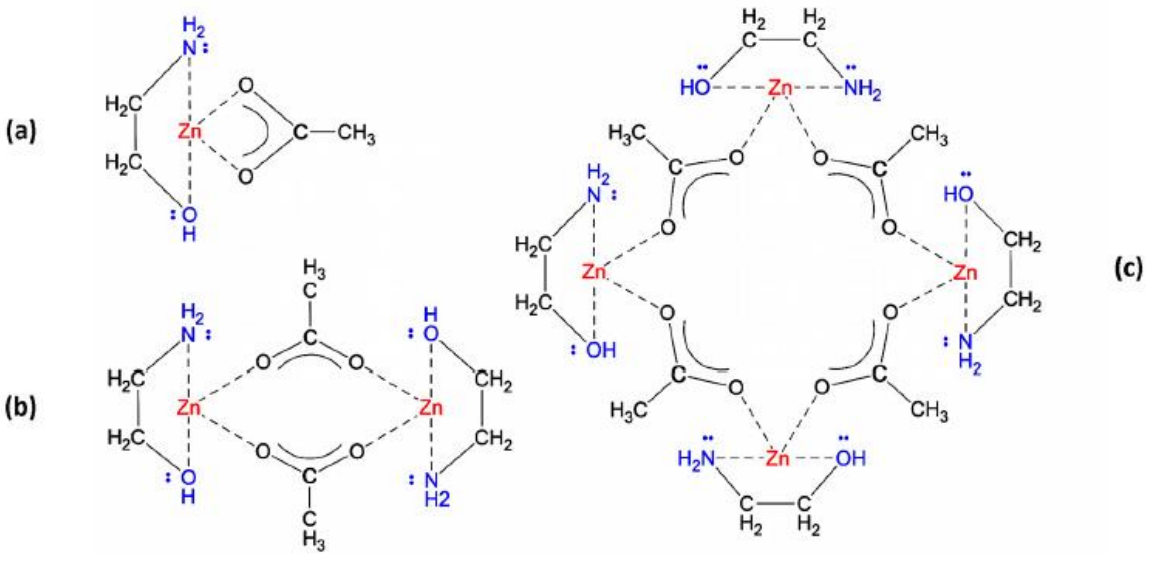

Figure 19: The proposed stabilized complexes formed from Monoethanolamine (MEA) stabilized ZAD. The a) monomer structure b) dimer and c) tetramer all increase the solubility of ZAD in nonpolar solvents [135].

Several different stabilizing agents have been explored in literature to determine which have the greatest impact on the orientation of the films [139].

Table 7: Stabilizing agents examined for their impact on crystal orientation in ZnO dip coated films [139].

Name (abbreviation)	Chemical formula	Boiling point (°C)	Density (g/ml)	Viscosity (mPa s, @25 °C)	pH
Monoethanolamine (MEA)	(CH_2CH_2OH)-NH_2	170	1.012	19.4	11.8
Diethanolamine (DEA)	$(CH_2CH_2OH)_2$-NH	271	1.097	351	11.5
Triethanolamine (TEA)	$(CH_2CH_2OH)_3$-N	335	1.124	592	11
Triethylamine (TeA)	$(CH_2CH_2)_3$-N	90	0.726	0.363	12.7
Ethylenediamine (EDA)	H_2N-(CH_2CH_2)-NH_2	118	0.899	1.8	11.9

TeA and MEA were shown to give the highest degree of c-axis orientation on glass substrates under identical dip conditions determined by XRD. MEA is commonly used as a stabilizing agent in literature [52], [142]–[144] for the growth of oriented films, since for many applications device performance improves with crystallinity. It can be used to increase the metal salt solubility, has relatively low viscosity as to not drastically increase layer thickness and boiling point high enough to not rapidly flash off and disrupt the layer. A 1:1 MEA:ZAD ratio was used the stabilizing agent based off literature review.

4.2.1.2 Doping

In the interest of increasing the conductivity for transparent conductive oxide (TCO) aluminum doped zinc oxide (AZO) has been a widely researched. The prospect of this work is

replacing the relatively expensive ITO contacts. The aluminum doping is typically a few % of the zinc concentration and acts as a donor species by substitution of Zn, where an extra electron on the Al 3s orbital is donated to Zn 4s conduction band states [145]. The relatively small size of the Al atom combined with the formation of $Al_2O_3/ZnAL_2O_4$ clusters leads too a decrease in the conductivity due too passivated donors and decreased mobility [146]. Literature review shows these species to form as low as 2% in sol-gel samples. Higher percentages (7.8% [147]) have been demonstrated with vacuum deposited layers. The high surface area of the sol-gel colloids likely makes the formation of these species easier in sol-gel samples.

Results from The X-ray diffraction (XRD) experiments performed on glass substrates can be seen in Figure 20.

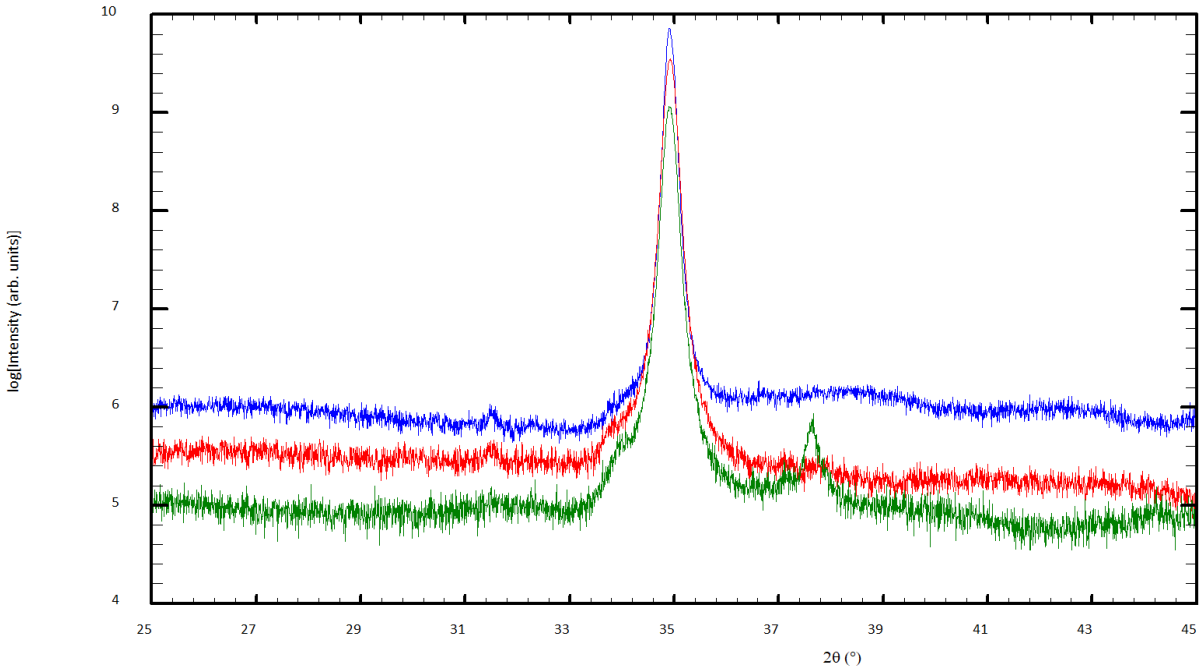

Figure 20: Semilog plot of XRD peaks in the range of 2Θ=25˚ to 45˚ for increasing Al content in the film. Each sample is 15 dips on a glass slide. The highest peak (blue) is 0% doping, next (red) is 0.5% and green is 1%.

From these experiments a decrease in the overall peak heights is observed as aluminum content increases, roughly an order of magnitude for 1.0% doping. A small peak in the semilog plot was observed at 37.4˚ which can be attributed to $(11\bar{2}0)$ Al_2O_3. The formation of this insulating oxide is undesirable and 1.0% aluminum doping was taken as the maximum doping level in this work.

4.2.1.3 Baking

The substrate melting point is important because it sets the upper limit for thermal process of both the ZnO films and further processed layers. In this work the upper limit is taken to be 650°C for ZnO from the observed decomposition under vacuum. The baking process in sol-gel is used to evaporate water, alcohol and organic by-products of the gel process. Insight into the dynamics of the baking process can be found using Thermogravimetric/Differential Thermal Analysis (TG-DTA) on dry samples. Results published in [135] can be seen in Figure 21.

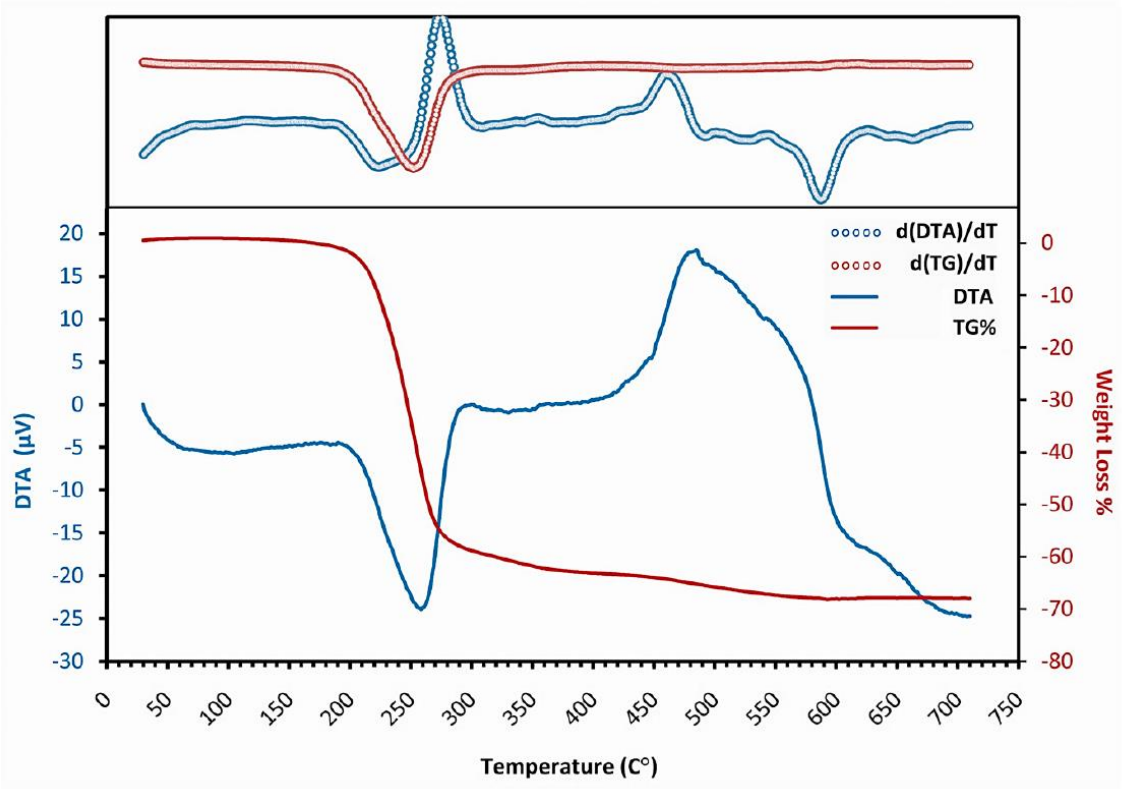

Figure 21: TG-DTA analysis of the baking process for ZAD sol-gel showing weight loss beginning at 275 °C [135].

The weight loss in these graphs corresponds to the vaporization of different component of the sol-gel film. These results were paired with FTIR in this work to identify which components where responsible for the weight loss. The results show a significant reduction of the carboxyl and amine related peaks at 275 °C. The endothermic peak around 430 °C was observed to be onset of Zn-O bond formation through the combined measurements. To minimize the disruption of the annealing and crystallization by the organic evaporation it is therefore important to separate these two processes as far apart in temperature as possible. The minimum bakeout temperature is therefore taken at 275 °C. The current through the heater coil was adjusted to reach a maximum of 275 °C on the calibration thermocouple.

4.2.1.3 Dip Rate

The dip rate refers to the rate that a sample is pulled from the solution bath and coated. It is not necessarily part of the chemistry, but once the solution is prepared it is the final control variable to change the thickness of deposited layer. As shown in Figure 15 there exists a cross over regime between the entrenching and draining dominated regimes where the minimum film thickness occurs. There are two effects that constrain the choice of dip rate:

1. High dip rates will deposit too much material at once. To achieve crystallinity in these films the deposited layer must have a homogenous nucleation on the previous layer. If the deposited layer is thicker than the average crystallite size nucleation may not occur on the previous layer but in the volume of layer (heterogeneous nucleation), causing porosity and a decrease in the relative texture of the XRD and an increase in surface roughness [135]. The minimum thermally stable diameter of ZnO is reported to be in the range of 60-70 nm [148]. The withdraw rate should not exceed values which deposit more than this per dip.

2. Too low of a deposition rate is inefficient at depositing material, but can also transition the deposition to the capillary regime (Figure 15) . The transition to this regime can increase the deposition rate, possibly introducing heterogenous nucleation. The so-called coffee-ring effect is also prevalent due too the high evaporation of the alcohol [149].

The optimal dip rate changes between experiments because of variation in the viscosity and density of the different alcohols/stabilizing agents. To determine the optimal dip rate, a fixed number of dips are tested at different withdraw rates. Beyond the optimum dip rate, the surface will roughen as it becomes polycrystalline and a decrease in the XRD FWHM will be seen.

4.3 Chemical Vapour Deposition (CVD)

The most common production methods for III-Nitrides are Hydride Vapour Phase Epitaxy (HVPE) Metal Organic Chemical Vapour Deposition (MOCVD). The vapour used in the reaction is a precursor to the deposited film, requiring elevated temperature to initiate a chemical reaction near the substrate surface and deposit the desired material. The thermal decomposition creates a concentration many orders of magnitude higher than the equilibrium vapour pressure of the material and drives a condensation on the surface of the substrate. The consumption of the near surface vapour phase precursor creates a diffusion current to grow the crystal, assuming the temperature is high enough completely decompose the precursors. Too low a temperature will be limited by the thermodynamics of precursor breakdown, known to have Arrhenius exponential dependence. The result is exponentially decreasing growth rates and an increase in surface roughness. Too high a temperature can also occur, where desorption of deposited material reduces the observed growth rate. In both techniques a stable window exists where the optimal growth

occurs. A typical growth rate curve bounded by these effects for GaN CVD can be seen in Figure 22.

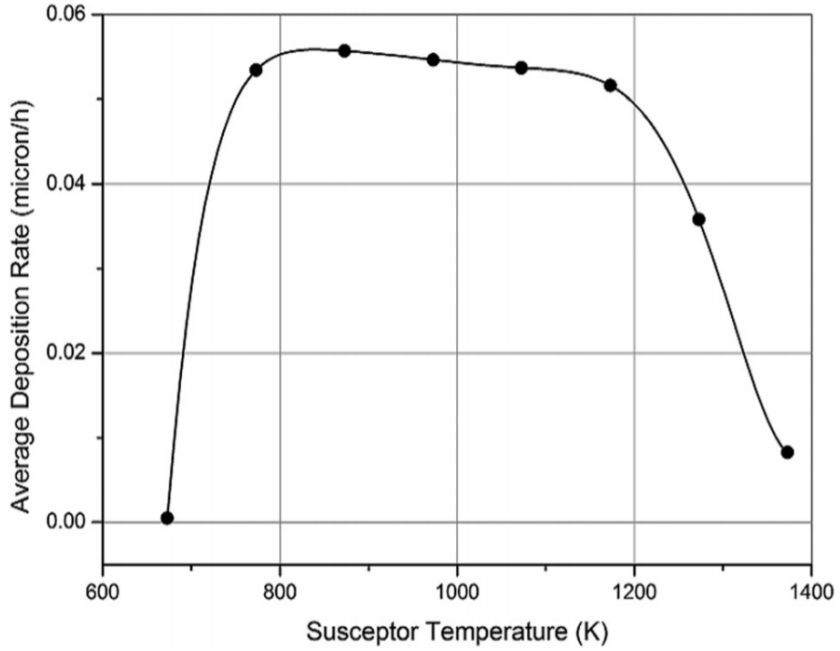

Figure 22: Growth rate curve showing three distinct deposition regimes. At low temperatures, the growth is limited by the precursor breakdown and at high temperatures decomposition and evaporation occurs. In between these two regimes the transport from the gas phase is diffusion limited, the growth rate is high and stable [150].

CVD and HVPE are preferred on a commercial scale for nitrides due to the relatively low vacuum conditions needed compared to Physical Vapour Deposition (PVD) techniques. In MBE and sputtering a long mean free path of gas atoms is needed to deposit on a substrate. Techniques which rely on vaporizing elemental sources and gas kinetics in this way require Ultra High Vacuums (UHV, $<10^{-8}$ Torr), making it more difficult to scale the reactor volume and more time is required to fully re-establish vacuums after maintenance. PVD techniques are also non conformal, the beam-like path of the precursor elements means they primarily coat in line of sight, giving higher anisotropy in their coverage. CVD does not require long free paths and is driven by temperature gradients near the surface, thus can be used to coat complex geometries and non line

of sight features. PVD is useful on research scale work since it can have lower impurity levels and lacks process by-products. The deep vacuums used allow for electron diffraction tools such as Reflection High Energy Electron Diffraction (RHEED) to be used in real time to monitor the growth dynamics.

HVPE is distinguished from other growth techniques due too the production of a hydride anion (H-) in the initial reaction of a metal precursor with hydrogen chloride. This produces metal chlorides which are transported downstream to a heated substrate and the substrate supersaturation occurs. The higher reactivity of the chlorine species vs. organic ligands which are used in metal organic CVD (MOCVD) allows for fast reaction kinetics to occur and significantly higher growth rates can be achieved. Given the additional hydride production that occurs in these systems and the fast deposition rates, it is difficult to create superlattice and multi quantum well structures used in LED and some transistors. HVPE is therefore largely applied for thick film growth or freestanding GaN growth since growth rates as high as 1800 μm/h are possible [151].

For device layers in III-Nitrides the most common technique is Metal Organic CVD (MOCVD), the lower deposition rate and abrupt control allows for thin quantum well structures. In MOCVD group III precursor is a triethyl- or trimethyl-(aluminum, gallium, indium) gas. The source of nitrogen for III-Nitride deposition is typically ammonia (NH_3), because the nitrogen molecule itself is very stable (N-H = 3.25 eV vs. N≡N = 9.80eV [152]) deposition with N_2 is not feasible. Other gas phase sources have been considered in research such as hydrazine (NH_2- NH_2), methylamines (NH_2-CH_3) and molecular single precursors such as dimethylgallium amide ($[(CH_3)_2GaNH_2]_3$), [153]–[155] that can directly deposit GaN, but ammonia remains by far the most common and well established choice.

Single crystal epitaxy of III-Nitrides has been successful with low alloying content AlGaN and InGaN for transistors and optoelectronic applications, with many products currently available from companies such as Cree [156], [157]. A typical device structure with MOCVD begins with a thin (20-30 nm) AlN interface layer on either (111) silicon or sapphire to produce a closer lattice match seed layer between the substrate and GaN. This is initiated with N_2 exposure at elevated temperatures [158] or at lower temperatures in plasma systems [159], [160] to produce a thin (~1 nm) interface layer. GaN growth then proceeds with low temperature (~550 °C) buffering structure which is then annealed at the growth temperature (~1050 °C). The low temperature growth induces the VW island like growth mode which grow along the angled $\{11\bar{2}2\}$ facets. The growth along this direct facilitates the bending of dislocations towards the growth surface so that upon coalescence they can annihilate one another. The annealing at above growth temperatures causes a redistribution of the surface atoms (both Ga and N) through evaporation and local redeposition on the surface [161]. This redistribution preferentially removes the high energy $\{11\bar{2}2\}$ facet to create larger islands faced with $\{0002\}$. A thick (1-3 μm) GaN layer can then be grown to reduce substrate effects in the active devices layer. Thicker layers can be grown on free standing GaN substrates to be used as drift layers in high power vertical devices, but wafer bowing limits thickness on sapphire and silicon.

The flow rates of the precursors are usually determined empirically from observing characteristics of the grown layers, such as surface roughness, photoluminescence spectra, X-ray diffraction spectra, carrier mobilities and growth rates. Since the decomposition of NH_3 is relatively small and the vapour pressure of nitrogen is high over the substrate, III/V ratios are typically on the order of 4000 to help lower nitrogen vacancies [162], significantly higher a ratio of 1-10 seen in GaAs growth [163].

A dual or two-flow system was pioneered in the early 90's by Nakamura while developing blue LED's while at Nichia [164]. These are cold walled systems where a main carrier gas subflow (H_2, N_2, Ar) is mixed with a reactant gas through a separate injection port, usually located above the substrates. A plasma source can be easily incorporated into this reactor design by placing an excitation chamber in series with the subflow. This could be an inductively coupled plasma (ICP) coil, a microwave cavity, or DC/RF capacitive plates.

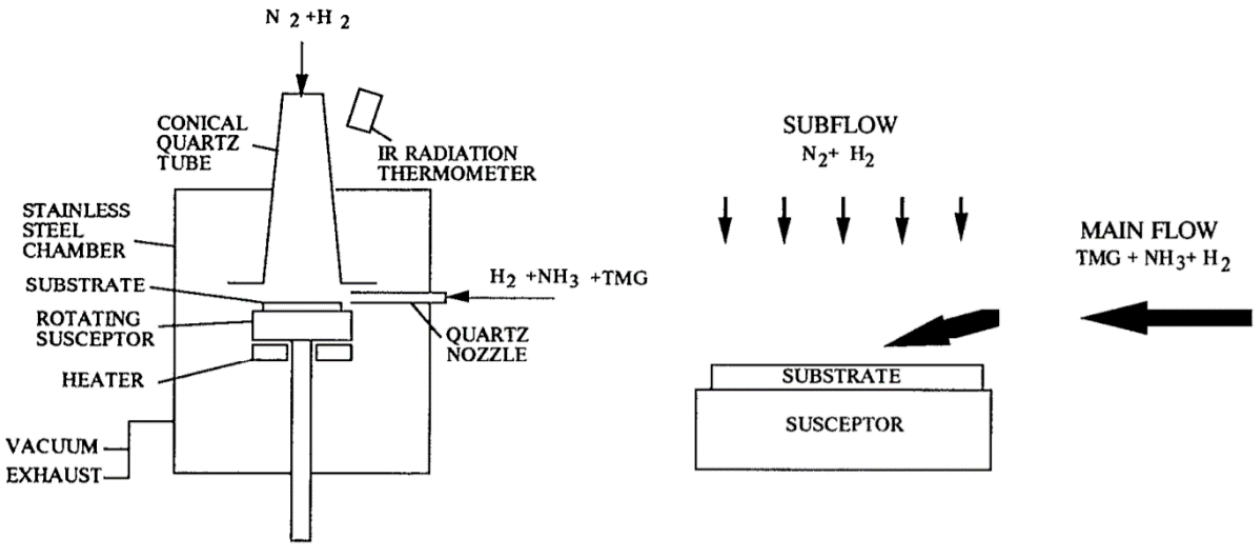

Figure 23: Basic dual flow system used in nitride epitaxy proposed in the early 90's [129].

Plasma sources have benefits over ammonia as a nitrogen source, where temperatures must be >600°C for efficient cracking of the molecule. The increased reactivity of the nitrogen species from plasma excitation is a benefit to its availability in thin film growth, however the presence of excited nitrogen species mixed with the group III precursors can lead to increased gas phase reactions, seen as a powder formation on the surface of the substrate. A surface powder can be removed by a simple scotch tape adhesion test or ultrasonic cleaning but may still introduce impurities in the layers. The addition of small amounts of hydrogen can help to decrease the

amount of carbon-nitrogen species evidenced by optical emission spectroscopy measurements [165], [166].

Another method to decrease the powder formation is alternating the injection of the precursors to eliminate overlap in the chamber. This technique is referred to as migration enhanced epitaxy (MEE) in MBE systems or flow modulated epitaxy (FME) when used with CVD [167]. The idea is the same in both cases, group V precursors tend have higher vapour pressures which leads to poor sticking of the atoms on the surface and desorption. III-V growth therefore tends to occur in group V rich conditions so that the surface is heavily bombarded with N/As/P during growth. In this case it is possible that a migrating Ga atom on the surface can recombine with a N atom on the surface before migrating to an appropriate edge or kink in the surface. Without sufficiently high temperature to increase migration distances this can lead to the so called Volmer-Weber (VW) island-like growth modes and rough surfaces of small grains. By separately injecting the precursors, the group III precursors can migrate further on the surface, stimulating island plus layer Stranski-Krastanov (SK) growth, where crystallites grow on the $\{11\bar{2}0\}$ facets to expand the monolayer (Figure 2). The increased migration allows for grains to expand two dimensionally on the surface and complete surface coverage before new layers are started.

Deposition in FME and MEE techniques occurs by repeating a series of short growth loops which can be tailored to control composition. The alternating injection also allows additional time for the group III precursors to migrate on the surface, since the formation of immobile nitride species cannot occur until the nitrogen injection phase of the growth loop. This has been experimentally demonstrated to increase the crystalline quality in deposited films [168]–[171]. An overview of the system used, and the gas control cabinet are given in Figure 24 and Figure 25.

FME and MEE are also closely related to Atomic Layer Epitaxy (ALE), where a saturation of the growth surface occurs during each growth cycle. This can be achieved by isolating the growth chamber during each precursor injection and purging the system after each injection. The temperatures used in this technique are intentionally low to avoid complete removal of the methyl groups on the group III precursor. This prevents additional precursors from coating the surface and self limits the growth to one layer. These techniques usually take place <500 °C since incomplete breakdown is necessary, and no surface migration is needed to complete the monolayer. The additional purge and isolation steps in the growth recipe combined with the upper limit of one monolayer per growth cycles give very low growth rates that are not suitable for device production. The highly conformal low temperature films are however very useful in thin quantum well structures, gate oxides and passivation layers in devices [9], [172], [173].

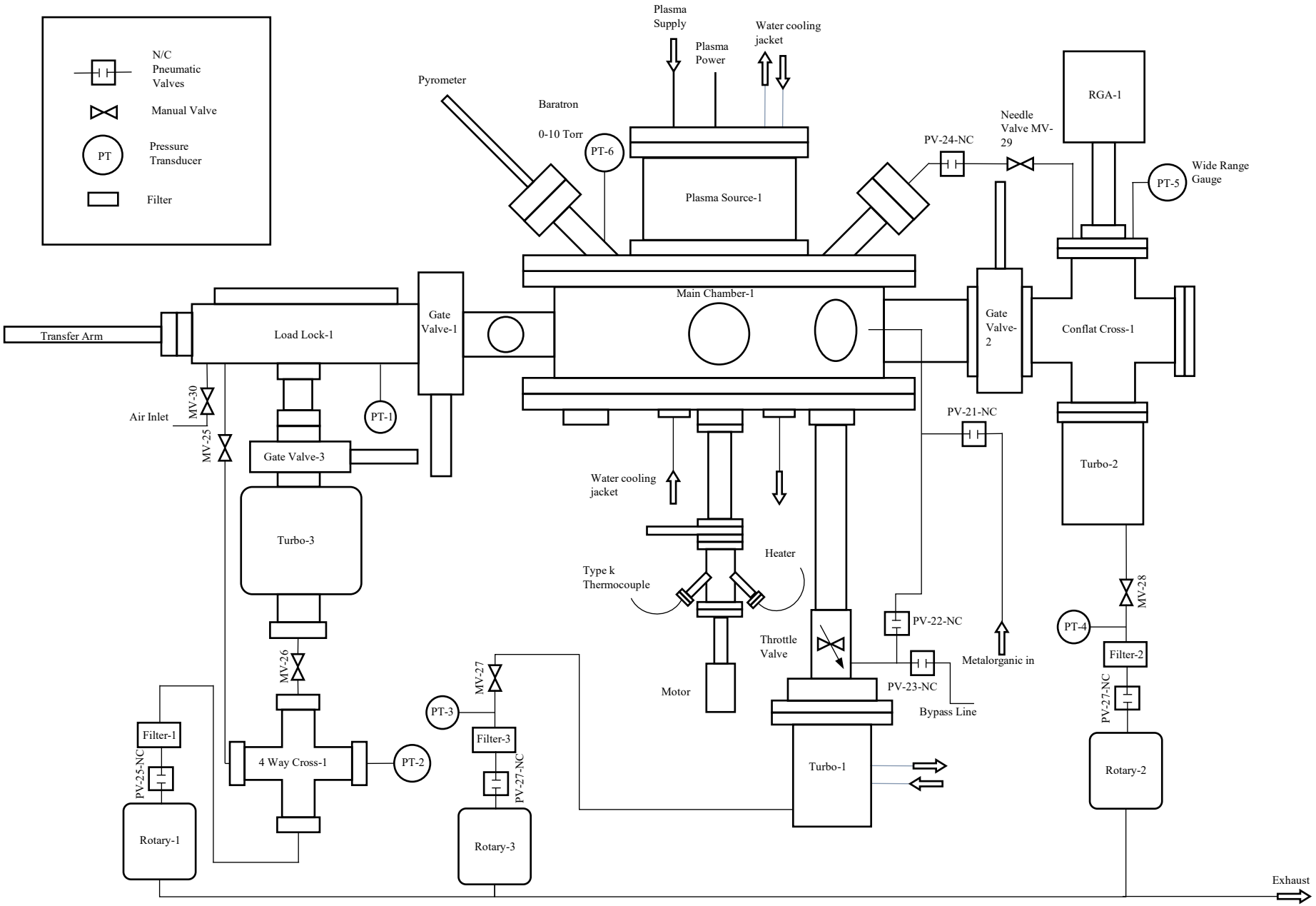

Figure 24: Low pressure remote plasma MOCVD system used in this work.

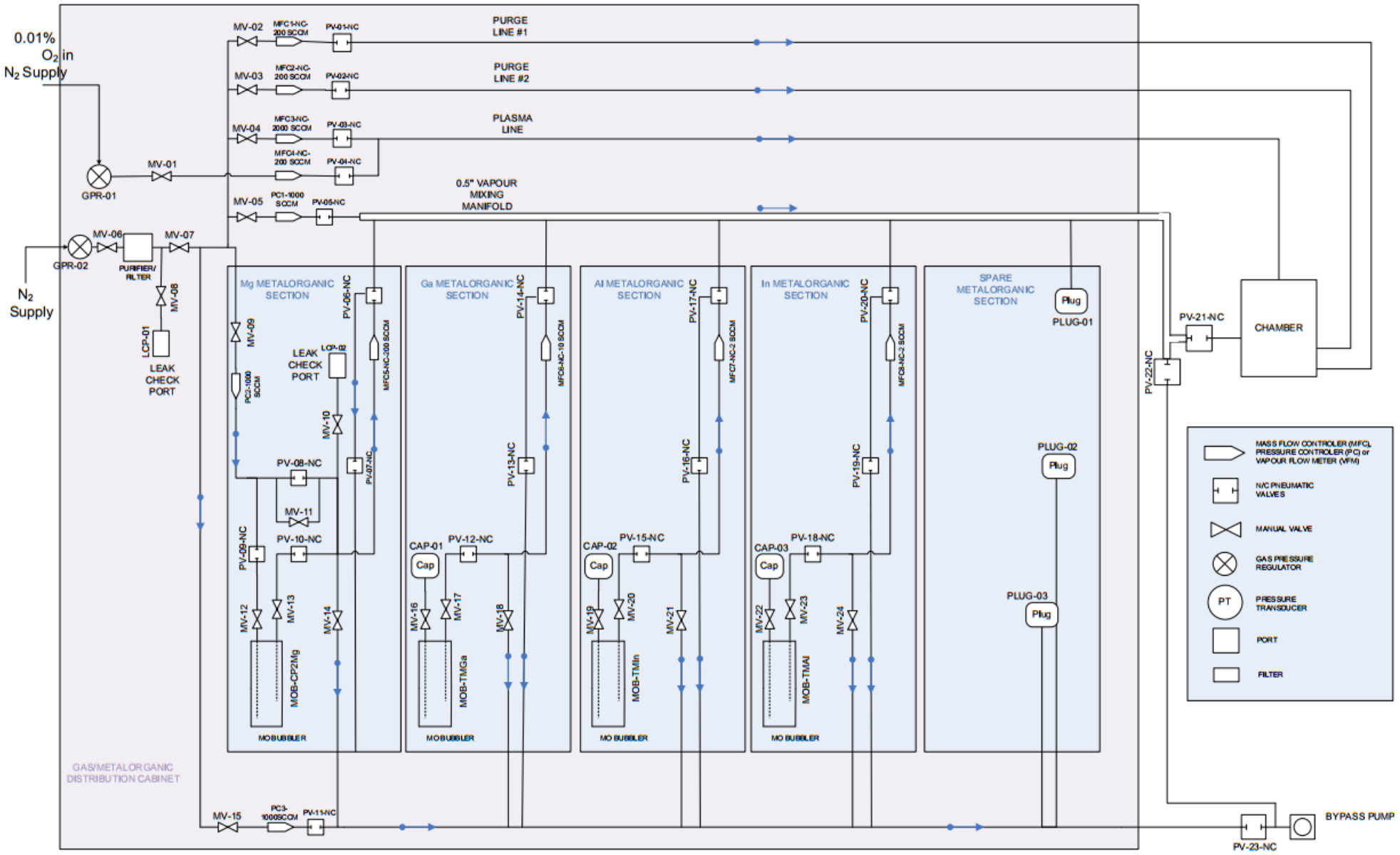

Figure 25: Gas delivery system used to supply the MOCVD system seen in Figure 24.

While thermal ALE is possible [9], [174], the addition of a plasma source bodes well with the low temperature requirements and ALE. The equipment featured in Figure 24 can perform both ALE and FME within the same growth by adjusting the structure of the loops.

The head itself is a modified capacitive plasma system, where the bottom plate acting as the cathode has an array of holes patterned into it, each acting as a plasma aperture into the system. This enables additional generation of nitrogen radicals through the hollow cathode effect [175]. The system is reported to provide significantly higher electron densities as measured by Langmuir probe compared to parallel plate systems [176]. The design can also be scaled by increasing the area of the array and avoids any oxide windows that can be a source of contamination. The cathode and anode can be seen in Figure 26. The cathode array dimensions, anode-cathode gap and source substrate distance are fixed geometric features that determine an optimal operating pressure, which can be determined empirically from the XRD and AFM measurements.

In this work, flow modulation epitaxy (FME) is combined with the hollow cathode plasma system in a dual flow style system seen in Figure 24. N_2 is used as a carrier gas for the TMGa during the Ga deposition, provides background pressure and is a source nitrogen plasma. The nitrogen used in this experiment is Praxair semiconductor 5.0 grade (99.9999%) purity. The significant impurities here include oxygen (1 ppm), water vapour (3 ppm), CO_2 (1 ppm), CO (2 ppm), H_2 (2 ppm) and various hydrocarbons (1 ppm) [177]. The growth conditions have been selected from work performed with sapphire samples. Some techniques such as nitridation are not applicable to LTCC and are not performed.

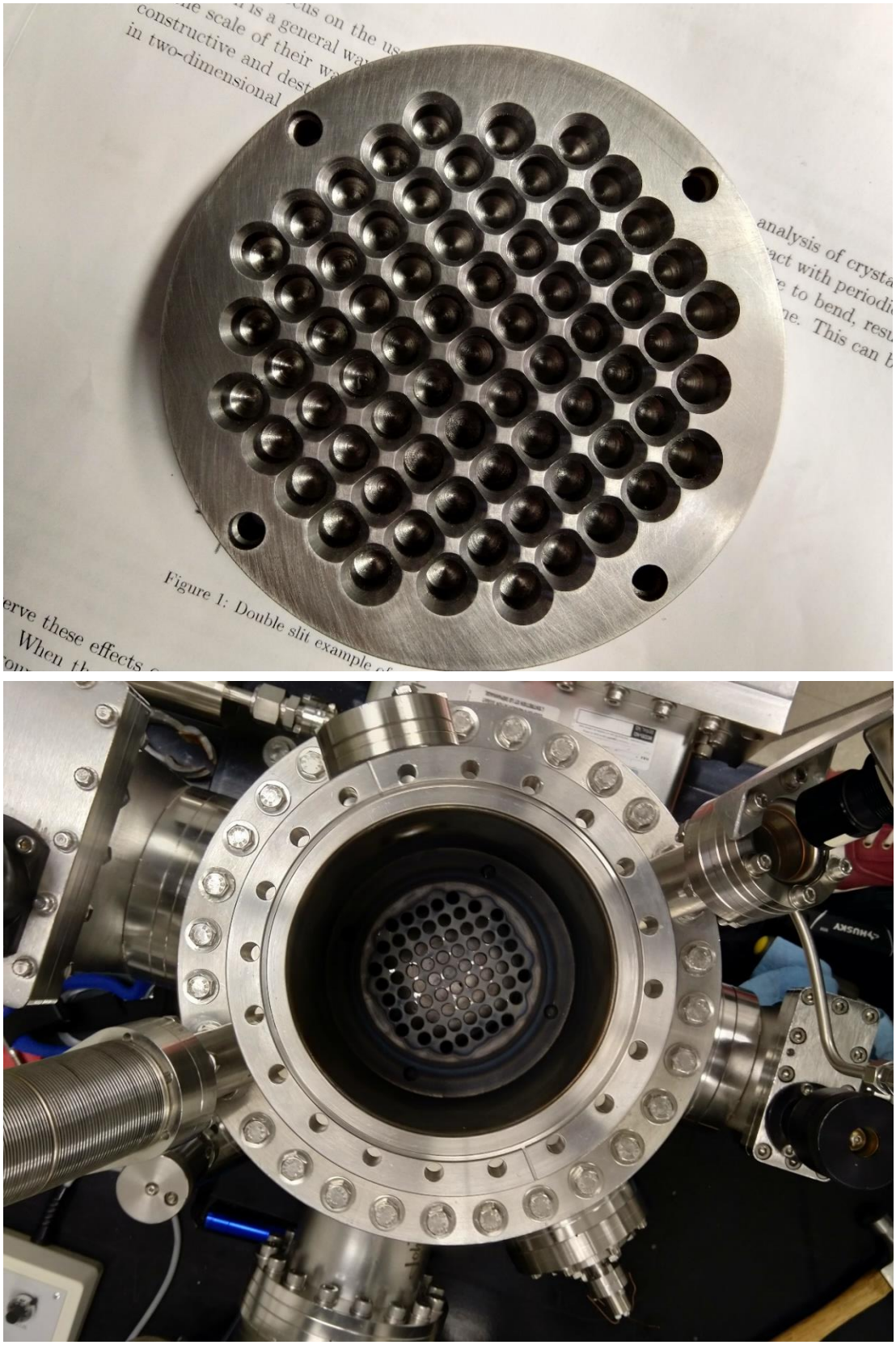

Figure 26: Top-down view of the hollow cathode (lower) and the patterned anode (upper).

4.3.2 Amorphous Deposition

The deposition of nitride materials on amorphous/polycrystalline substrates is a common goal of many different researchers looking to improve on limitations imposed by sapphire. These included but are not limited too, cost, available wafer size and thermal conductivity. In the interest of large area rigid substrates, the main contender is float (soda-lime) glass due too its low-cost production and very large surface areas available. The deposition on glass substrates presents a similar challenge to deposition on glass ceramics since the glass phase mixture of these ceramics gives them their low firing characteristics. A challenge in both cases comes from a lack of an underlying crystal structure to control the orientation of nitride materials during growth, however glass ceramics present the additional challenges of a heterogeneous and rough surface.

It is important that the initial nucleation on the substrate aligns the growth directions for a single orientation along both the a and c axis of the crystal. Normally an underlying single crystal substrate provides an atomically smooth surface and alignment with both axes. Multiple buffering layers between GaN device layers and the substrate are used to mitigate mismatch. This is often accomplished with depositing thin AlN layer [3], [178], [179], a low temperature GaN nucleation layer [4], [180] or more complicated superstructures [181]–[183] followed by several microns of bulk material to further allow dislocations to form loops and annihilate.

For deposition on amorphous substrates a direct deposition is possible [184]. Since the $\{0001\}$ facets have the lowest surface energy, growth will preferentially orient along this direction, however the initial glass surface may be inhomogeneous with no crystalline order and impurities such as sodium and boron are present. Initial nucleation will be randomly oriented and therefore many dislocations will be generated on coalescence. Figure 27 shows the behaviour of GaN nucleation on polycrystalline (a), single crystal (b) and amorphous substrates (c).

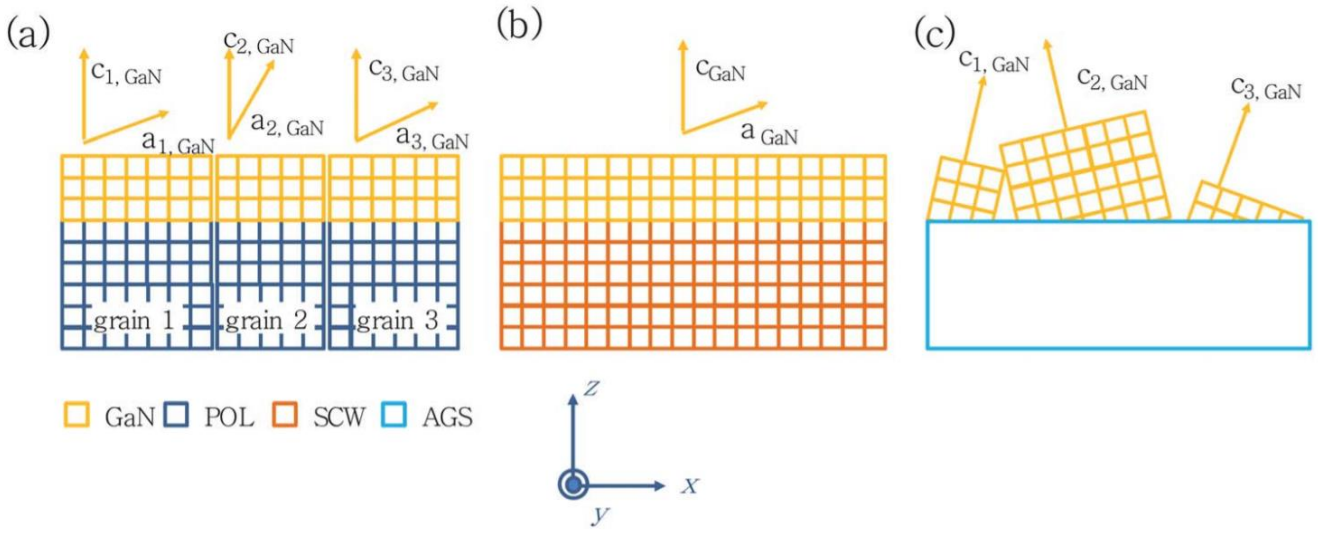

Figure 27: Nucleation behaviour of GaN nucleation on polycrystalline (a), single crystal (b) and amorphous substrates (c) [160].

A buffering layer can be applied to homogenize the surface and provide a surface texture to help align the grains. Titanium has a hexagonal close packed structure giving only a 7.4% [185]–[187] mismatch with GaN, significantly better than sapphire (16.1%) and silicon (17%). The use of a metallic buffering layer also allows its dual purpose as a back contact and is additionally stable with temperature and the NH_3/H_2 environment of MOCVD. Titanium is primarily deposited through vacuum techniques such as electron beam evaporation and sputtering to produce a mosaic structure where grains are aligned vertically but randomly rotated. Like most metals, the thermal expansion is higher than that of crystalline materials and therefore may cause residual stress in the structure and unintentional alloying with GaN is possible.

AlN has been used as a growth template for GaN on both glass and LTCC substrates for GaN growth and can be deposited through reactive sputtering to give a (0002) mosaic texture. Much like GaN, AlN will preferentially orient itself along the c-axis to minimize surface energy provided enough adatom mobility, and additional polishing can be applied to lower the roughness.

Limited research has been done on its applications with LTCC, with some as a heat spreading dielectric [95], [97], and recently as a template for MBE GaN [96], [188].

ZnO has been deposited on several substrates, including glass [189], [190], silicon [191], [192], and sapphire [193]–[195] using a variety of vacuum techniques such as MBE, ALE, PLD, and MOCVD. A major disadvantage of using it as a buffer for nitride growth is how easily it is reduced by the ammonia used as the nitrogen precursor in many growth techniques, especially at growth temperatures upwards of 1050 °C. The stability of ZnO due too the high vapour pressure of zinc was also found to be an issue, contributing to system contamination (see 2.2.1.1). Use of ZnO buffers for GaN are therefore not expected to be possible under conventional MOCVD growth conditions.

4.3.3 Surface Roughness

The reduction in surface roughness of the substrate is a critical step in preparing substrates for thin film deposition. For crystalline substrates this is done through a chemical-mechanical polishing using fine particles in a slurry. This technique can be applied to ceramics, however the inhomogeneity of ceramic surface combined with voids induced in the structure from the sintering process limit the roughness achievable. Examination of the electrical properties of sputtered AlN layers has shown the importance of a smooth surface in aligning columnar grains to reduce leakage currents and structural voids [96].

The initial LTCC sintered surface is rough (0.4 um rms) with several microns of waviness over the surface. Both properties measure surface height, but as a distinction the waviness can be considered as lower frequency variations that the roughness is imposed upon. This distinction can sometimes be difficult to discern in rough samples and an arbitrary threshold between the two may have to be chosen. Both properties can however be improved through a multi step polishing

process. Recent work on polishing has been reported to reduce the average roughness to 345 nm measure via laser scanning microscopy (LSM) [96], and an rms roughness as low as 120 ± 5 nm with AFM [196]. The pore structure was then effectively filled by sputtering 8 microns of AlN, reducing the rms roughness to 42 nm [197]. The sputtered AlN layer were then polished in a similar manner to further reduce the rms roughness to 5.6 nm over a 5x5 μm area [197]. An overview of the process can be seen in Figure 28.

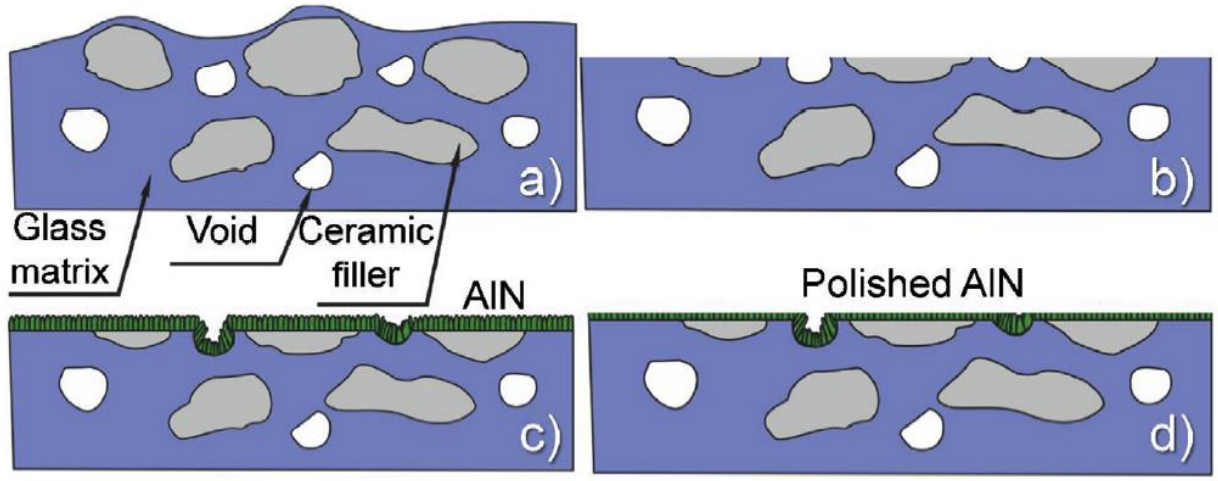

Figure 28: AlN sputtering treatment of the bare LTCC (a). The initial surface polishing (b) levels the waviness and opens surface voids, decreasing the initial rms roughness to 120 nm. The sputtered AlN (c) reduced the roughness again to 42 nm and a final polishing (d) reduced the roughness to 5.6 nm measured on a 5x5 μm AFM scan [188].

These layers were used as a template for GaN growth using MBE, with ALN thicknesses between 0.75 μm and 9.90 μm tested [188], [197]. The deposited GaN layers were approximately 400 nm in thickness with temperatures varying from 600-900 °C using Dupont 9k7V LTCC. The GaN layers under all conditions were found to be columnar polycrystalline layers, with the best results showing a relative texture coefficient of 80% for the (0002) planes and rms roughness of only 5.7 nm over a 1x1 μm^2 AFM scan, largely dependant on the MBE process conditions. Some of the large surface features of the LTCC were still found to be present in the upper GaN layer, in some cases leading to thin or absent sections.

Similar work on the planarization of LTCC has been performed using silica derived from Tetraethyl orthosilicate (TEOS) [72]. TEOS is a well-established precursor for sol-gel silica, an amorphous silicon dioxide layer used in spin-on-glass techniques. The chemistry involved is similar to the ZnO chemistry previously covered, however no crystallization will occur with the silica. Multiple coatings of TEOS layers were observed to crack upon reaching a critical thickness due too difference in TCE. This was improved by using a composite silica coating, where larger silica particles (35 nm diameter) were mixed with TEOS sol-gel to decrease the shrinkage (and thus strain) on drying. At a 1:3 ratio of TEOS silica to nanoparticle silica the average surface roughness was reduced from 350 nm to 64 nm using spray pyrolysis, 81 nm using dip coating and 72 nm for spin coating measured by Laser Scanning Microscope (LSM). The thickness in these layers was increased to around 1 μm/coating for each method and cracking was avoided. This work demonstrates the ability of sol-gel to coat LTCC and reduce roughness, however it is clear thick layers are required and cracking may occur. The work in [72] was performed on unpolished LTCC (CT700) substrates, therefore it can be expected polishing to further improve these results.

Planarization of many different metallic substrates such as Hastelloy [198], [199], Ni-W [200], [201], Mo [202], stainless steel [203] has been demonstrated in the last decade using the solution deposition planarization (SPD) technique. In all of these works an amorphous oxide material is deposited on the rough metal surface through dip coating to significantly lower the surface roughness and act as a diffusion barrier for the metal substrate. One or many texture layers are then applied though a PVD technique such as Ion Beam Assisted Deposition (IBAD) or sputtering. The texture material is usually MgO (111), but AlN (0002) has been demonstrated through reactive sputtering [204]. The substrates in these works are usually metal foils that have been polished to an RMS roughness on the order of 10-100 nm and using the planarizing properties

of the liquid surface tension, this technique has shown the reduction of surface roughness to <2 nm RMS [205]. These textured metal foils have been shown as suitable substrates for MOCVD growth of YCBO superconductor films [206] and III-Nitride devices [202].

In this work the surface of polished LTCC will be planarized and homogenized through three different oxide coating techniques. Al_2O_3, SiO_2, and ZnO are coated LTCC through three different low temperature techniques for GaN growth. Alumina was deposited through anodic oxidation of metallic aluminum, silicon dioxide through spin coating sol-gel TEOS solutions and zinc oxide through ZAD sol-gel. The first two techniques and LTCC polishing were performed by our research partners at TU Sofia and TU Ilmenau. ZnO dip coating and GaN CVD on all samples was performed in the Lakehead research lab.

5. Defects In III-Nitrides

Defects in the crystal structure are deviations from the perfect crystal which have influence on its optical and electrical properties. At high enough concentrations they can be the controlling factors in device operation and lead to undesirable device behaviour. They are classified according to their dimensionality, acting from a single point in the lattice (0D), along a line (1D), in a plane (2D) or in a volume (3D) of the material.

In this chapter a review on the defects is given mainly through density functional theory (DFT) computations found in literature. This computational technique relies on approximating bulk material properties by creating a supercell of repeated unit cells and using a functional is used to describe the electron density. Defects and impurities can be introduced into the lattice to observe their electrical, optical, and physical properties. A typical supercell can consider on the order of hundreds of atoms before becoming computationally prohibitive (a 96-atom supercell is common). The motivation behind this technique is to reduce the dimensionality of the many body electron-electron interactions to just three spatial dimensions of the density. Many different approximation techniques exist all of which trade some accuracy of the exact Schrodinger solution for computational speed. The solutions found using any computational method have some degree of error which may be impossible to estimate, it is therefore important to use these results as a supplement to experimental data when possible.

5.1 Extended Defects

Extended defects are those which exist over long distance in one (dislocations) or two dimensions (planar defects), both of which can extend the full device structure to the surface. Experimental observation in GaN has generally shown that these defects alone tend to be

electrically inactive under the absence of dangling bonds and wrong bonds (Ga-Ga, N-N bonding). Even in the case of edge and screw type where dangling bonds may be present, three-fold coordinated dangling bonds from Ga atoms are expected to relax into sp^2 coordination and lose an electron the doubly occupied nearest neighbour nitrogen, leaving an empty Ga state above the conduction band minimum and occupied N states below the valence band maximum. The ionicity of the III-N bond gives a high formation energy to wrong bonds which makes them unlikely to form. It is believed that this ionicity induced behaviour is responsible for the ability to produce efficient LED's despite many orders of magnitude more dislocations than other III-V materials [207].

Though they are not expected to generate gap states on their own, extended defects serve as ionized lattice distortions and are undesirable since they will decrease charge mobility in the layers. The local strain caused by these defects may also lower the overall formation energy for impurity point defects that can introduce gap states.

Three types of perfect threading dislocations are seen in GaN, known as edge, screw, and mixed type with burgers vectors ($\vec{b}$) of $\frac{1}{3}\langle 1120\rangle$, $\langle 0001\rangle$ and $\frac{1}{3}\langle 1123\rangle$ respectively. The Burgers vector is defined by the completion of a clockwise closed loop around the dislocation as seen in

Figure 29 and Figure 30 for the edge and screw type respectively. These are referred to as perfect dislocations since the magnitude of the burgers vector is equal to a lattice spacing, in contrast to partial dislocations where it is smaller.

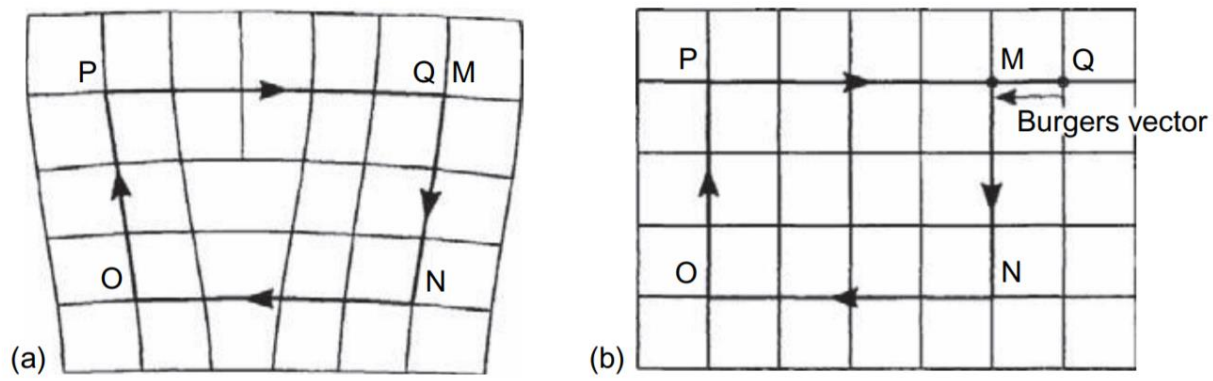

Figure 29: a) Edge dislocation resulting from the insertion of and extra half plane and b) normal lattice with burgers circuit overlay to show the burgers vector [208].

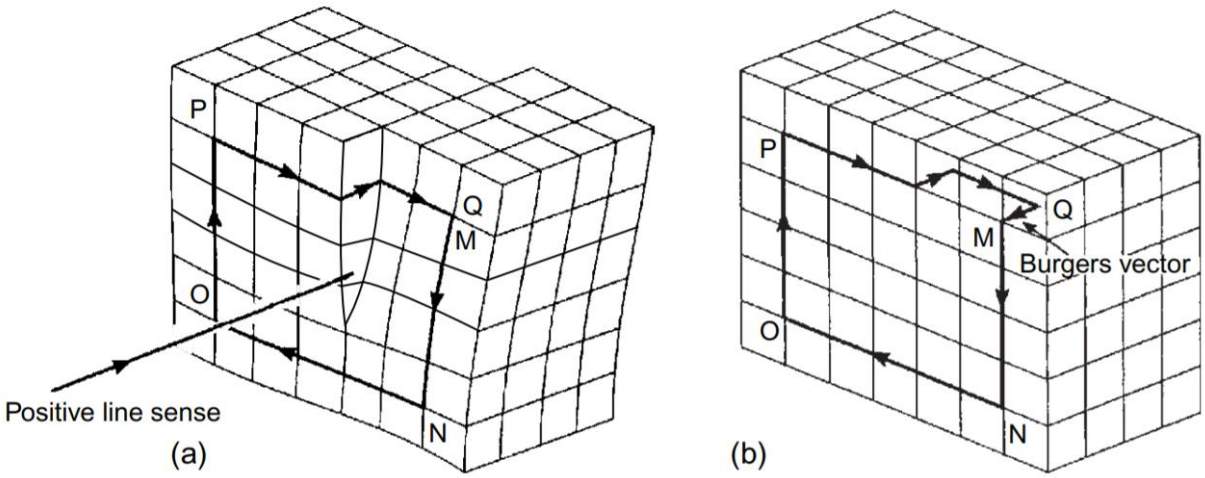

Figure 30: Screw dislocation and b) normal lattice with burgers circuit overlay to show the burgers vector [208].

Growth of crystalline layers on foreign substrates inevitably leads to dislocations due too lattice and thermal expansion mismatch between the materials. This mismatch is expressed as the difference in the crystallographic planes perpendicular to interface of the two crystals. In the case of (111) Si /GaN the relationship is $(1\bar{1}00)_{GaN} \parallel (110)_{Si}$ and in sapphire/GaN systems it is the $(1\bar{1}00)_{GaN} \parallel (11\bar{2}0)_{Al_2O_3}$ planes. For ZnO (and 6H-SiC) no rotation is necessary since the lattice is the same shape and close in size and the match is $(1\bar{1}00)_{GaN} \parallel (1\bar{1}00)_{ZnO}$.

Misfit dislocations will also appear at the interface in these systems after a certain layer thickness to accommodate growing biaxial strain as thickness increases. Since these appear along the interface, they tend not degrade the performance of device where the active region is further away near the growth face of the crystal.

Dislocations originating from the interface which travel (thread) vertically through the bulk of the material towards the growth face will typically pierce interfaces, creating inhomogeneous regions or act to scatter lateral current flow in devices. A major aspect of improving active layer mobility and increasing device lifetimes is the reduction of these dislocations. During the initial nucleation of systems with relatively large mismatches (such as GaN on Si and Sapphire), growth initiates as individual island crystallites that will continue to expand along (0001) and $(1\bar{1}00)$ low energy facets provided enough thermal energy for adatom migration. Low temperature buffering layers are usually grown first to encourage growth along $(11\bar{2}2)$ facets which can act to bend dislocations formed at the interface into one another. The initial grains eventually coalesce into a layer where their relative orientation (tilt and twist) to one another will induce dislocations along their interface. If islands meet with a relative rotation about the c-axis (Figure 31b) edge type dislocations will be generated, with the amount depending on the degree of relative rotation. If grains meet with a relative rotation about a $\langle 1\bar{1}00\rangle$ edge (Figure 31a) they will generate a screw dislocation parallel to the c-axis and another along $\langle 11\bar{2}0\rangle$ [209]. This leads to a so called mosaic structure in GaN, where a lateral correlation length can be observed due the limited size of the grains (Figure 31).

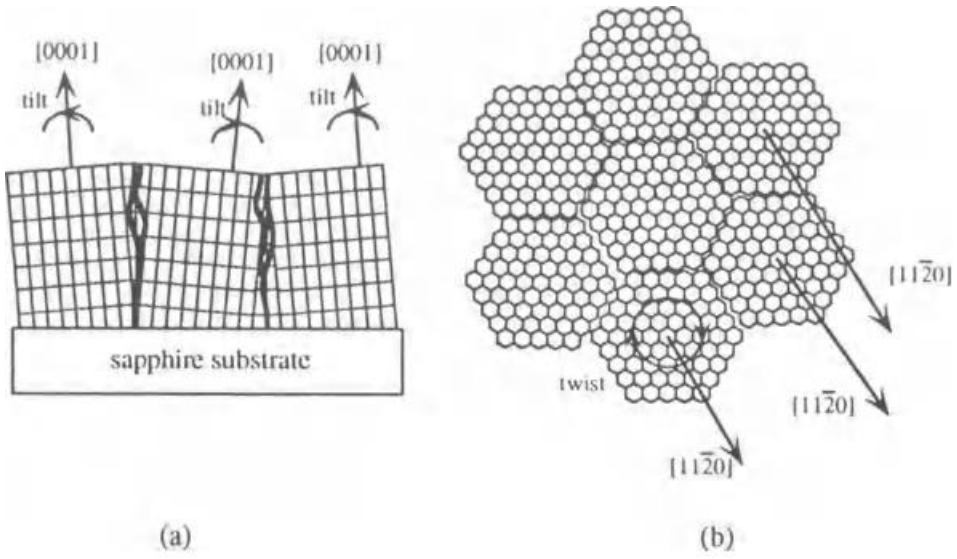

Figure 31: the effect of grain tilt (a) and grain twist (b). Tilt (a) causes slight variations in heights of the coalescing nuclei leading to screw type dislocations. Twist (b) introduces edge type dislocations [109].

Screw type dislocations have been experimentally shown through a combination of cathodoluminescence (CL) mapping and selective defect etching to not be electrically active recombination sites in LED's, whereas mixed and edge type act as non radiative recombination centres, and have been shown to getter impurities due to local stress fields [210]. Studies on their role in Schottky diodes have shown that mixed and pure edge dislocations can act as current traps, lowering the overall conductivity of layers and leakage primarily occurs at screw dislocations [211]–[213]. These leakage studies on Schottky diodes use conductive AFM mapping combined with selective defect etching to correlate large etch pits with open screw type dislocations and reverse current leakage. The behaviour of impurities at these site has been examined in literature using scanning transmission electron microscopy (S-TEM) combined with electron energy loss spectroscopy (EELS) to show that oxygen preferentially segregates to the inner surfaces of open screw type dislocations, where it substitutes nitrogen acting as a donor [214]. These effect of these dislocations on Schottky diodes can be reduced by modifying the interface with a passivating oxide between the Schottky contact and GaN layers [215], [216]. Thermal treatment of the diode in

ambient environment has been shown to create a 2-3 nm Ga_2O_3 layer that can passivate the surface donor states, decreasing leakage and increasing effective barrier height.

5.2 Point Defects

Research in point defects is heavily focused on their formation energies and charge states calculated from first principles using some variation of density function theory (DFT). These formation energies are related to the defect concentration by:

$$c = N_s e^{\frac{-E_f}{kT}} \tag{5.1}$$

Where N_s is the number of possible sites the defect can occupy and E_f is the formation energy determined from the DFT calculation.

5.2.1 Vacancies

Several publications have comprehensive review of point defects in GaN using DFT to determine the most abundant defects present and their likely charge state [222]–[224]. The calculated formation energies from [222] using the semi local Perdew, Becke, and Ernzerhof (PBE) density functional are shown in Figure 32.

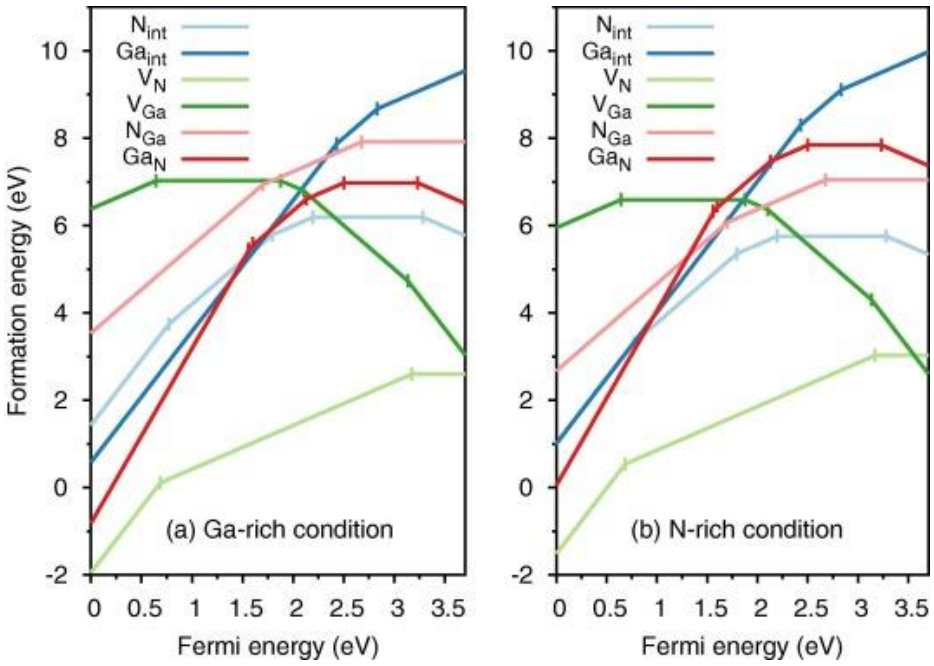

Figure 32: Formation energy for native point defects in GaN under a) Ga rich conditions and b) N rich conditions [222].

Their results agree well with the other works and the lowest formation energy seen in both Ga and N rich layers is the nitrogen vacancy, with a negative formation energy for p-type conditions. These vacancies are therefore a significant source of compensation donors in p-type materials and were originally presumed to be the source of high n-type background concentrations found in nominally undoped layers, however similar calculations for the formation energy and charge state identify oxygen donors to be the most significant source [222].

5.2.2 Impurities

The most common impurities found in nitride growth are carbon, oxygen and hydrogen. Carbon and hydrogen are by-products of the decomposition of the metalorganic precursors and oxygen comes from residuals in the vacuum, impurities in the nitrogen source and water vapour.

5.2.2.1 Carbon

Computational studies of the role of carbon using the hybrid functional developed by Heyd, Scuseria, and Ernzerhof (HSE) in GaN have shown the most energetically stable position for carbon is a nitrogen substitution, C_N. The exceptions to this are gallium substitution (C_{Ga}) only seen in nitrogen rich conditions where the Fermi level is below the mid gap and interstitial carbon (C_i) in Ga rich conditions [225].

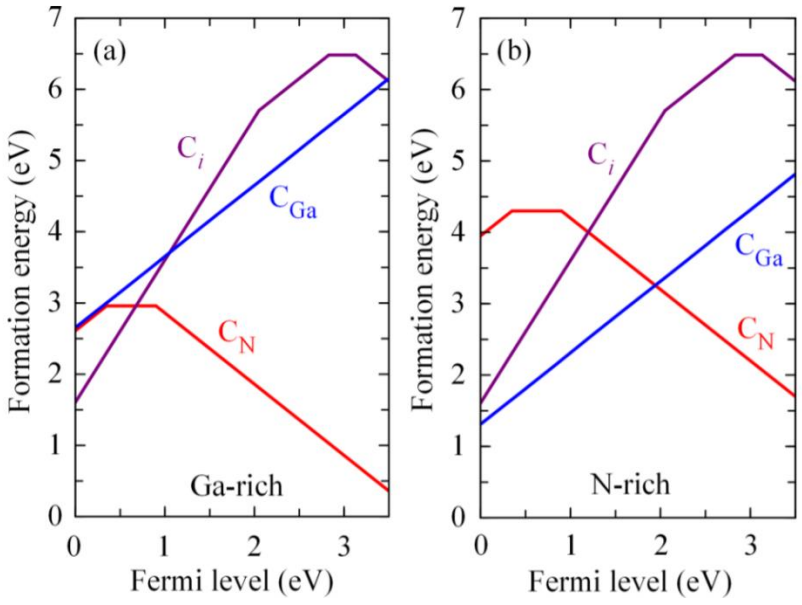

Figure 33: HSE-DFT calculations of the formation energies of gallium substitution (C_{Ga}), nitrogen substitution (C_N) and interstitial carbon (C_i) for carbon impurities. Gallium rich (a) and nitrogen rich (b) stoichiometries are considered [225].

Previous work from the same group calculated the C_N state to be a deep level acceptor with an activation energy of 0.90eV above the valance band [226]. In this work they also proposed the $C^0_N \rightarrow C^-_N$ transition to be responsible for the yellow luminescence seen many MOCVD grown devices [227], [228]. Due too its tendency to form deep acceptor states, carbon has been used as a compensating dopant for unintentional donors present in GaN.

5.2.2.2 Oxygen

Oxygen has been identified as the primary candidate for unintentional background n-type doping in nitride materials. HSE-DFT calculations (Figure 34) have shown the formation energy of the oxygen substitution on nitrogen sites to be the most favorable position for the impurity where it forms a shallow single donor with an activation energy of 29-32.4 meV [229]–[232].

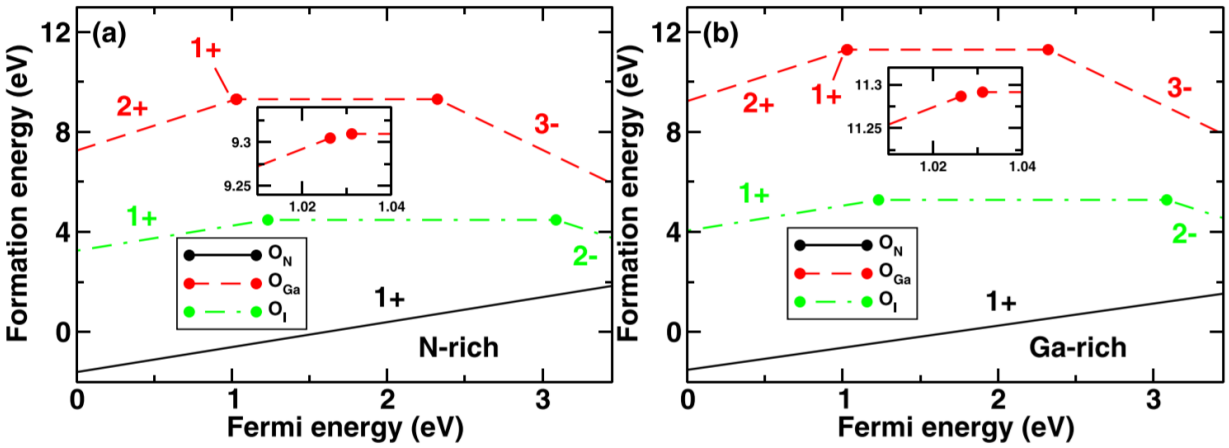

Figure 34: HSE-DFT calculations for oxygen with various positions and charge states in wurtzite GaN. In both a) nitrogen rich and b) gallium rich conditions the most stable position for oxygen is a nitrogen substitution (O_N) where it forms a single donor [233].

Given the relatively large concentration of threading defects and their ability to concentrate oxygen contaminants, high levels of oxygen can be particularly detrimental since the combination can create conductive line defects that run vertically through devices. Oxygen may also incorporate up to 25 at% in GaN without disturbing the sp^3 bonding and lead to high levels of background donors even in highly crystalline samples due too the relatively close bond length to Ga-N [234].

5.2.2.3 Hydrogen

Hydrogen is known to act as an acceptor in n-type materials and a donor in p-type materials. Due too its relatively small size, in the +1 state it is energetically favorable for it to sit in between Ga and N bonds parallel to the c-axis forming a bridge between the atoms, only distorting the Ga

tetrahedral position. For the -1 and neutral charge states it is located in an octahedral position [233]. Figure 35 shows the stable occupation position for each of these charges in the wurtzite unit cell. Figure 36 gives the formation energy of each of these complexes given the position of the Fermi level.

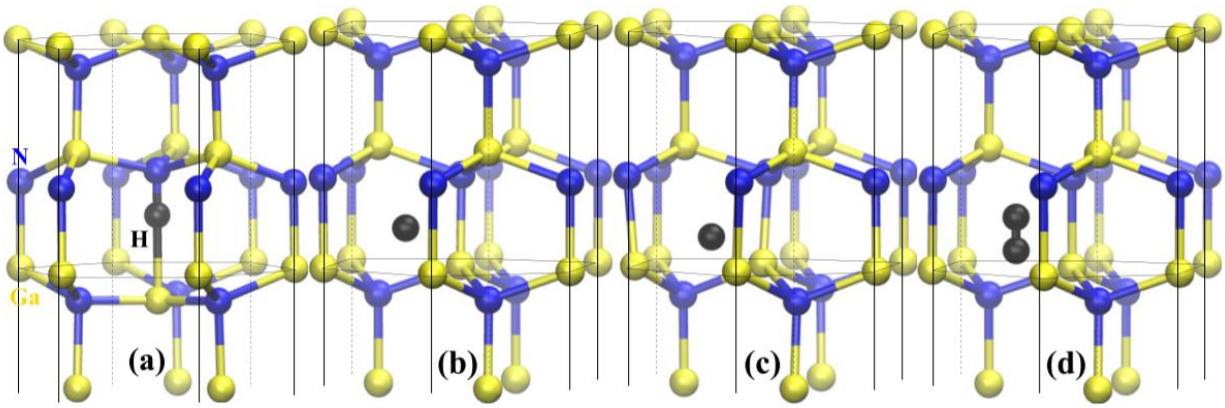

Figure 35: Stable positions of hydrogen in the GaN wurtzite lattice for the a) +1 donor state where it is in line with the Ga-N bond b) the octahedral neutral charge state c) the octahedral acceptor charge state and d) the H_2 molecule [233].

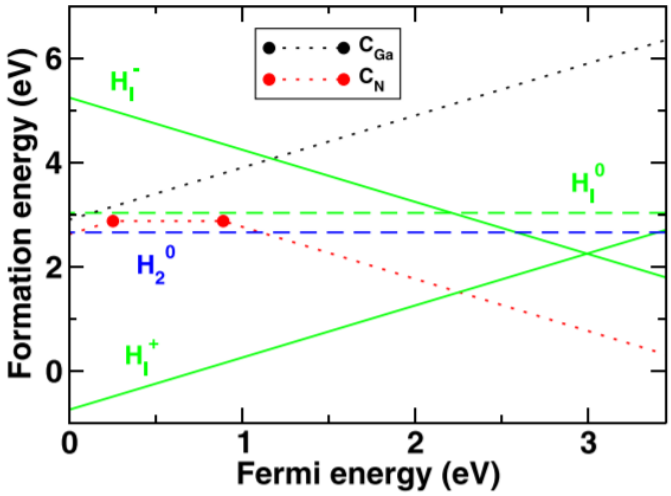

Figure 36: Hydrogen interstitial formation energy for different charge states of hydrogen [233].

The carbon nitrogen substitution (C_N) and carbon gallium substitution (C_{Ga}) in Ga rich condition are also included in Figure 36 since their complex formation is energetically favorable

in n-type conditions. Hydrogen is known to passivate dangling bonds in many materials (such as amorphous silicon) and was concluded to be the source of unintentional Mg passivation in early p-type doping. Due too the low diffusion barrier of hydrogen in GaN (0.7eV) it was able to be removed with annealing. Hydrogen may also form double donor complexes with carbon gallium substitutions in p-type materials and compensation acceptor type carbon nitrogen substitutions (C_N). Figure 37 shows the formation energy of these complexes along with the interstitial positions of hydrogen [233].

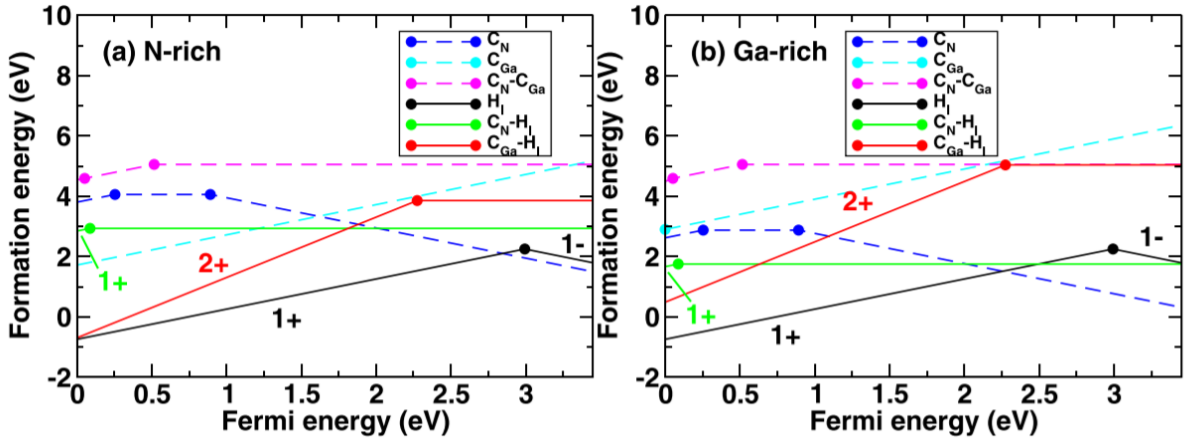

Figure 37: Interstitial hydrogen charge states and complex formation energy in a) nitrogen rich and b) gallium rich conditions [233].

Substrate diffusion may also be a factor in device processing. The stability of sapphire substrate and relative thickness used in planar device does not make this an issue for sapphire heteroepitaxy, but in silicon significant diffusion of Ga has been observed into the wafer, disturbing the morphology of the subsequent growth (meltback etching). However, Zn-O bonds are weaker than Al-O bonds and an intermixing diffusion at the interface is possible. Reports of Molecular Beam Epitaxy (MBE) grown GaN on ZnO have shown at 700 °C a thin (3-4 nm) interdiffusion layer can be observed with TEM, likely resulting in the formation of Ga_2O_3 and Zn_2N_3 [235], [236]. Zn is known to be a deep acceptor on substitution of Ga (Zn_{Ga}) and was

originally researched as a potential dopant for p-type Ga [237]. However, due too the relatively high ionization energy (0.46eV) compared to Mg (0.26eV) it saw little application in real devices [238].

5.3 Conclusions

The influence of screw dislocations on the interface is the most concern for Schottky contacts. They present a high surface area and local strain attracts oxygen substitution that acts as an n-type donor. To maintain a significant barrier in the Schottky diode the unintentional doping should be kept low. As far as the controllable process factors go, this means lowering the surface roughness as much as possible to minimize the generation of edge and screw defects which may act to getter oxygen due too their local strain field. Any oxygen impurities in the layer will act as an n-type donor by occupying a nitrogen site in the lattice. Screw dislocations can have open cores which segregate more oxygen donors on their (1-100) interior surfaces and can diffuse oxygen down their length. They are primarily generated in the coalescence stage of the growth from grain due too differences in rotation around the $\langle 1\bar{1}00 \rangle$ direction.

In the case of solution deposited ZnO as a buffering technology it is also possible that oxygen diffusion may be a significant contribution. Impurities related to oxygen are largely unavoidable aside from keeping low water content in the vacuum system and using high purity precursor materials. High temperatures and low pressures are generally desired to encourage trimethyl group dissociation as far from the substrate as possible, however these process parameters are fixed from the low melting point of the glass phase in the ceramics and the cathode-anode gap in the capacitive plasma head.

6. Instrumentation

Process dependant material properties that can affect device performance such as defect densities, crystal texture, surface roughness and impurities can be detected using a wide range of characterization tools. This chapter is dedicated to the tools available at the semiconductor research and instrumentation labs at lakehead university.

6.1 X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a non-destructive, non-contact method of determining the crystal structure in solid samples. This technique relies on the constructive interference of scattered X-rays from the crystal lattice of the sample. Samples are placed in the path of a collimated beam of X-rays where the angle of incidence (θ) is swept over a set range to determine which angles satisfy the Bragg condition.

Diffraction in general can occur when a wave encounters a series of regularly spaced scattering sites spaced on the same order as the wavelength of the incident wave. The X-rays used in these experiments are usually from a copper anode held in a vacuum tube where a high-tension voltage (10-40kV in our system) is applied across to tube and the emission current is controlled (5-45mA). High voltages are required since L to K transitions are needed for wavelengths of interest ($\lambda \approx 1$Å). Additional X-rays generated from higher shells can be filtered by lower atomic weight metal foils since absorption edges tend to increase along rows in the periodic table (Ni is used for copper anodes). Additional apertures and collimator slits are used to limit beam divergence. In high resolution applications a finer bandpass filtering can be achieved using a single crystal monochromator on the input and an analyzer crystal on the output. The input monochromator consists of a quality single crystal sample (graphite or (220) Ge are commonly

used). The beam divergence may also be lowered by the inclusion of parabolic mirrors on the incident beam.

When the X-rays are incident on the sample, they will scatter on the electrons at each atom with both inelastic and elastic scattering. The Inelastic scattering (Compton, Bremsstrahlung) leads to a broad incoherent background in the detector, while elastic scattering allows the observation of interference, dependant on the crystal structure and the incidence angle θ. The Bragg-Brentano scan geometry used by the PANalytical X'Pert Pro in this work can be seen in Figure 38.

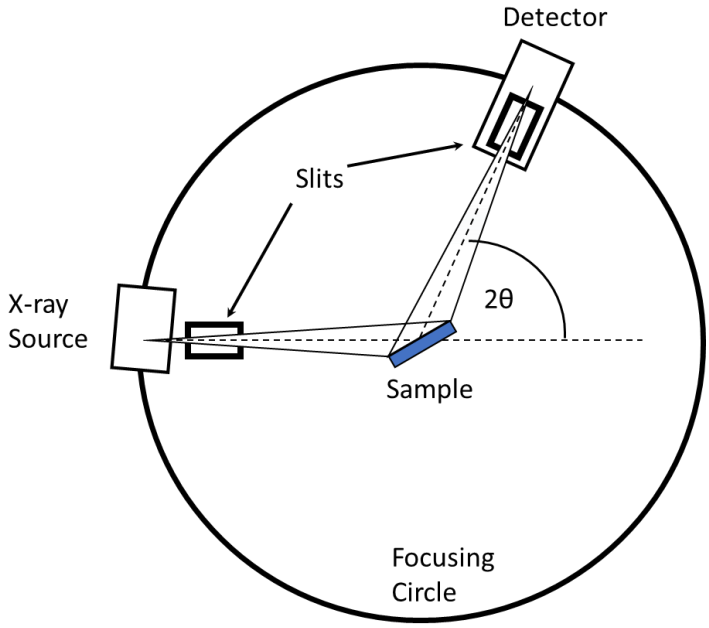

Figure 38: Bragg-Brentano goniometer experimentally used for XRD. Measurement of planes parallel to the surface are performed using a Θ-2Θ scan where the sample remains flat with the source and detector moving at the same constant rate.

This system is designed to focus on the plane of the sample with high intensity and detect crystal planes parallel to the surface. The type of scan used in this work is a Θ-2Θ scan where the sample remains flat and the source/detector are moved at the same constant rate. It cannot be used to produce full reciprocal space maps or produce high resolution rocking curves but can still

provide useful information about the crystal unit cell and orientation. To determine useful information about the crystal structure the Bragg condition must be applied and a priori knowledge of the crystal shape is needed to identify the plane index. For all nitrides and ZnO the structure is the wurtzite (WZ) cell and miller indices can be found using:

$$\frac{1}{{d_{hkl}}^2} = \frac{4}{3}\left(\frac{h^2 + hk + k^2}{a^2}\right) + \frac{l^2}{c^2} \tag{6-1}$$

Since the WZ cell will preferentially orient its c-axis perpendicular to the surface, the $\{000l\}$ peak properties are used for comparing growths.

The Bragg Condition can be best illustrated with the ideal crystal sample in Figure 39.

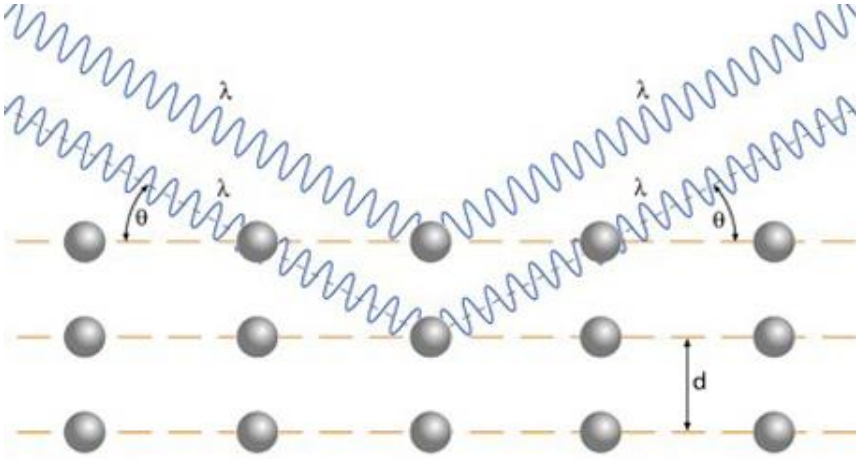

Figure 39: Bragg condition for x-ray diffraction [234].

For constructive interference to occur X-rays leaving the sample must arrive in phase at the detector. X-rays scattering from different planes within the crystal must therefore travel an additional distance of $n\lambda$ to not disrupt their relative phase. From the geometry in Figure 39 the length of the path over which it must do this is $2dsin\theta$. Therefore when $2dsin\theta = n\lambda$ it can be expected that a high intensity of X-ray's will be detected. This is the Bragg condition and is a very useful observation since θ is experimentally easy to measure and control, while interplanar spacing

on the order of 1Å is difficult to observe. The large area and penetration depth of the X-rays can sample statistically large volumes of material compared to electron or neutron diffraction and can be performed in ambient environment.

6.1.1 XRD Analysis

In real crystals there exist imperfections that disrupt the perfect order of the crystal and therefore broaden the distribution of scattering centres observed. Given the significant volume probed by the X-rays, a statistically large number of d planes are sampled and a Voigt profile is typically observed. A Voigt profile is a convolution between a Lorentz and Gaussian distribution, which for curve fitting analysis is commonly approximated as a linear combination of the two (referred to the Pseudo-Voigt distribution). The angular spread of the intensity peak is related to the distribution of the d-spacings withing the crystal by the Bragg condition. High quality crystals will consistently have the same spacing between planes and a sharp peak will be observed. Conversely, as the crystal becomes more disordered the peak will broaden until it flattens into the background noise. The broadening of the peaks is largely attributed to shape or size related effects, with shape effects contributing to a Gaussian like peak and size effects leading more a Lorentzian peak [47].

Many different parameters can affect interplanar spacing such as crystallite size (grain boundary density), defects and impurities, alloy composition and strain induced from the substrate. Additional broadening is contributed from the instrument since beam divergence and linewidth on the X-rays is unavoidable, for the purposes of comparison from the same instrument these will be ignored. The full width at half maximum (FWHM) is a standard measures of crystal quality for XRD. In the case of the Θ-2Θ scans used in this work the broadening is related to the distribution of planes parallel to the surface, which can be attributed to strain gradients induced by the substrate

and microstrain from impurity atoms and dislocations in the c-plane, and composition gradients. The broadening of the peaks in these types of scans does not directly measure the tilt or twist of the grains, for which high resolution rocking curves are needed. The lowering of the FWHM therefore represents a reduction in the strain induced by TCE/lattice mismatch along the LTCC/Oxide/GaN structure.

6.2 Scanning Electron Microscope (SEM)

The SEM is a versatile tool for imaging the surface of samples with high resolution in real time. The Hitachi Su-70 Schottky Field Emission SEM is capable of resolving 1 nm at 15 kV acceleration and is equipped with an Oxford Aztec 80 mm/124 eV Energy dispersive X-ray spectrometer (EDX) and solid state back scatter electron (BSE) detector for back scatter imaging. The main application of the SEM in this work is with its ability to gather accurate thickness profiles along a cross section of a sample as well as its ability to identify surface morphological features in an unambiguous way along with chemical composition.

A typical SEM column can be seen in Figure 40 showing the rastering of the beam over the sample surface.

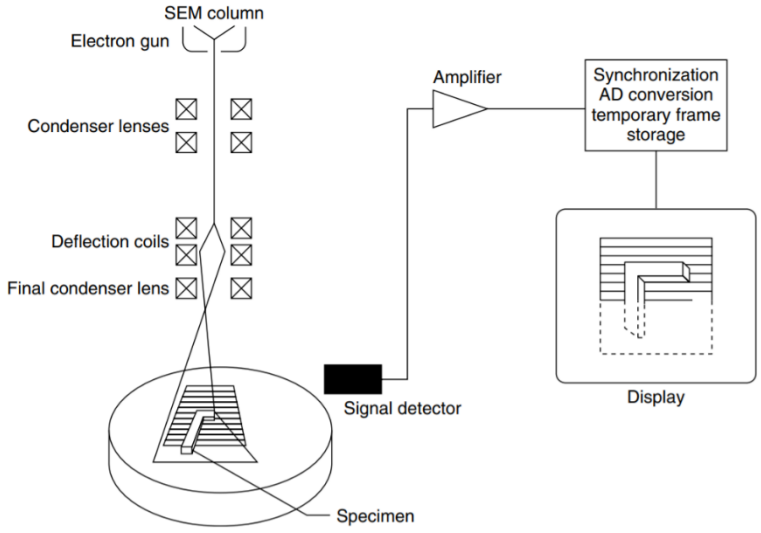

Figure 40: Schematic diagram of SEM operation [239].

The electron beam has many different interactions with the surface, producing different secondary particles used for analysis seen in Figure 41. The beam itself can penetrate several μm of material, however Secondary and Auger electrons generated beyond the first few nm will not have enough energy to escape to vacuum and be detected. Secondary electrons are generated from impact ionization in greater quantity than the Auger electrons and are the primary source of surface imaging.

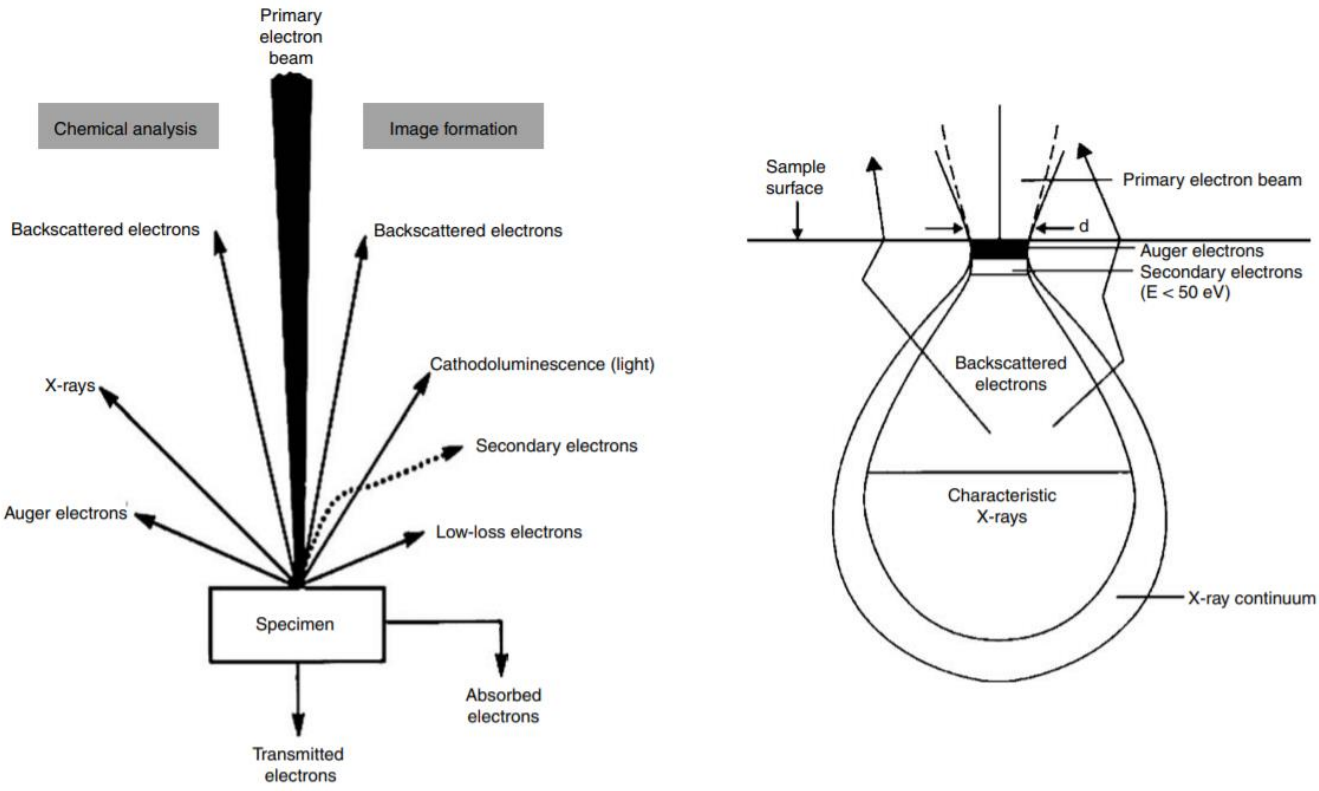

Figure 41: Primary electron beam interaction within the SEM. The electron beam can penetrate um of material releasing secondary particles along its path [239].

Auger electrons are only sometimes released instead of a photon when core holes are filled from higher levels. Their kinetic energy is equal to the hole filling transition energy minus the ionization energy of the atom. This makes them very useful for elemental composition of samples on the near surface, like characteristic X-rays, however unlike X-rays they cannot travel

from the bulk of the samples. Both are used in X-ray photoelectron spectroscopy (XPS) for probing core level states since their energy is element specific and distinctly defined by the energy levels which are involved in the Auger process. The collected Auger electrons are labelled using X-ray notation, for example, a KL_1M_1 Auger electron is a result of a hole in the K shell (1s) being filled from the first L subshell (the 2s orbital) and an Auger electron is ejected from the first M subshell (M_1, or the 3s orbital).

Secondary electrons of interest are typically low in energy (<50eV) and their trajectories are therefore easily altered by the presence of electric and magnetic fields. The detection of these electrons is performed using an Everhart-Thornley detector, which consists of a lightly biased (300V) grid over the surface of a scintillator crystal to attract free Secondary electrons. These electrons are converted to photons in the crystal and coupled out to a photomultiplier tube and electronically sampled. The sampled intensity is then used to map a grayscale intensity to a pixel. To gather a complete image of the surface needs to be sampled for each pixel.

The intensity of the collected electrons is a function of the detector position relative to the surface of the sample, the work function of the material itself, and the accelerating voltage of the primary beam. Contrast in the greyscale image can therefore be an indication of composition changes as the work function changes from one material to another. Backscattered electrons (BSE) may also be used to generate contrast since the scattering cross section is dependant on the elements atomic weight, however they are significantly higher in energy (50%-80% of primary beam energy) and can originate deeper than Auger or Secondary electrons. They are therefore not useful for high resolution imaging, but the image contrast in BSE measurements can be used to distinguish elemental composition based on atomic mass.

Characteristic X-rays are also released from the core hole transitions in the sample and can be used in energy dispersive X-ray spectroscopy (EDX) measurements. Since X-rays can penetrate significantly more material than electrons, these X-rays can originate from um of depth from the surface and cannot be used to map elements but can be used to sample the composition of bulk layers. The Oxford Aztec EDX equipped in this work can measure 0-20KeV with 0.124KeV resolution.

In this work Secondary electron images will primarily be used to measured dimensions of surface pits and layer thicknesses from prepared cross sections. While the SU-70 SEM does have a BSE detector, the resolution is low and may only be used to verify film boundaries.

6.3 Atomic Force Mircoscopy (AFM)

The AFM is an extremely useful tool for characterizing the surface of instruments. It can be considered a blind microscopy technique, where a probe, laser, and feedback electronics are used to sense the surface. A basic outline of the system can be seen in Figure 42.

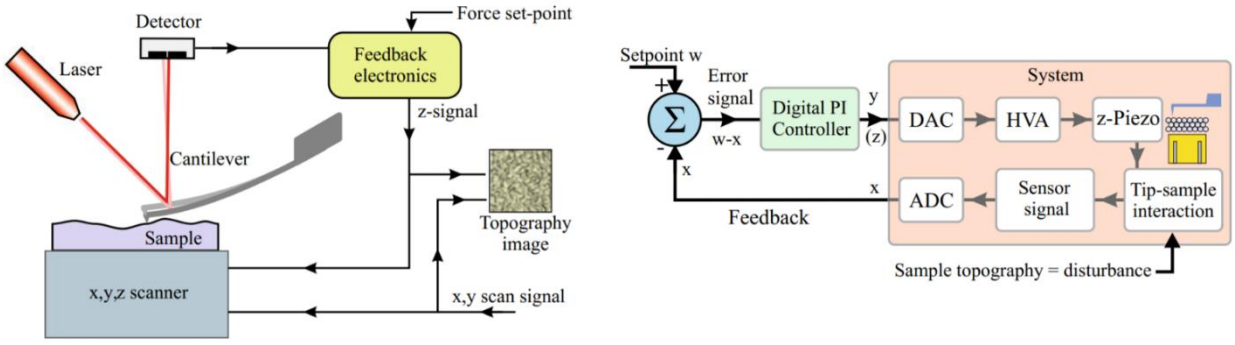

Figure 42: Overview of AFM system (left) and the feedback system (right). The error signal used determine height is generated by monitoring the tip sample interaction with a laser and maintaining the setpoint through the high voltage amplifier (HVA) and piezo element [240].

The probe itself is made from silicon bulk wafer, shaped into a cantilever with predetermined length and width depending on the desired application. The dimensions of this cantilever are usually on the order of 100's of μm in length and 10's of μm in width with at tip radius of <10 nm. The tip is located on the bottom of the cantilever, analogous to a record stylus. Stepper motors and piezo elements precisely lower the tip towards the sample until the feedback system monitoring the tip sees a change in either its deflection or resonant frequency, depending on the operating mode.

Two types of measurements are employed using the AFM, a contact mode where the static tip deflection is measured, and non-contact mode where the oscillation amplitude is measured. Both modes work on the same principle, a set point is given to the PI(D) controller in the feedback system and the piezo element will control the tip-sample distance to maintain the set point as the probe is scanned across the sample. The set point is either a force (usually in nN) or a % of the free vibration amplitude. The x-y scanning system moves the probe over a predetermined area as the feedback adjusts the height of the probe to maintain the set point.

Contact mode operates in region 1 of the force distance curve seen in Figure 43, where the interaction is repulsive from the surface. Non-contact mode operates in region 2 were the forces are attractive towards the surface. Contact mode offers a higher sensitivity to surface features since the slope of this curve is significantly higher in region 1, and the inorganic materials imaged in when analyzing semiconductor surfaces are not easily damaged from the tip. A noncontact mode is used on soft samples where applied force may damage or deform the sample. In this case the loading of the cantilever due too attractive surface forces acts to shift the resonant frequency of the cantilever and a loss of vibration amplitude is sensed when driving it at its free resonant frequency.

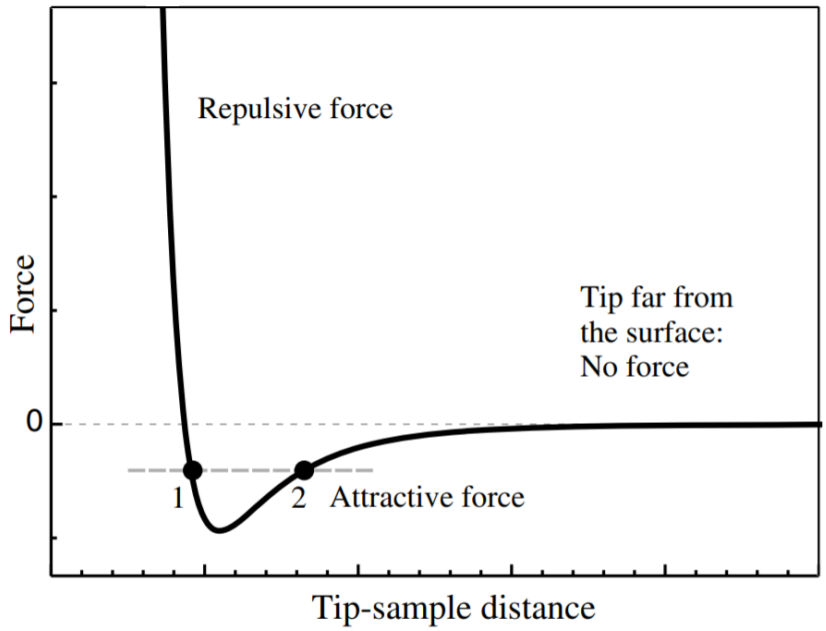

Figure 43: Force-distance curve showing the operating regimes of (1) contact mode and (2) noncontact mode. In both cases the force is attractive towards the energy minimum, but the slope of the curve is drastically different [240].

6.3.1 AFM Analysis

The elevation data is gathered from the error of the control loop, therefore convoluted by the PI(D) controller response and tip sample interaction characteristics. Both can have a significant influence on the image of the surface. The PI(D) settings should be set to avoid slow step response and ringing on surface steps and probe tip should be exchanged when the tip becomes worn or broken.

The data gather is a (usually) square matrix of height values that the z-controller needed adjust to maintain the set point. An RMS value (σ_{RMS}) for this is given as a statistical measure of the surface roughness calculated in the same way as a discrete time domain signal. The RMS of the surface can be calculated as:

$$\sigma_{RMS} = \sqrt{\frac{1}{N}\sum_{n=1}^{N}|z_n|^2} \tag{6-2}$$

Where N is the total number of points in the array and z_n is the height measured at point n. The summation can be done in any order for the set of data, since the RMS value only looks at the spread of the heights and does not consider lateral dimensions. This leaves it as a somewhat ambiguous description of the surface since any RMS value found can be represented by a sine wave which will not represent the measured surface. The RMS roughness should therefore not be blindly considered as indicative of surface quality.

6.4 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a surface characterization technique used to probe to elemental composition and core energy levels of near surface atoms. Similar to the X-ray tube used in XRD, the XPS performs the reverse process, to releasing characteristic electrons using X-rays. The XPS uses a monochromatic X-ray source (Al Kα = 0.83401 nm) to excite core electrons to vacuum. The electrons travel into a hemispherical analysis chamber where a a magnetic field curves their trajectory. The curvature of their path is proportional to their energy. The energy of the electrons comes from the energy of the X-ray source minus the ionization energy of the core state.

The photon in/electron out nature of the measurement makes it strictly a surface measurement. The core energy levels can be deduced by examining the energy spectra of the characteristic electrons collected. Auger electrons are also released from higher core levels as explained in section 6.2 Scanning Electron Microscope (SEM). Minor shifts in the core energy levels occur from the local bonding of the atom can be detected to determine the nature of bonding.

The XPS is useful for its surface selective analysis and its insight into the chemical bonding present. It is relatively new to the Lakehead University Instrumentation Lab (LUIL) Instrumentation Lab and was not available for all samples.

7. Experiments

Experimentation is still a critical step in characterizing a device processing. Due too the large number of atoms involved in a macro scale devices and large number of process variables interacting during device fabrication, a complete ab initio approach to device design is not currently feasible. Computational tools are split into many different applications applications such as material modelling (chapter 5) at an atomic scale, finite element methods, and statistical analysis on large data sets.

Sapphire serves as a baseline for the experiments in this work. For the sake of comparison all measurements done on ceramic samples will be contrasted to the same films on sapphire. The recipes for these growths were developed using results from our high temperature (700 °C in our system) growth conditions.

7.1 Sapphire Growth

The environmental variables that can be controlled in our system include system pressure, temperature, precursor flow rate, plasma power, and precursor exposure time. Migration enhanced epitaxy systems works by first introducing the metal species followed by nitrogen. The III/V ratio is not completely the same as traditional systems since they are not present in the chamber at the same time. The growth is instead divided into repeated cycles of group III rich conditions immediately separated by group V exposure. The III/V ratio is controlled by the relative time of these two exposures in a growth loop. It is generally desirable to have a high growth rate per hour, so these cycles are ideally as short as possible.

7.1.1 Temperature

The temperature should be as high as possible to increase surface diffusion effects in all cases. The highest possible temperature in these experiments is set by the softening of the ceramics at 700 °C. If ZnO is coated on the sample the upper limit is set at 650 °C to avoid decomposition and contamination.

7.1.2 Pressure

The pressure is controlled from the downstream throttle valve in Figure 24 and the PV3/MFC3 lines in Figure 25. The limiting factor for growth rate in this system is the rate at which nitrogen radicals can be provided to the substrate. The trimethyl flow rates can be adjusted through the mass flow controllers and their injection time can be used to vary the dose of Ga in any growth loop. The plasma head has a maximum power output of 600W which cannot be further increased. The species of nitrogen reaching the substrate is therefore determined by the pressure in the system. If the pressure is too low however, not enough nitrogen molecules are passed through the plasma head. The power output of the head is also observed to decrease as the plasma current is lowered. If the pressure is too high the excited plasma species can collide to recombine or relax before reaching the substrate. This can be observed visually through the reactor viewports or measured with a spectrometer.

While is it possible in this system to dynamically vary the pressure during growth by adjusting the throttle valve position, it generally takes 10-30 seconds to reach steady state on the PI controller which can significantly reduce the growth rate per hour if performed twice per loop. A single pressure was therefore chosen as the operating pressure for the growth. In order to determine the optimal pressure a series of growths were performed varying the pressure from 350

mTorr to 1600 mTorr with the otherwise same recipes. The variation in AFM roughness and XRD FWHM can be seen in Figure 44.

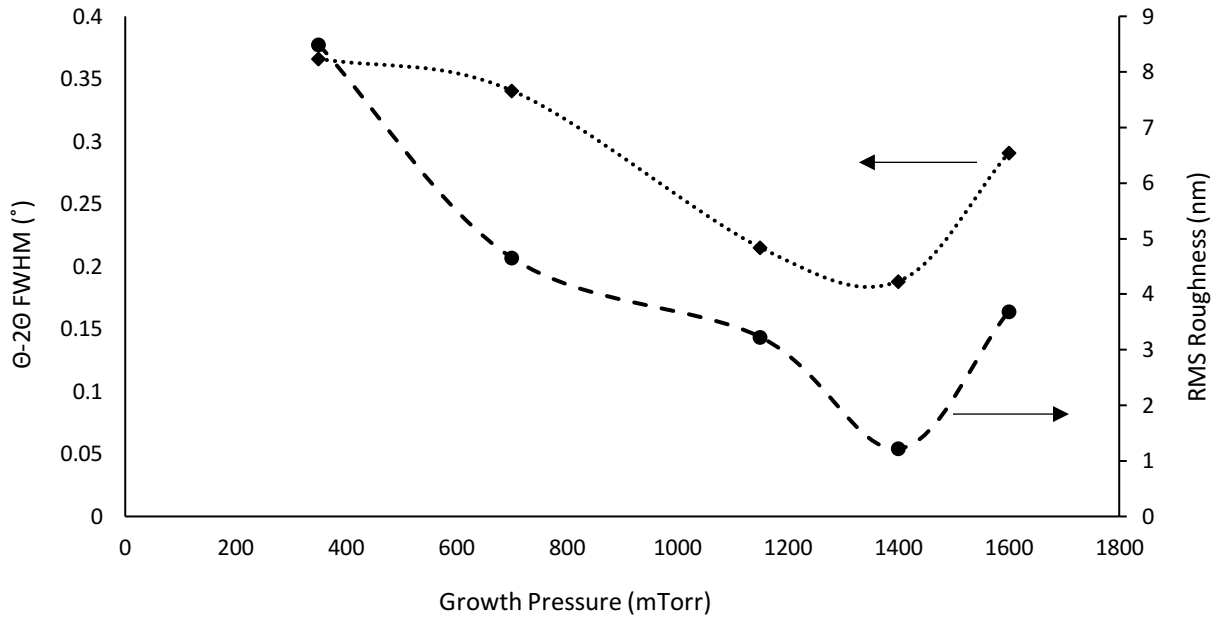

Figure 44: (0002) GaN Θ-2Θ FWHM and surface roughness as a function of growth pressure in our system.

Based on these results the optimal growth pressure was determined to be 1400 mTorr. A similar effect can be seen on the surface roughness in Figure 44. The pre and post growth AFM image can be seen in Figure 50. The bare wafer on the left exhibits an extremely smooth surface with only 57.83 pm roughness, while post deposition is rougher at 1.219 nm. The increased roughness is greater than a monolayer (~0.5 nm) and is observed to be granular. This can be attributed to a partial VW type growth where island growth is occurring. To further decrease the roughness additional migration energy needs to be supplied to the system, without significant heating of the substrate to avoid melting.

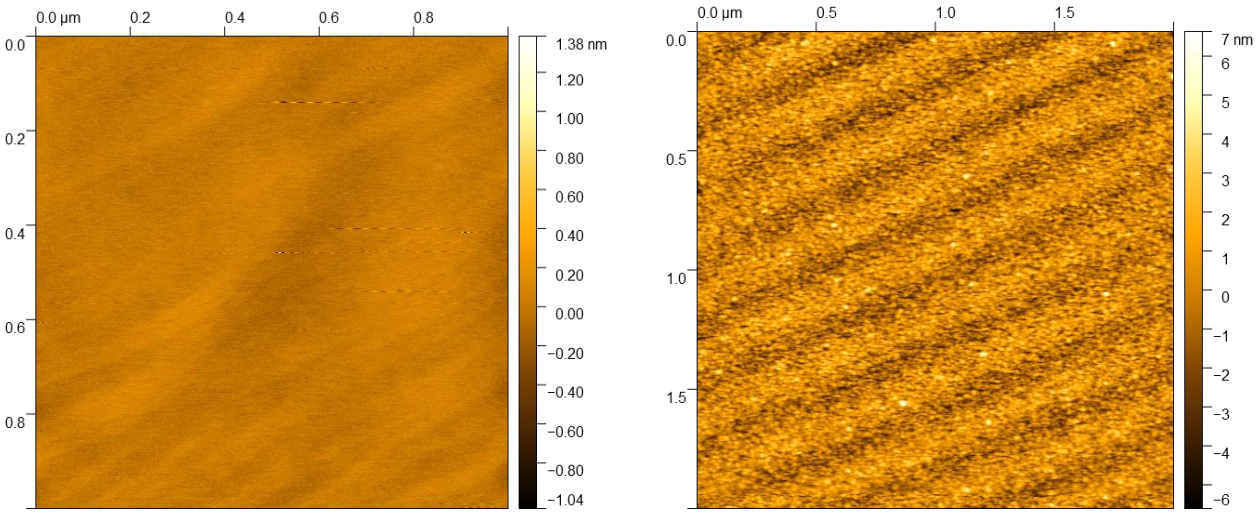

Figure 45: AFM surface image for the bare sapphire wafer (1x1 µm, left) and 700 °C post growth surface (2x2 µm, right). The measured RMS roughness changed from 57.83 pm (left) to 1.219 nm (right).

A decrease in the temperature can be expected to decrease the observed FWHM and grain size and increase the surface roughness by lowering the migration distance of surface atoms.

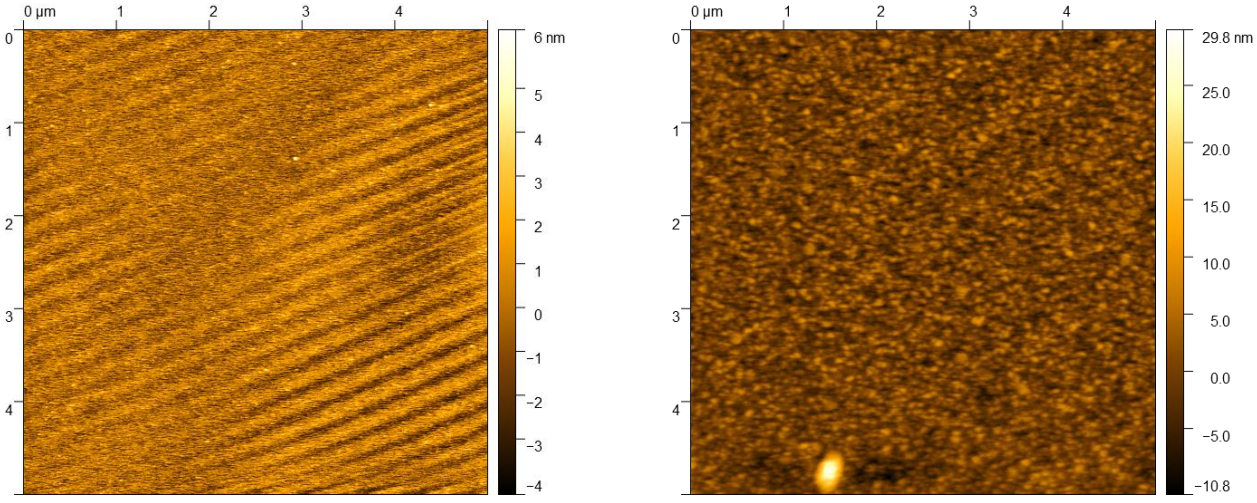

Figure 46: AFM surface image for the 700 °C sapphire deposition (5x5 µm, left) and 650 °C post growth surface (5x5 µm, right). The measured RMS surface modifying the roughness from 1.219 nm (left) to 2.891 nm (right).

7.1.3 Precursor Flow Rate

The trimethyl precursor flow rate can be used to control to group III dose per cycle. The duration of the cycle should be kept as short as possible to increase the growth rate per hour, therefore a lower limit for the durations is desirable. The lower limit in this system is 4s, below

this the flow rate was not able to reach a steady state condition on the system monitor. The precursor flow rates are measured in standard cubic centimeter per minute (sccm) by the mass flow controllers (MKS Instruments 1179/1479/1640A, MFC1-8 in Figure 25). The flow measurement is based on differential heat transfer between temperature sensing heater elements which are placed symmetrically in the sensor tube. The system monitor reads a 0-5 VDC signal which is proportional to the mass flow by the specific heat capacity and the density of the gas used in the line (nitrogen in this case) and needs to be calibrated for different carrier gases. The initial experiments above were performed at 0.5 sccm, resulting in an average deposition rate of 0.153 nm/cycle, lower than the 0.25-0.26 nm/cycle expected from monolayer deposition. A BSE image was used to see the contrast of the film layer with the substrate (Figure 47).

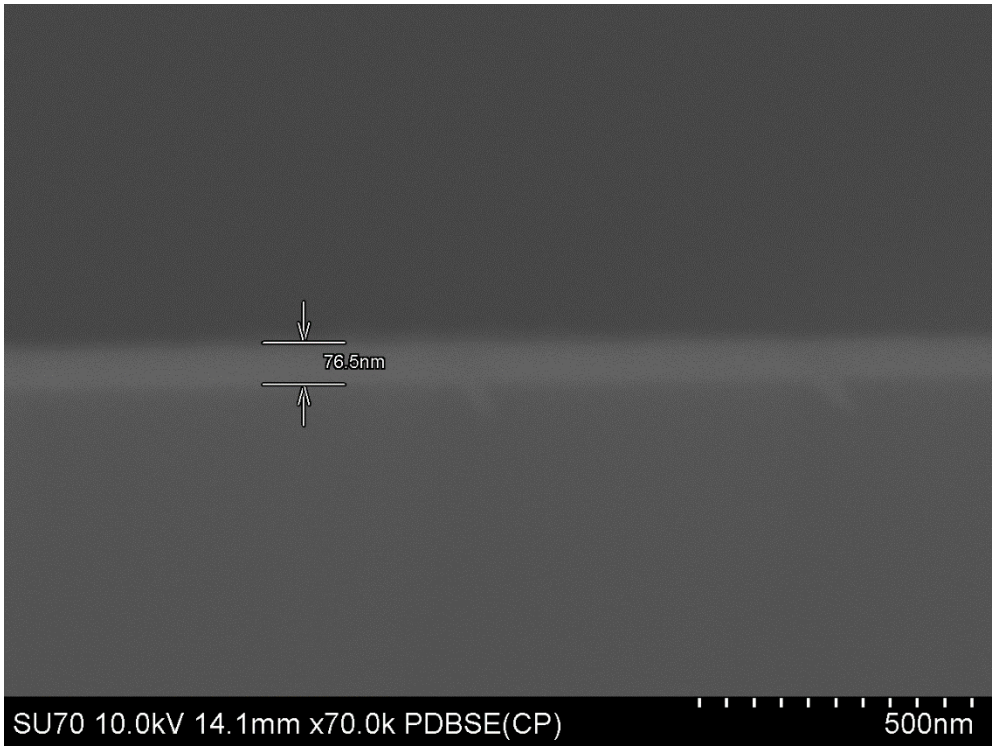

Figure 47: BSE Image of GaN sapphire growth at 700 °C, 1400 mTorr, 0.5 sccm flow rate.

The precursor flow rate was increased to 1.0 and 1.5 sccm with otherwise same recipe as above (Figure 47) to observe the effect on the growth rate and XRD FWHM. Figure 48 summarizes the results.

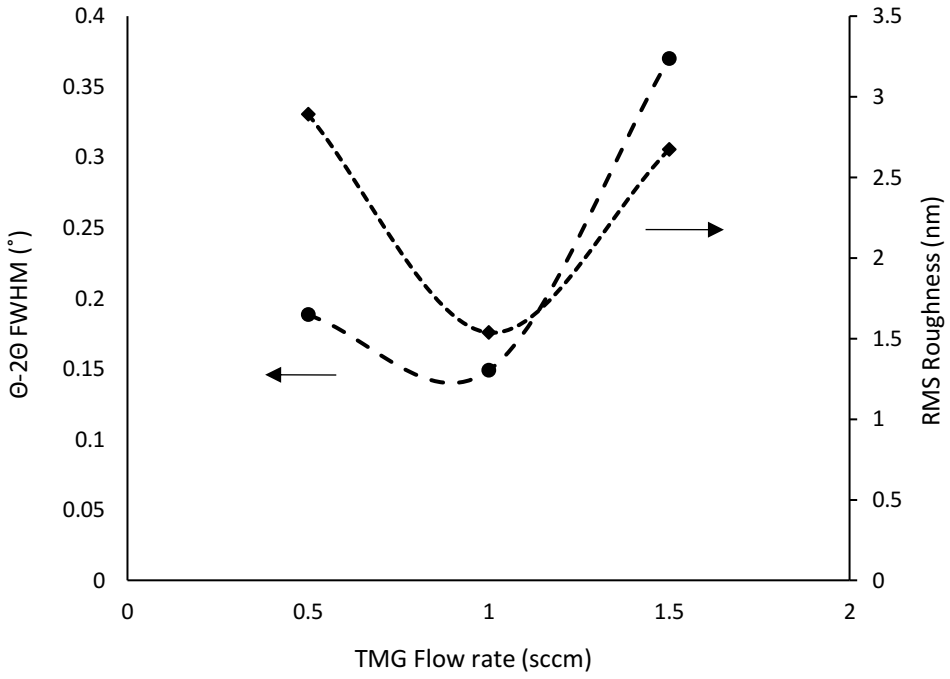

Figure 48: Effect of varying the TMGa flow rate on the Θ-2Θ FWHM and RMS roughness.

The increased flow rate was observed to slightly decrease the RMS roughness and Θ-2Θ FWHM. The growth rate increased from 0.153 nm/cycle (Figure 47) to 0.26 nm/cycle at 1.0 sccm. Based on these results a 1.0 sccm 4 second dose was taken as the group III portion of the growth loop.

The plasma power was kept at 600 W in all cases. The duration of the plasma exposure should be minimized in the recipe design, after the complete nitridation of the group III atoms additional nitridation is unnecessary. Insufficient exposure per cycle will result in metal accumulation in the growth, increasing surface roughness, possibly introducing Ga metal peaks or

polycrystalline GaN peaks into the XRD. Figure 49 shows the effect of decreased plasma duration in the system.

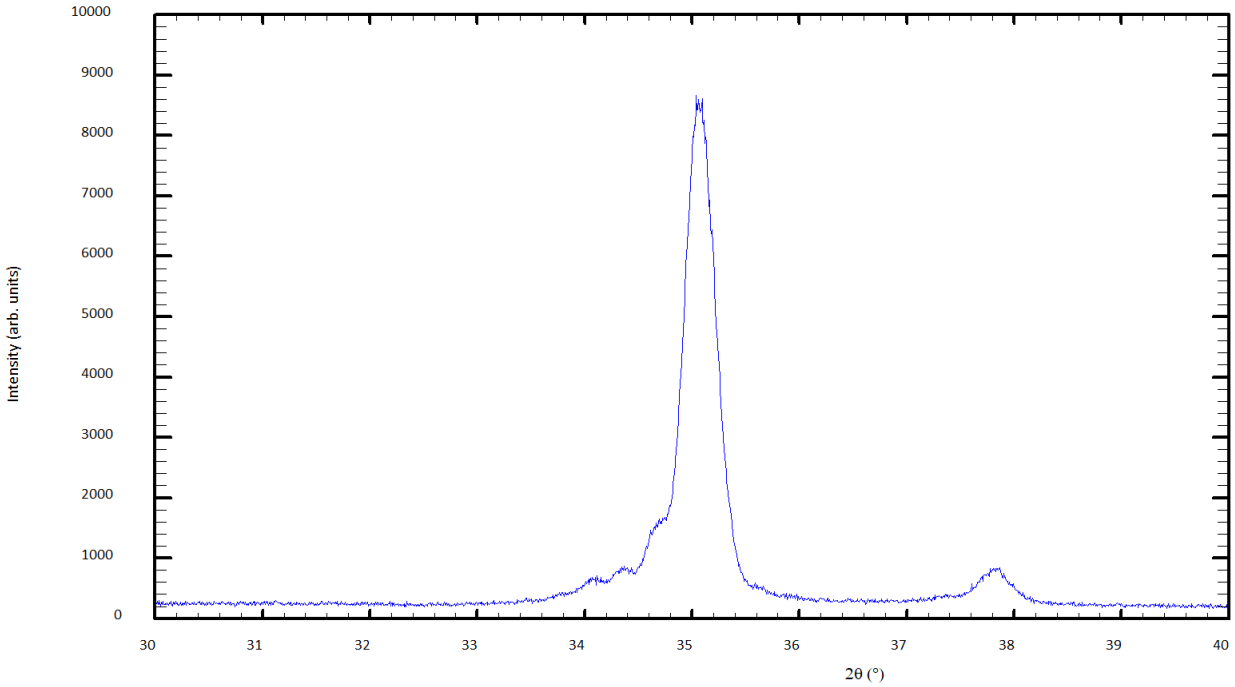

Figure 49: A decrease in plasma duration is observed to decrease the XRD peak quality and introduce additional polycrystalline peaks.

7.1.4 Conclusions

A plasma exposure of 8 seconds was found to give the best results based on the analysis of Θ-2Θ XRD patterns. The optimal growth loop is therefore found to be 4s exposure of TMGa followed by 8s of nitrogen plasma. The optimal growth pressure was found to be 1400 mTorr. The maximum temperature is taken to be 700 °C based on the observed softening of the LTCC. This recipe was applied to the oxide coated samples at their appropriate temperature.

7.2 Ceramic Properties

The properties of the deposited films are examined through many different techniques. Additional measurements not covered in section Instrumentation were performed by research partners in some cases for the purposes of publication.

7.2.1 Ceramic Composition

The ceramics used in this work are the Heraeus CT700 series. X-ray diffraction and energy dispersive X-ray spectroscopy (EDX) data for the bare substrate can be seen in Figure 50 and Figure 51.

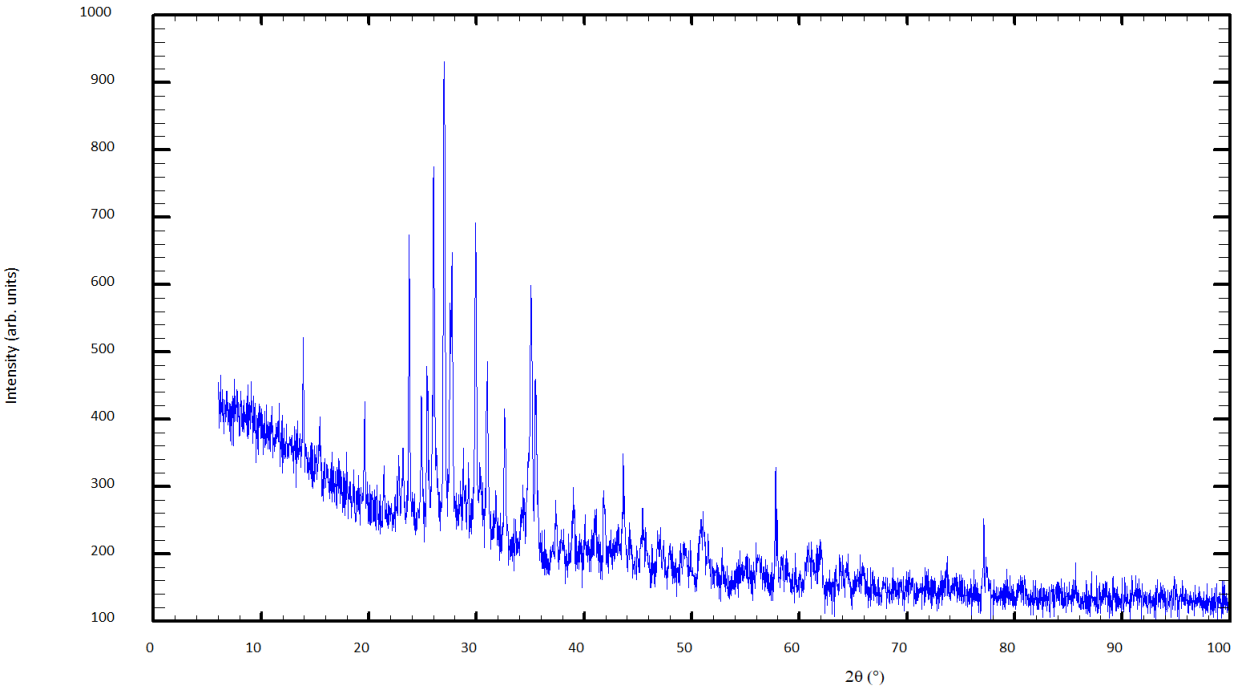

Figure 50: XRD spectra of bare ceramic substrate. The significant number and sharp distribution of peaks indicates a non oriented multiphase mixture is present.

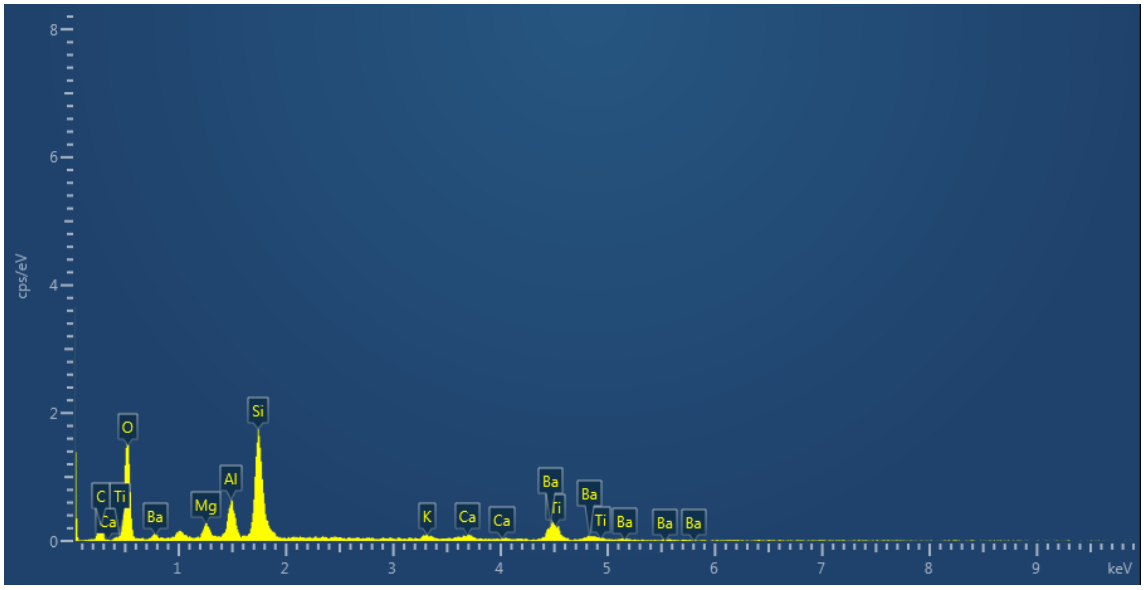

Figure 51: EDX spectra of the bare ceramic. The EDX gives an elemental analysis of the sample based off characteristics X-ray energies.

The EDX is useful for probing the composition since it samples the bulk volume, showing the ceramic to be a mixture of Ca, Ba, Ti, K, Mg, Al,Si, and O. The XRD confirms there are several crystalline phases present in random orientations. To rightfully perform a quantitative analysis of these peaks the intensity needs to be compared to standard sample with known composition. The relatively high intensity of the oxygen and silicon EDX peaks however is indicative of the modified glass matrix model for the ceramic. The relatively weak XRD spectra shows only a small amount of the ceramic is crystalline material. The surface may therefore be considered a network of amorphous oxides with some crystalline inclusions.

7.2.1.1 Surface Roughness

The morphology of the surface can be seen from atomic force microscope scans of the surface combine with SEM cross section in Figure 52.

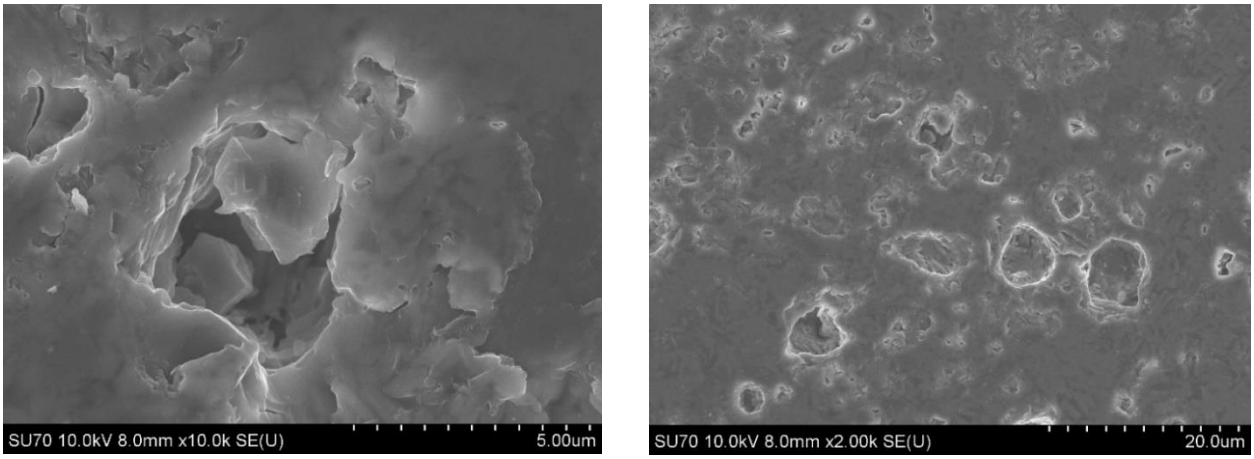

Figure 52: SEM surface image of the bare ceramic. Two distinct pit sizes are visible in each scan, originating from different processing in the ceramic.

Two distinct pore features can be identified. Large surface pits up to several microns in size are a result of filler particles that were removed from the surface during the polishing process, while the smaller pits are a result of void formation in the sintering process. Both are largely unavoidable for the polishing process, as more voids are continuously generated as polishing continues. The

larger pits present a more significant challenge since many microns of material will be needed to fill them.

7.3 Oxide Properties

The effect of oxide deposition on LTCC surface is investigated here. The surface texture of the LTCC refers to the crystal structure facing the surface.

7.3.1 Surface Texture

In the case of silicon dioxide and anodic alumina no crystal texture is introduced to the system since these layers cannot be annealed without melting of the ceramic. For ZnO, annealing can be done at <600 °C and a (0002) WZ surface can be observed under optimal dipping conditions. The effect of repeated dips on the (0002) peak properties can be seen on a log scale in Figure 53. The trend shows a clear increase in the ZnO (0002) peak height with increasing thickness.

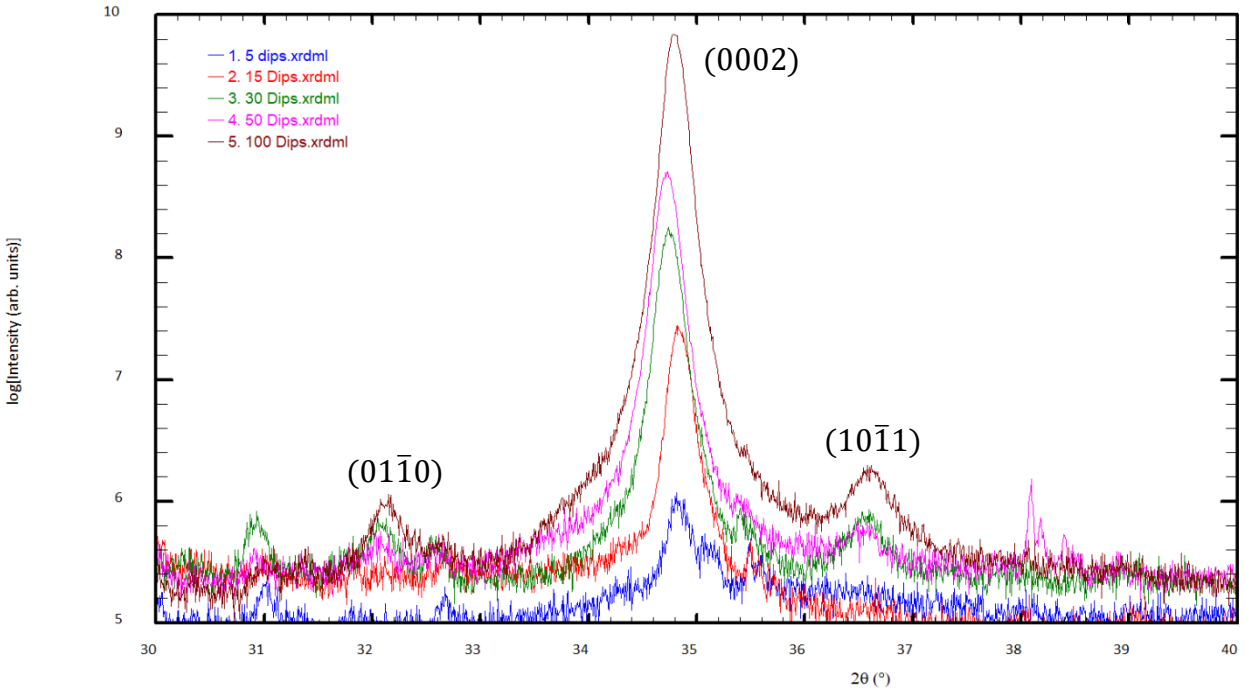

Figure 53: Semilog plot showing the evolution of the $(10\bar{1}0)$, $(10\bar{1}1)$ and (0002) peaks of ZnO on LTCC. The strain free positions of these peaks are 31.7768˚, 36.2638˚ and 34.433˚ respectively with a=3.249 Å and c=5.205 Å.

The FWHM of each of these peaks and the position of the (0002) peak is given in Figure 54. The position of the peak changes from uniform biaxial strain in the layers, which deforms all in d spacings the same on average. The strain free position of the (0002) peak should be 34.433˚ at based on lattice constants of a=3.249Å and c=5.205Å for ZnO.

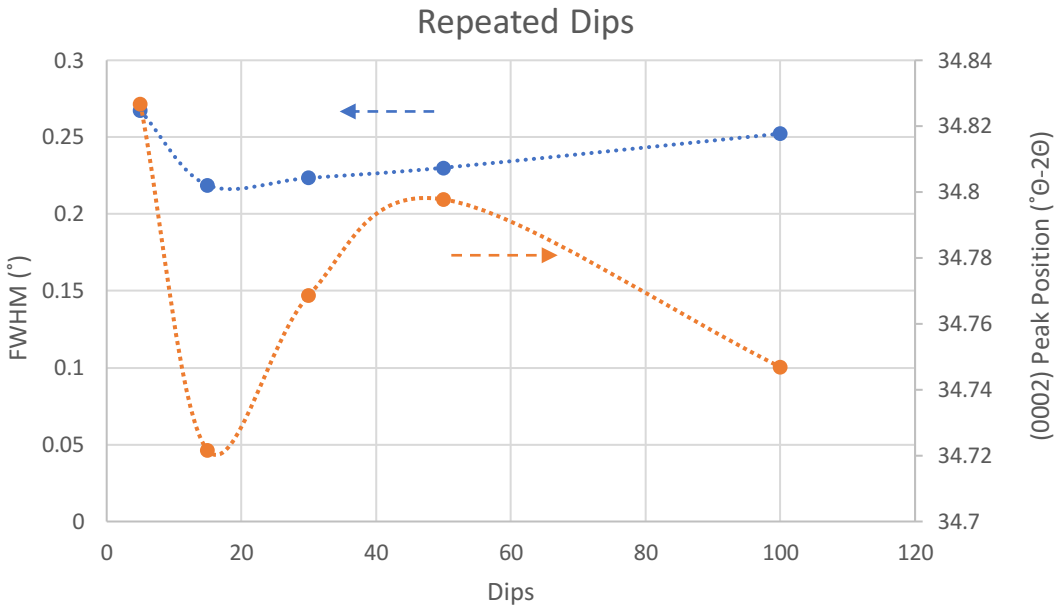

Figure 54: Plot showing number of the effect of subsequent dips on the (0002) *peak position to observe lattice strain and FWHM to observe the change in ordering along the c-axis.*

Repeated dips show a shift of the XRD peak towards the relaxed value. This indicates a reduction in the uniform strain in the layer, which is due to the thermal expansion mismatch with the substate. Beyond the initial 5 dips we can observe almost an order of magnitude increase in the peak height between each data point, with little change in the FWHM. It is important to remember this is measuring vertical strain gradients and micro strain that causes a spread of {0002} planes. The lack of improvement in the FWHM indicates the strain gradients are not a function of the total layer thickness and are likely related to the annealing of the ZnO nanoparticles.

7.3.2 Surface Roughness

7.3.2.1 ZnO

The surface roughness of the bare ceramics was measured to be 116.2 nm in Figure 55.

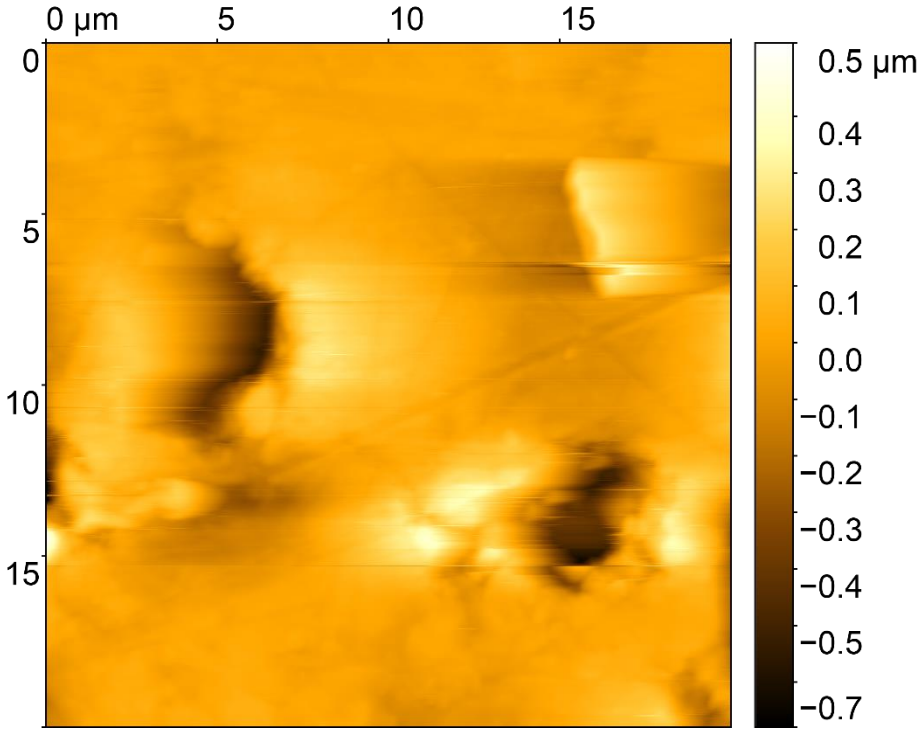

Figure 55: 20x20 µm² AFM scan of the bare ceramic. The measured surface roughness including the pores is 116.2 nm.

AFM scans and SEM cross sections of 5 repeated dips and 115 repeated dips are shown in Figure 56. A cross section of a surface pit can be seen in Figure 58. The pit can be seen to be significantly larger than the layer thickness of 654 nm. The evolution of the layer thickness can be seen in Figure 57.

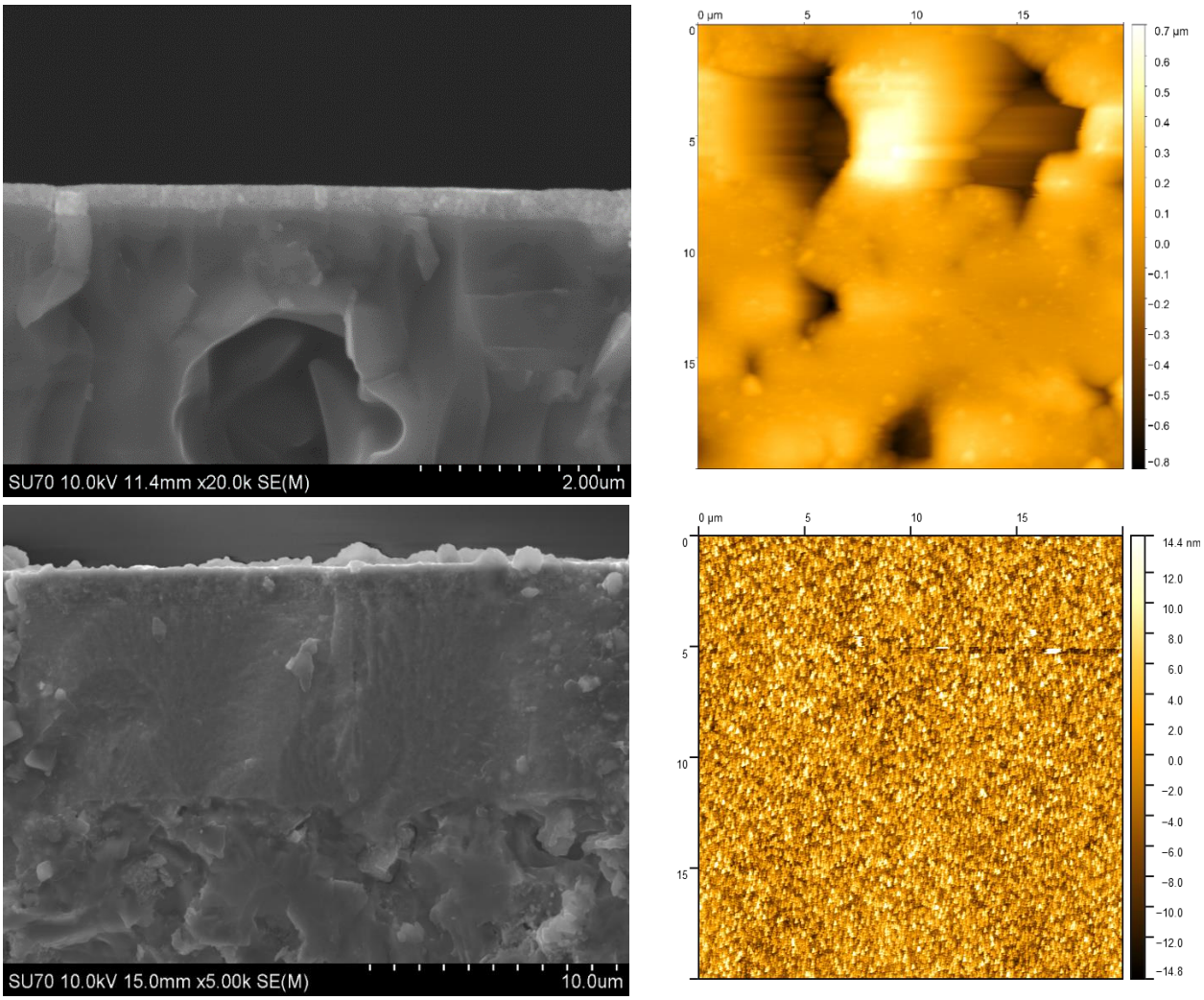

Figure 56: SEM cross section and AFM surface scans of ZnO dip coated samples. The upper two images represent 5 dips, while the bottom is 100.

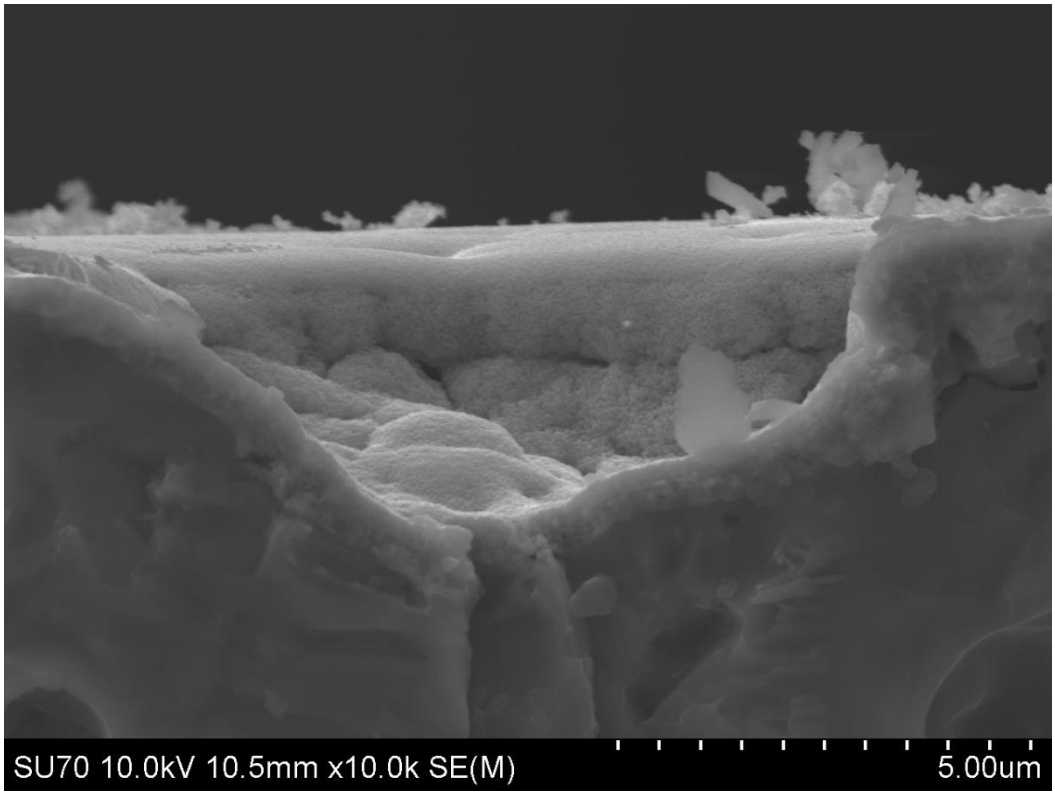

Figure 58: SEM cross section of a surface pore after 15 coatings. The layer thickness is measured to be 654 nm.

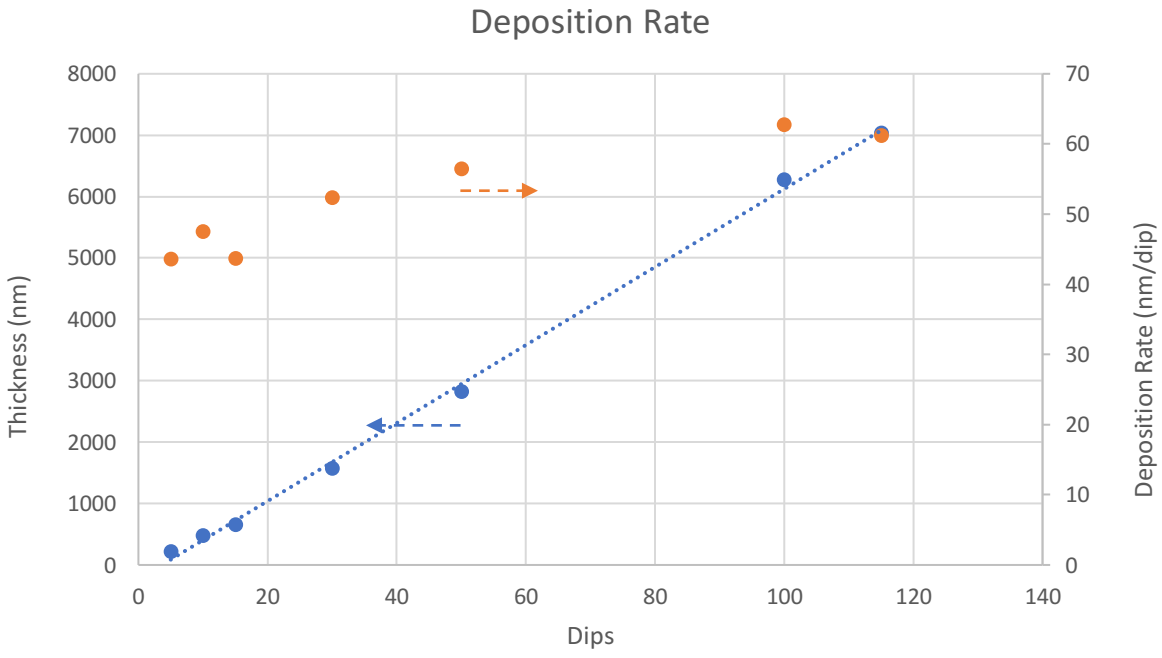

Figure 57: Dip coating thickness and deposition rate based on total number of dips. The average per dip is seen increase with a greater number of dips.

The final thickness of the layer was found to be linearly proportional to the number of depositions even up to 115 dips, indicating consistency between dips. The average deposition rate was seen to slightly increase as the thickness increased, likely due too evaporation from the dip coating reservoir. Evaporation of alcohol from the reservoir leads to an increase in the solution concentration, increasing viscosity and the volume fraction upon evaporation leads to an overall increase in deposition rate. This is difficult to prevent since the bath must remain open for dipping. A possible solution to this may be to decrease the temperature of the bath, however viscosity will also decrease and the optimal dip rate in this case will change.

RMS roughness was calculated over a 10x10 μm^2 area on 5 randomly selected spots on the surface for averaging surface roughness. Figure 59 shows the results of the AFM measurements as a box plot.

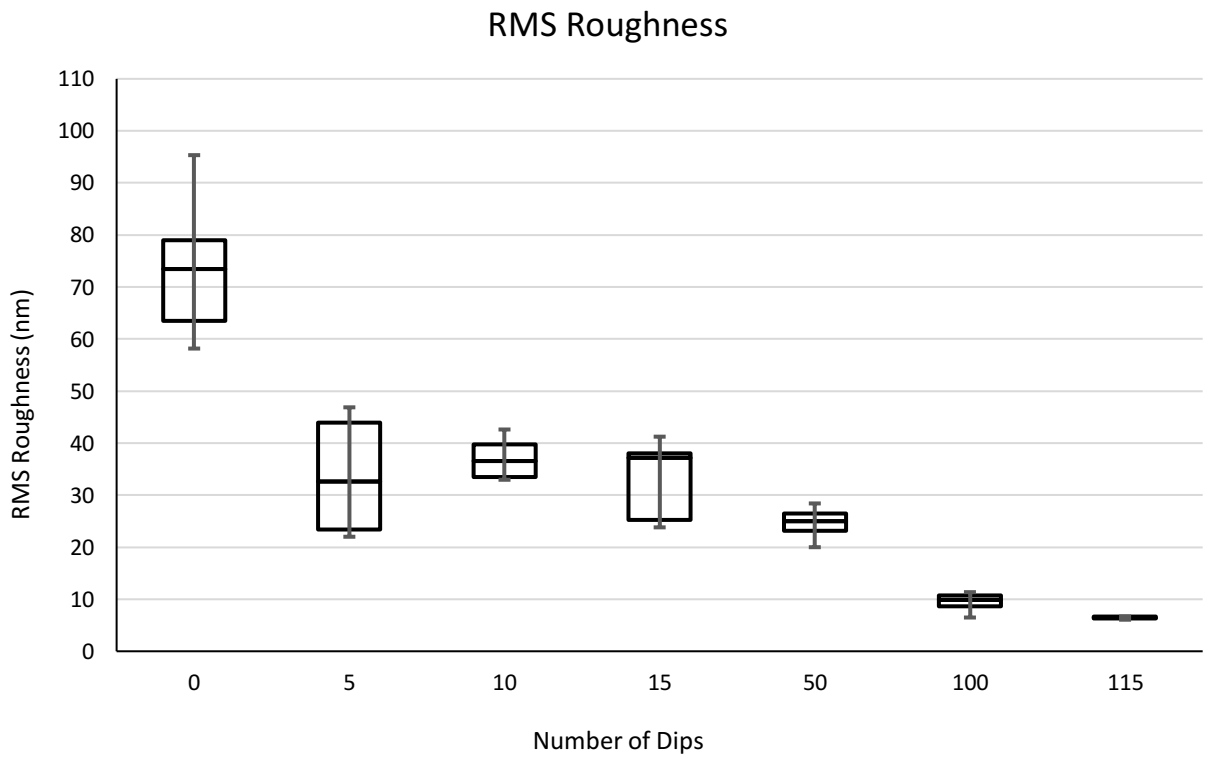

Figure 59: Box plot of the surface roughness as a function of dip counts. Each of the boxes is determined from 5 measurements of randomly chosen spots on the surface.

Imaging of the deep surface features in our AFM systems was difficult without introducing artifacts in the image. In order to reduce error due too including these in the calculations a mask was applied to each image to ignore features greater than 150 nm below average plane.

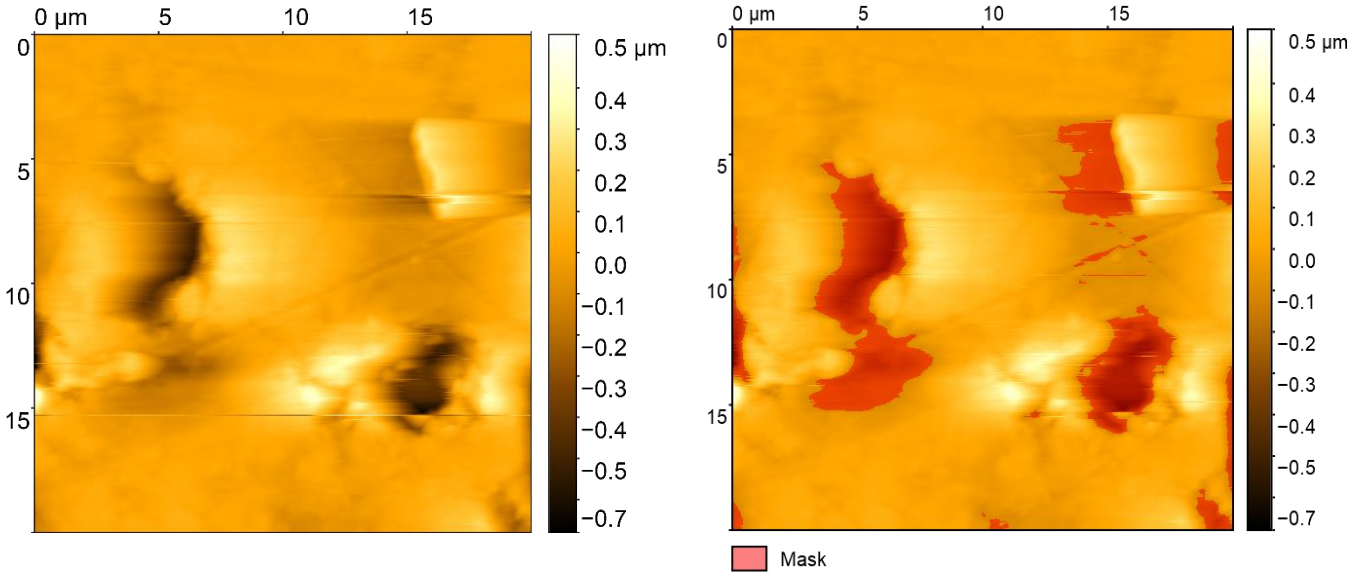

Figure 60: Masking of the AFM data to determine porosity and reduce pit induced errors in the data.

Figure 60 shows the results of this masking procedure on the bare substrate. The relative area of the pit it taken as the porosity of the sample. The surface roughness in Figure 60b excluding the masked regions is 79.91 nm with a porosity of 87.9%. The results of the box plot in Figure 59 effectiveness of the ZnO layer to reduce the surface roughness of the samples as the thickness increases. The samples are observed to becomes more uniform in their coverage as the roughness becomes more consistent between measurements. Initially the ZnO has little effect because the layers are thin compared to the surface pits. As more material is deposited the pits are observed to fill and level out the surface. The surface pits were however still visible after 115 dips (Figure 61).

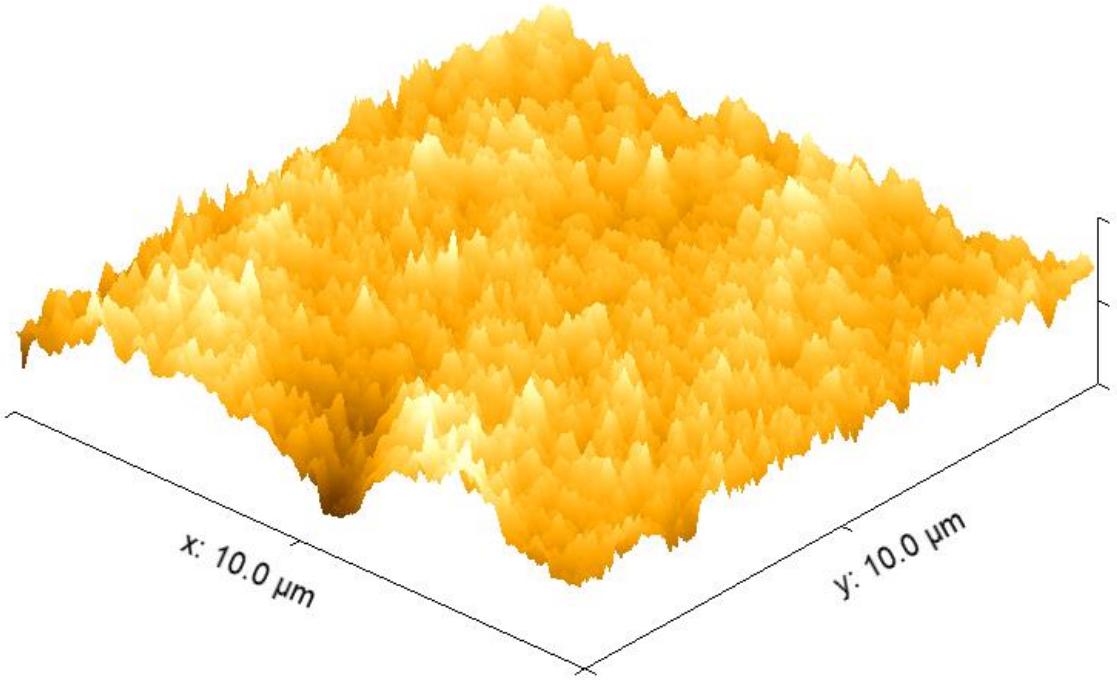

Figure 61: 3D AFM plot of 115 dips of ZAD sol gel solution. The micron scale pits on the surface of the ceramic can still be seen to influence the roughness of the layers despite a thickness of 7.1 µm.

The porosity of the layers as determined by the masking procedure can be seen in Figure 62. The decrease in the porosity is expected as the surface is filled. This graph may be somewhat misleading since the threshold was chosen arbitrarily. Features that do not fall in the pit criteria can still contribute to surface roughness and can still be seen on the surface (Figure 61 for instance is %100 filled, but a pit feature can still be seen on the x-axis).

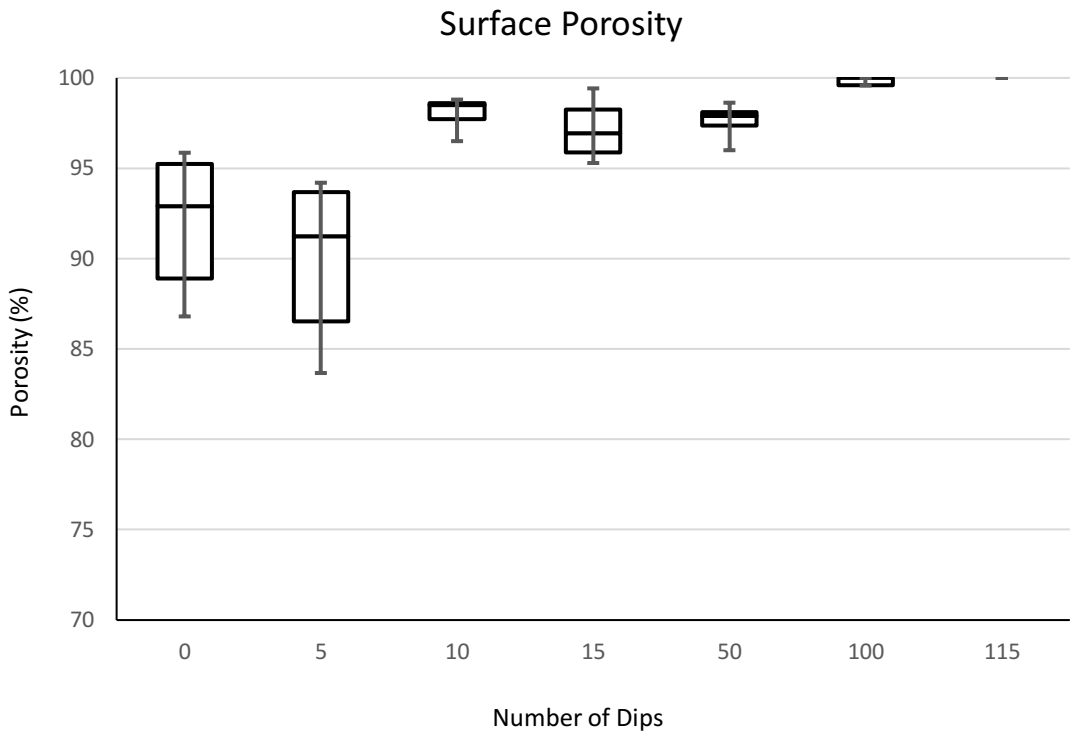

Figure 62: box plot of porosity determined form the arbitrary threshold masking done on the AFM samples. Surface features greater than 150 nm from the mean plane are taken as pit features.

7.3.2.1 Silica

The silica layers were deposited using a spin coating technique by partners at TU Ilmenau [72]. The samples were prepared using a hybrid dip coating method where 35 nm silica particles are mixed with the solution to increase the volume fraction of the deposited layer. Since these layers do not require crystallinity µm of material can be deposited in a single dip.

An AFM scan of the surface can be seen in Figure 64. The RMS surface roughness over 5 different samples was found to be 28.58 nm. Features of the underlying ceramic can still be observed in Figure 64, indicating thicker layers may be required. The amorphous silica layers were initially believed to be useful as thick surface filling layers, however annealing at 500 °C was observed to induce severe cracking in these samples due too the thermal expansion difference between LTCC and the silica.

30 dips of ZnO (~1.5 µm) were performed on these films despite the initial results. The cracking in these films was found to propagate through further deposited layers (Figure 65).

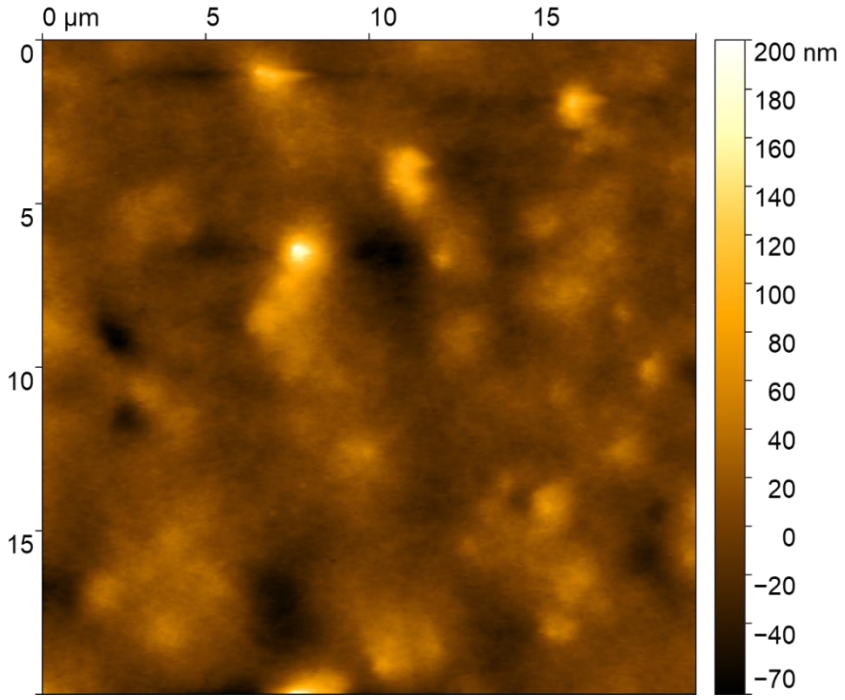

Figure 64: AFM scan silica coated LTCC. The RMS surface roughness over 5 different samples was found to be 28.58 nm

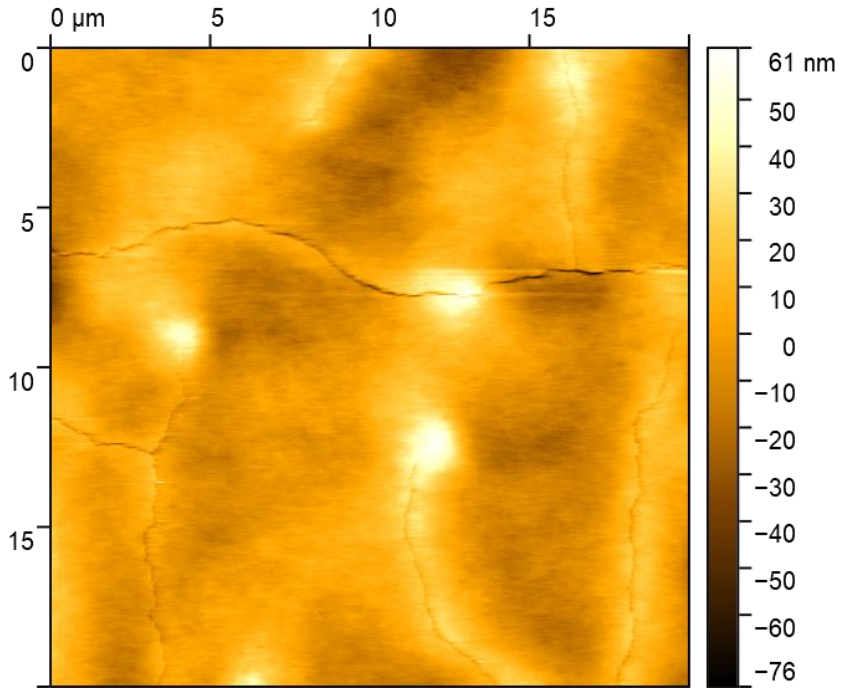

Figure 63: Silica sol gel samples annealed at 500 ˚C. Cracking can be observed in these layers due too thermal expansion of the substrate being higher than the silica layer.

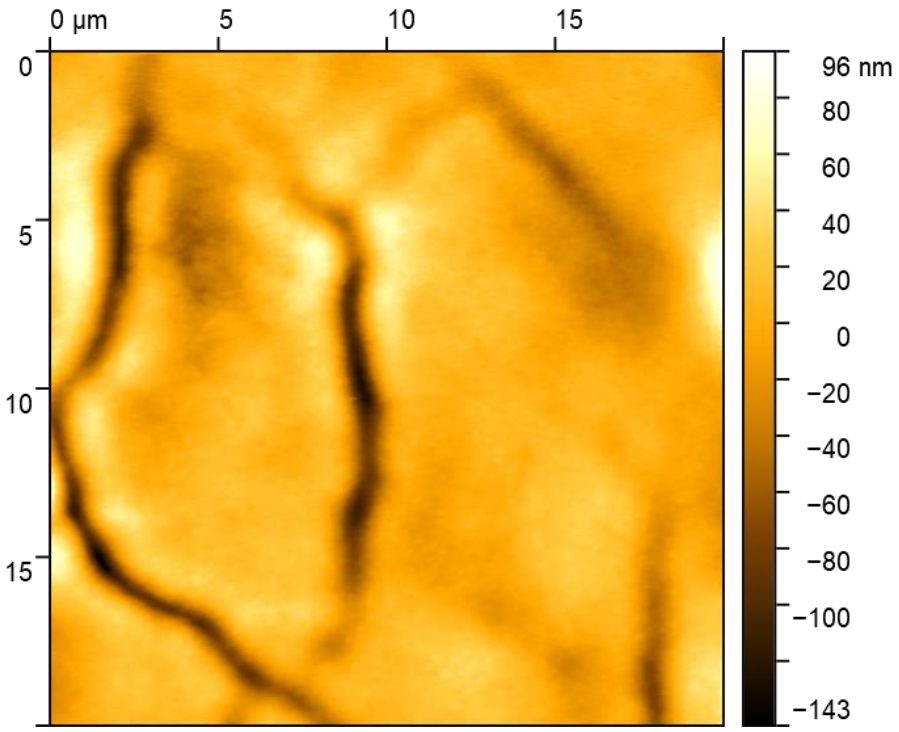

Figure 65: 1.5 µm thick dip coating layer on the silica sol gel.

The relatively low temperature cracking observed in these samples precludes them from being used as growth substrates in our system.

7.3.2.1 Anodic Alumina

The alumina surface was produced with partners at TU Sofia, Bulgaria. 500 nm of aluminum was initially sputtered on the surface. This metal coating was then oxidized using a solution of 4% oxalic acid at 40V DC at 15C. The thickness of the layer was chosen to ensure adequately low contact resistance, low thermal resistance to the ceramic and low internal mechanical stresses. Thick layers of aluminum could result in delamination of the film due too the volume expansion of the oxide as well as the difference in thermal expansion between aluminum and aluminum oxide. The low thickness required for the anodization on the ceramics does not allow for an electropolishing or pre cleaning in alkaline solutions step as the aluminum may

completely dissolve. For the same reason, a two-stage anodization cannot be performed under these conditions.

One of the significant drawbacks of these films is the top down process used to deposit the alumina. Since electrical contact is needed to perform the anodization it cannot be performed without depositing new metal to anodize.

The alumina layers produced under these conditions can be seen in Figure 66.

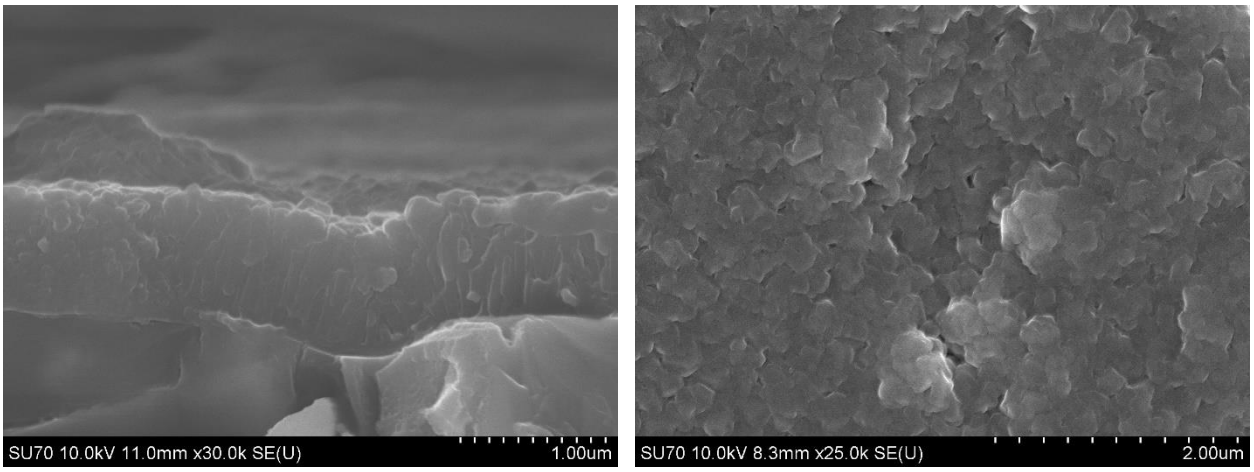

Figure 66: Anodized alumina film on LTCC cross section (left) and surface view (right).

The pore structure is visible in Figure 66 but is not as pronounced as layers observed in two stage anodized metallic samples. This is a consequence of the random crack nucleation that occurs in the one step process. In the cross-section view, vertical striations corresponding to the aligned pores can be seen to be perpendicular to the surface but are less visible from the surface images. This is again indicative of a random initial nucleation where the pore does not begin perpendicular to the metal surface. As the pore progresses the local stress and electric field aligns the pore perpendicular to the ceramic surface. A small pit feature can be seen in Figure 66 (left) being partially filled. It is clear from these results that elimination of the void structure would not be possible with these layers.

7.4 GaN Growth

Direct growth on the ceramics is expected to behave like direct growth on glass substrates, where many grains nucleate with many different orientations on the surface due too a lack of underlying order. An oblique view from the SEM can be seen in Figure 67. An estimate of the layer thickness in this case is not possible since it is difficult to define a layer on the surface.

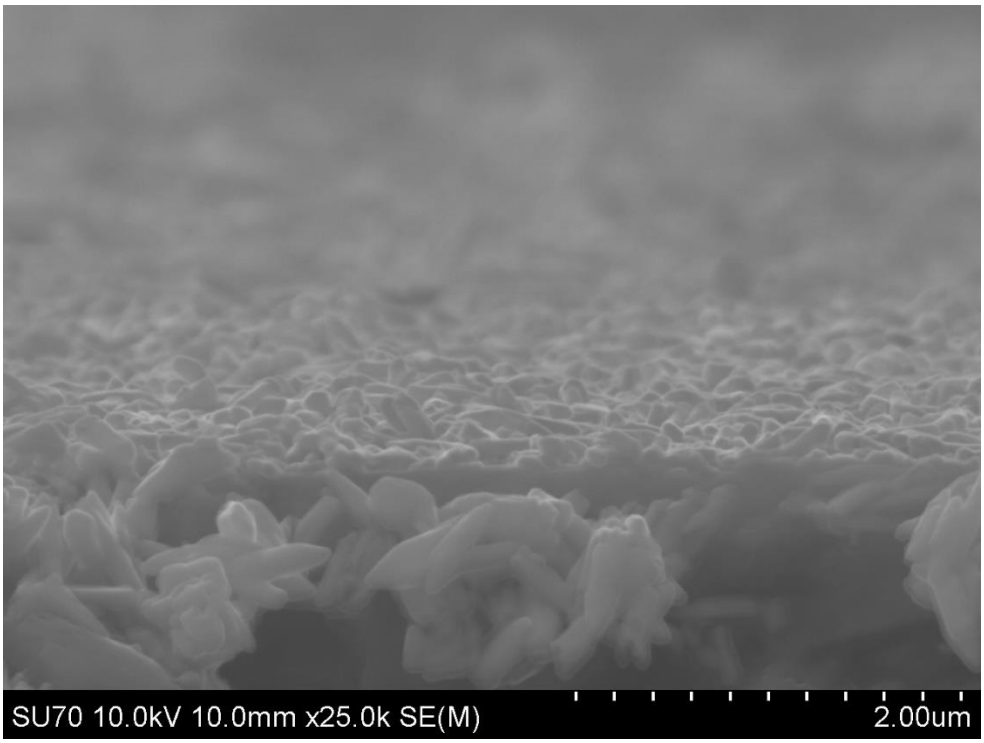

Figure 67: Oblique view of GaN growth on LTCC substrate with no layer in between, resulting in a dense network of misoriented crystallites.

Prior to deposition all samples were cleaned in the same manner. A 10-minute acetone ultrasonic cleaning followed by a 10 minute ethanol cleaning and a rinse with DI water is standard procedure on all samples.

7.4.1 Anodic Alumina

Anodic alumina results were completed in cooperation with partners at the university of Cádiz in Spain for publication [196]. Growth of the films was performed at Lakehead University, and electron microscopy was performed by our partners. During this time, the RF source was unavailable for powering the plasma head and a DC source was used. 700 °C was used as the growth temperature to avoid softening of the ceramic. An SEM cross section of a post growth layer is shown in Figure 68 after 3000 cycles. The approximate growth rate is 0.193 nm/cycle, slightly less than a monolayer per cycle.

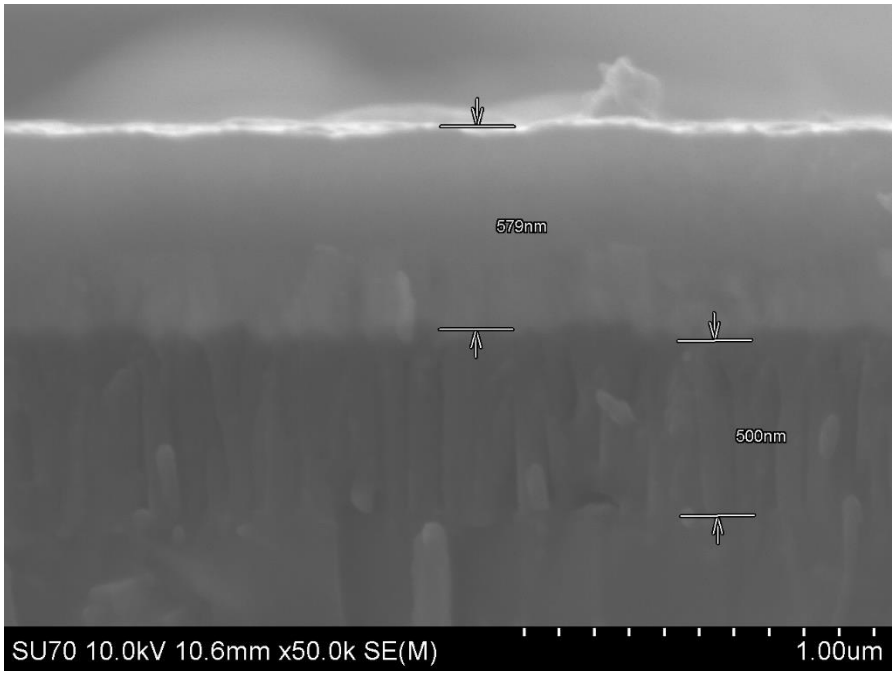

Figure 68: SEM cross section of 1500 cycles of growth on the anodized alumina/ceramic templates. The amorphous alumina homogenizes the composition of the surface, leading to a more uniform nucleation than the bare ceramic seen in Figure Figure 67.

DC excitation of the plasma head is still expected to produce nitrogen radicals, however the voltage required for DC source higher and the optimum pressure changes. RF excitation has serveral advantages over DC in that the RF fields can oscilate faster than the ions in the plasma can respond. Nitrogen atoms passing through the head undergo many passes of electrons as the field oscillates, leading to many more ionization events for the same voltage. The ossilation of

electrons near the grounded surfaces of the reactor also lead to excitation near the surfaces, whereas DC excitation can only occur between the plates. The same procedure was followed a in section 7.1 Sapphire Growthto determine the optimal pressure of 350 mTorr. The same rational design was applied, plasma power was kept as high as possible, loops as short as possible.

Figure 69 a)-h) shows several different features through the volume of the layers. Figure 69 b) shows the pore base where it is bonded to the ceramic. The AAO was found to be well adhered to the substrate across the sample, no signs of delamination or voiding was present. Figure 69 c) shows the AAO GaN interface where polycrystalline GaN has been observed, indicating the initial nucleation has no distinct phase. This could be expected from the lack of and underlying crystal structure from the AAO. The diffraction map inserts on c) and d) show a mixture of wurtzite and cubic phases are present within the first 100 nm indicative of stacking faults. Figure 69 e) shows that after about 200 nm the layer will preferentially orient itself towards the c-axis, however cubic domains are still present with the diffraction map inserts showing a wurtzite structure with present. The grains are observed to tilted and twisted relative to one another Figure 69 f)-h).

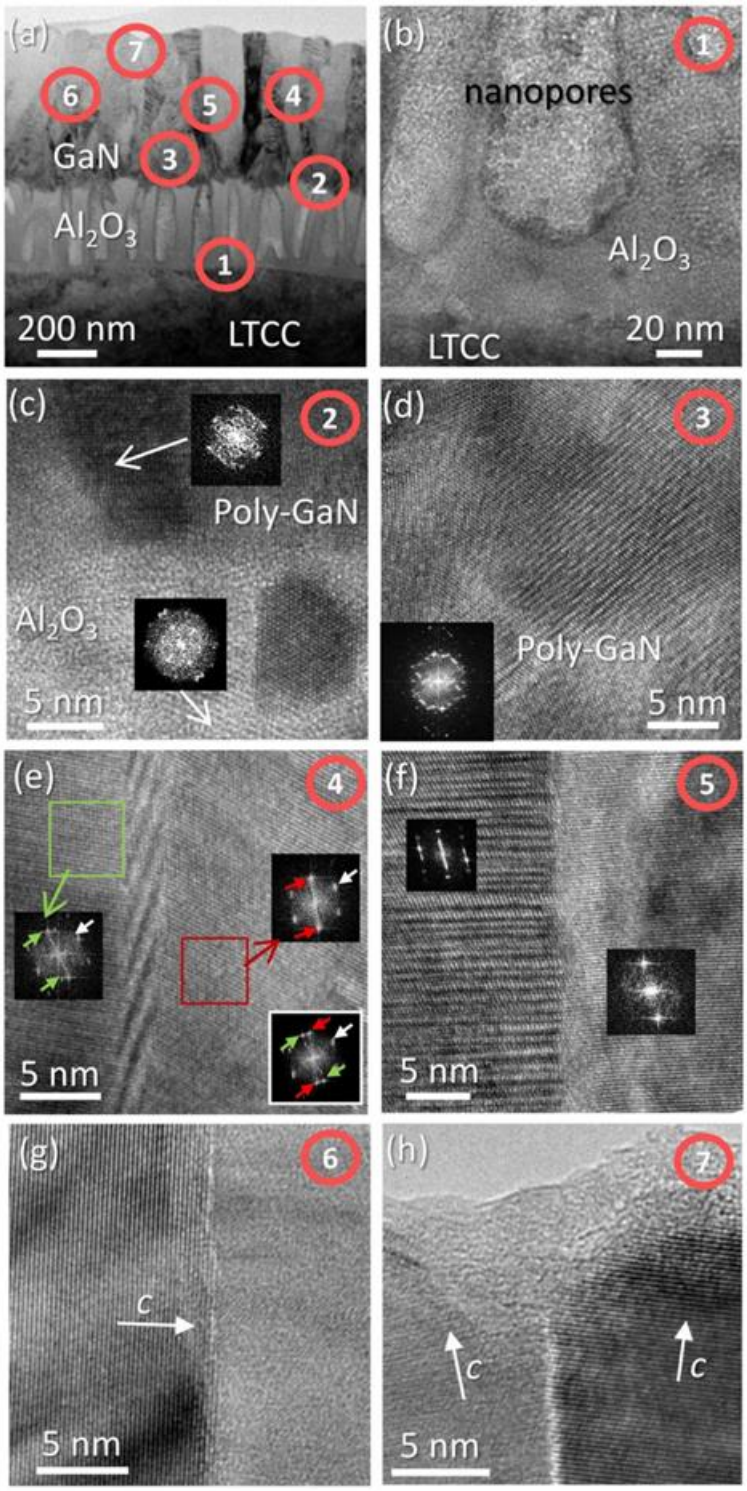

Figure 69: Bright Field Diffraction Contrast TEM (BF-DCTEM) cross section of GaN on AAO growth illustrating several structural features of GaN. a) Overview of areas examined. b) The interface between the LTCC and AAO, show an abrupt and well adhered interface. c-d) the GaN AAO interface is seen to be mostly polycrystalline for the first 100-200 nm. e) a mixture of cubic and hexagonal phases. f)-h) show the grains visible have a relative twist and tilt to one another.

No significant penetration into the pore structure can be seen in the TEM images of Figure 69 or the EDX line profile in Figure 70. [196]

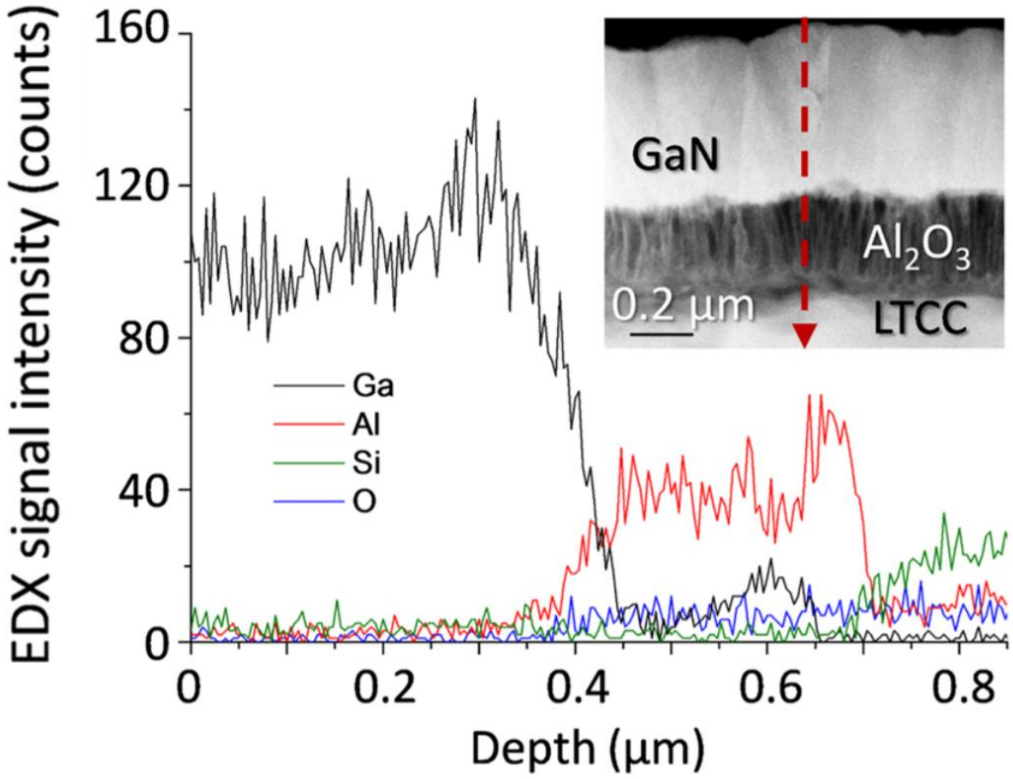

Figure 70: EDX line profile of the GaN/AAO/LTCC structure.

The lack of penetration into the layers shows a back contact to these films through the alumina may be difficult to achieve. Given the conformal nature of CVD the lack of pore filling could possibly be caused by line-of-sight properties of the plasma and the poor quality of the poor opening due too the single stage anodization.

XRD results from 3000 growth cycles on the AAO ceramic (blue) and sapphire (red) can be seen in Figure 71:. The FWHM of the sapphire and ceramic samples was measured to be 0.1477˚ and 0.1802˚ respectively.

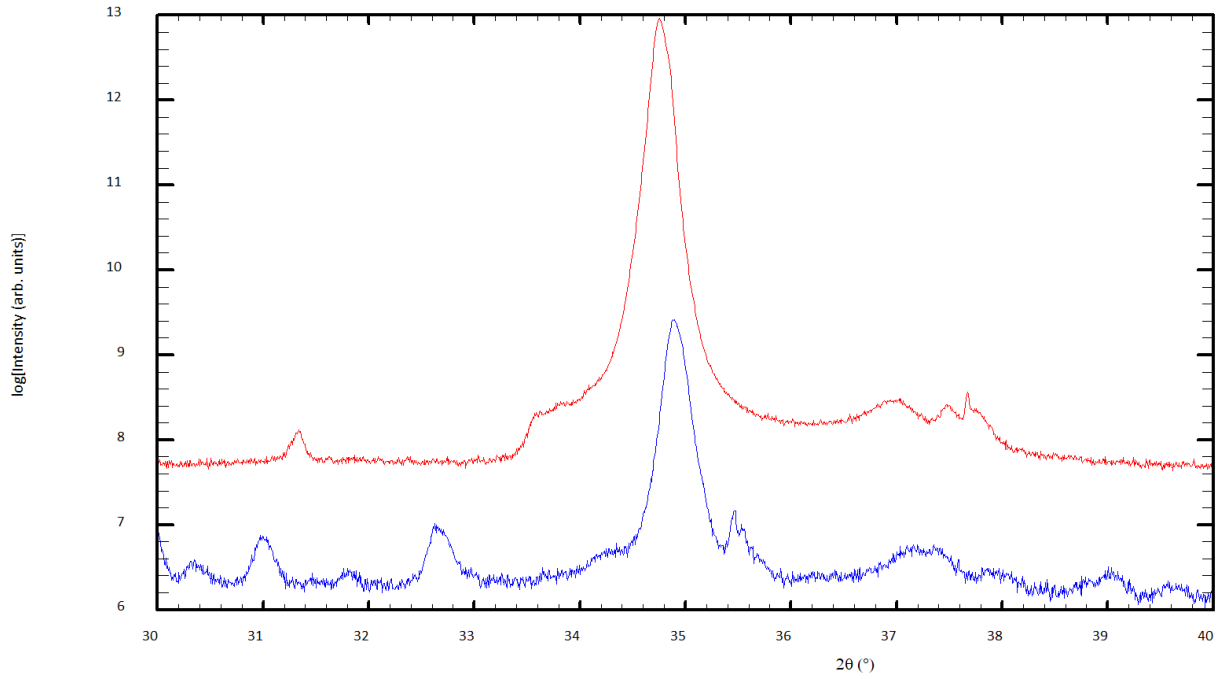

Figure 71: XRD results from 3000 cycles on the AAO ceramic (blue) and sapphire (red).

Given the same growth conditions the sapphire can be seen to have a peak 4 orders of magnitude higher with a lower FWHM compared to the ceramics. The peak in sapphire can also be seen slightly closer to the relaxed (0002) position of 34.63˚.

The results of this growth show that while deposition on anodized alumina is possible and represent an improved layer over bare ceramic deposition. Detailed analysis performed using TEM measurements indicates these layers contain a mosaic structure with a relative twist and tilt between the grains. The layers were observed to well adhered and abrupt, but the lack of penetration into the pore structure was observed through EDX.

7.4.1. ZnO

The conditions from experiments on float glass were used to determine and optimum withdraw speed of 10 cm/min, 0.7M ZAD concentration, 1% $AlCl_3$ doping and a 1:1 ZAD:MEA ratio. The preheating that occurs after each dip was calibrated using a type k thermocouple to be 275°C in the open tube style surface and the final bake was performed in a closed oven at 600 °C. The surface roughness measurements in section 7.3.2.1 ZnO show that many microns of material are needed to fill the pores under these conditions. Even after 115 cycles (over 24 hrs of constant dipping, > 7 µm thickness) undulations in the surface can still be seen on AFM and SEM.

For these experiments the RF source was available, and growth occurred at 1400 mTorr and 650 °C. The XRD results for GaN on ZnO Ceramic can be seen in Figure 72:.

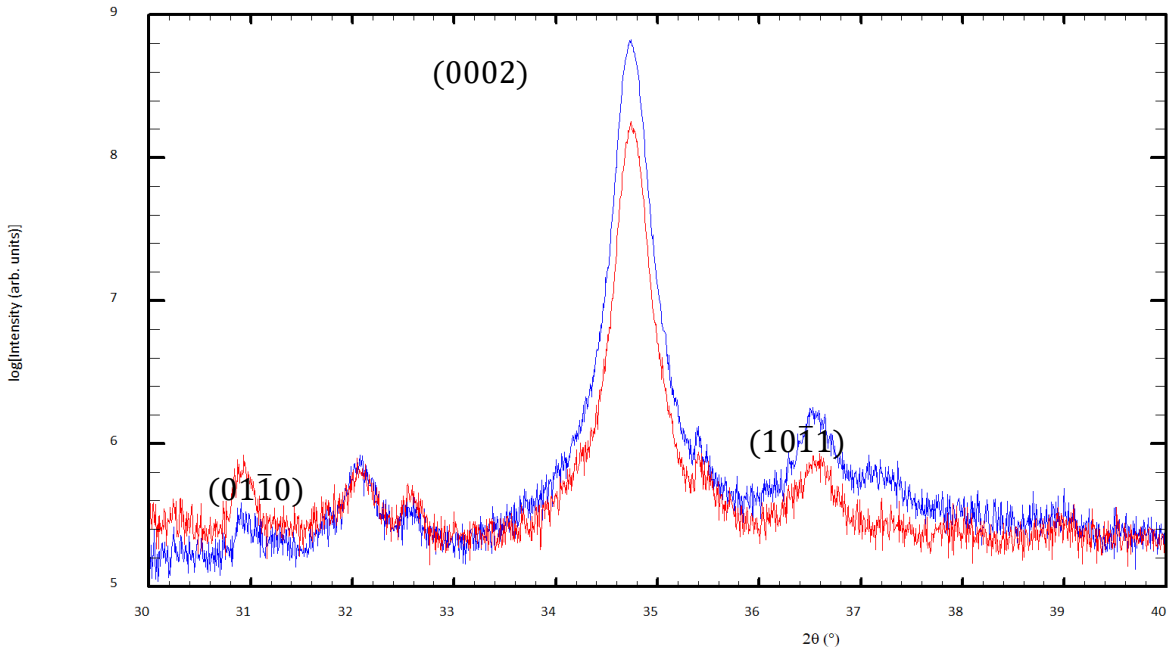

Figure 72: XRD of GaN on ZnO coated ceramic. The red scan represents the pre deposition ZnO surface, while the blue is post growth GaN.

One clear issue with using XRD to analyze these growths is the very close size of the ZnO and GaN crystals makes distinguishing their peaks impossible. To determine the effect of GaN growth an XRD needs be taken before and after to look at the change in the XRD spectra. Doing

this assumes the deposition condition in the reactor do not disrupt the ZnO. The initial ZnO peak ((Figure 73, red) FWHM was found to be 0.2522 ˚.

The post deposition peak (Figure 73, blue) was found to have a FWHM of 0.2519 ˚. The calculated difference (green) was found to have a FWHM of 0.2358˚.

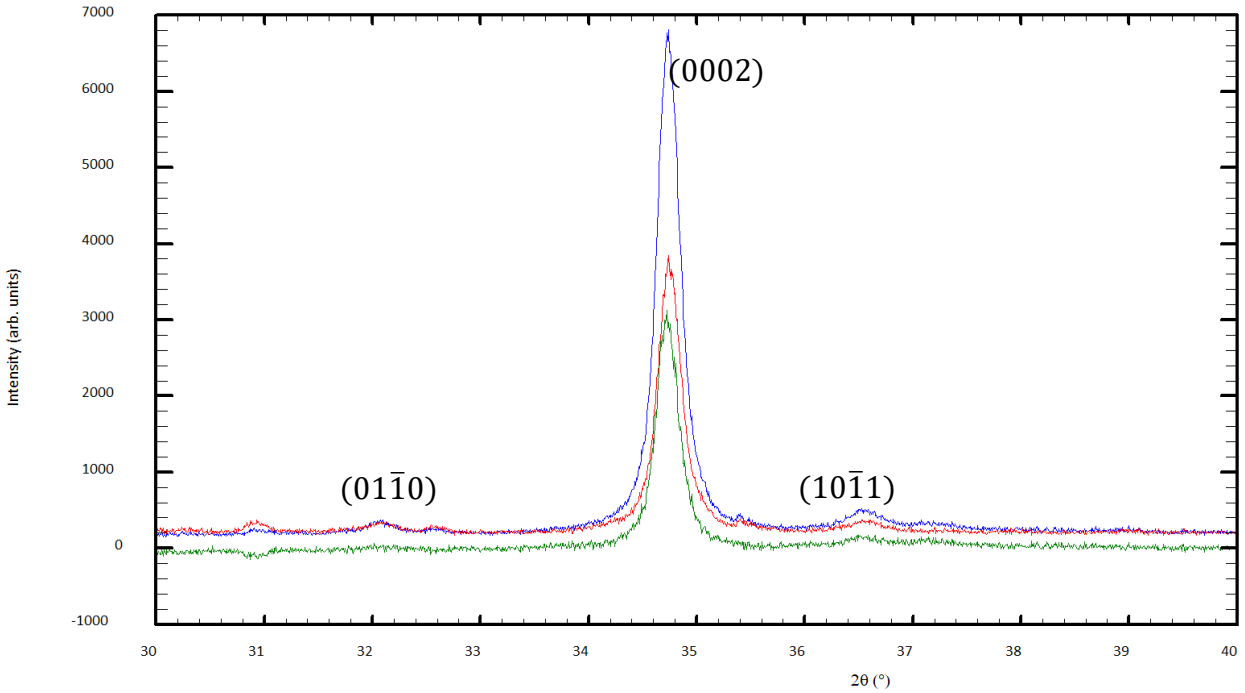

Figure 73: GaN growth on ZnO coated LTCC. The initial curve can be seen in red and post deposition can be seen in blue. The difference between the two curves (green) is a result of the GaN deposition.

Surface analysis was performed on this sample using X-ray photoelectron spectroscopy (XPS) (Figure 74) to determine impurities on the surface. The quantification of these spectra is given in Table 8: XPS peak quantification of GaN deposition on ZnO coated LTCC. and Table 9: XPS peak quantification of GaN on sapphire at 700 ˚C. Two important observations are the increase in the oxygen levels and the lack of Zn seen in the spectra. The increase in oxygen from the sapphire reference samples indicates an additional source of oxygen in these samples, likely diffusing from the ZnO layer.

Table 8: XPS peak quantification of GaN deposition on ZnO coated LTCC.

Component	BE [eV]	FWHM [eV]	RSF	Atomic conc. [%]	Error [%]	Mass conc. [%]	Error [%]
Ga 2p3/2	1116.60	0.00	3.72	15.61	0.13	47.66	0.24
O 1s	530.60	0.00	0.78	13.59	0.48	9.52	0.35
N 1s	395.60	0.00	0.48	63.77	0.44	39.12	0.22
C 1s	283.60	0.00	0.28	7.03	0.36	3.70	0.20

Table 9: XPS peak quantification of GaN on sapphire at 700 ˚C.

Component	BE [eV]	FWHM [eV]	RSF	Atomic conc. [%]	Error [%]	Mass conc. [%]	Error [%]
Ga 2p3/2	1116.40	0.00	3.72	17.34	0.14	50.90	0.26
O 1s	530.40	0.00	0.78	6.70	0.39	4.51	0.27
N 1s	395.40	0.00	0.48	68.70	0.41	40.52	0.24
C 1s	284.40	0.00	0.28	6.93	0.33	3.51	0.17
Ar 2p	235.40	0.00	1.16	0.33	0.11	0.56	0.18

A solution to this would be to decrease the temperature if possible, which is undesirable for surface migration in the samples. An increase in the growth rate can decrease the oxygen, since it is diffusing from the substrate a thicker layer will decrease the concentration reaching the surface. In this case the bulk may remain unintentionally doped with oxygen. A third solution that may be possible is to change the deposition technique from sol-gel to a vacuum technique. Sol-gel layers form as dense networks of crystallites, but as seen in the case with Al doping, the increase surface area can have an affect material property that are surface dependant. Since the temperature is close to the observed decomposition temperature of ZnO in our system, it is not unreasonable to expect this to be a source of oxygen.

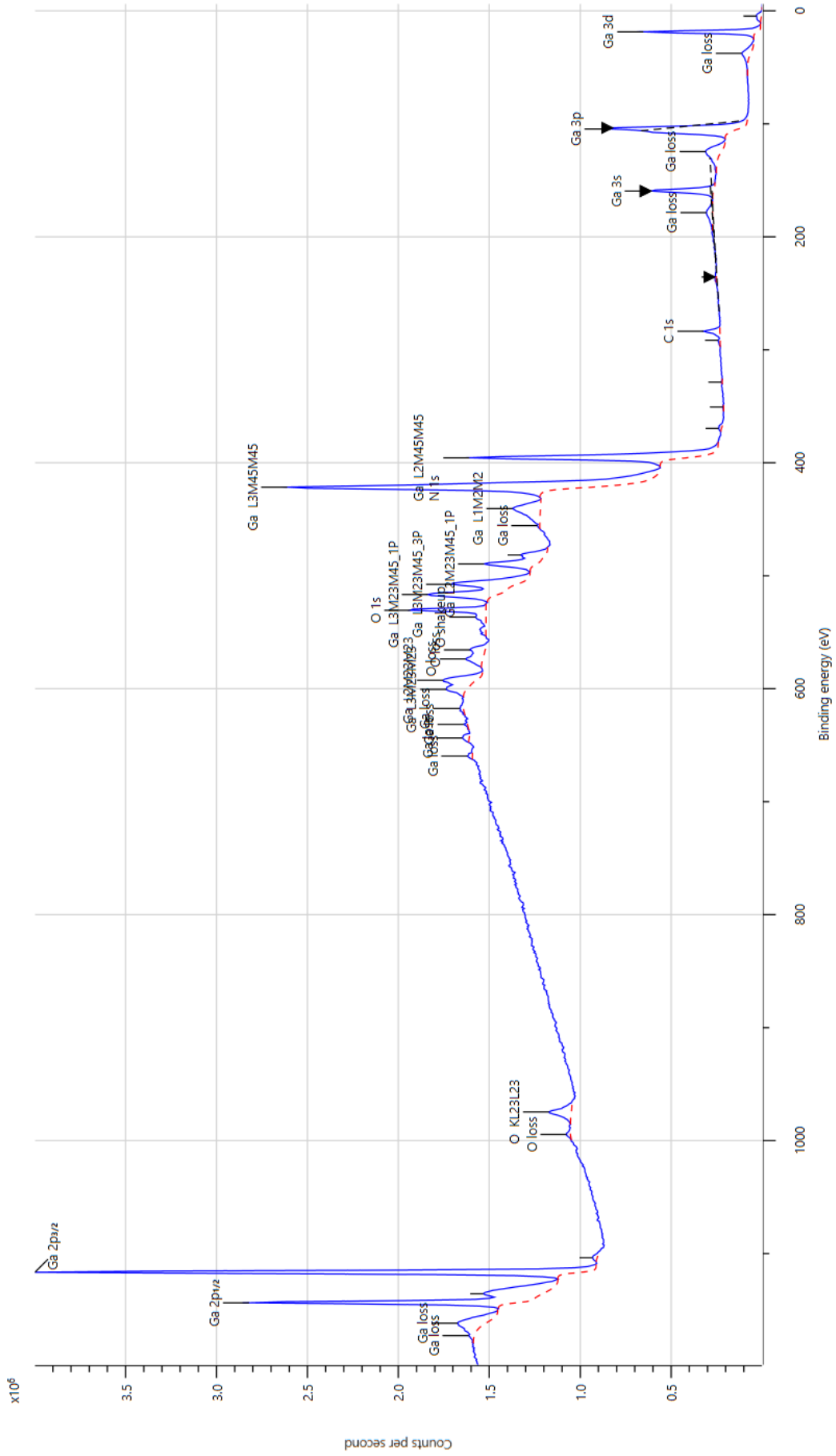

Figure 74: XPS surface analysis of GaN on ZnO ceramic. No zinc peaks can be seen in the analysis indicating diffusion through the sample did not occur.

An AFM scan of the surface shows an increase in the surface roughness from changes from the average of 6.351 nm found in Figure 59 to 12.36 nm in Figure 75.

7.4.2. IV Curves

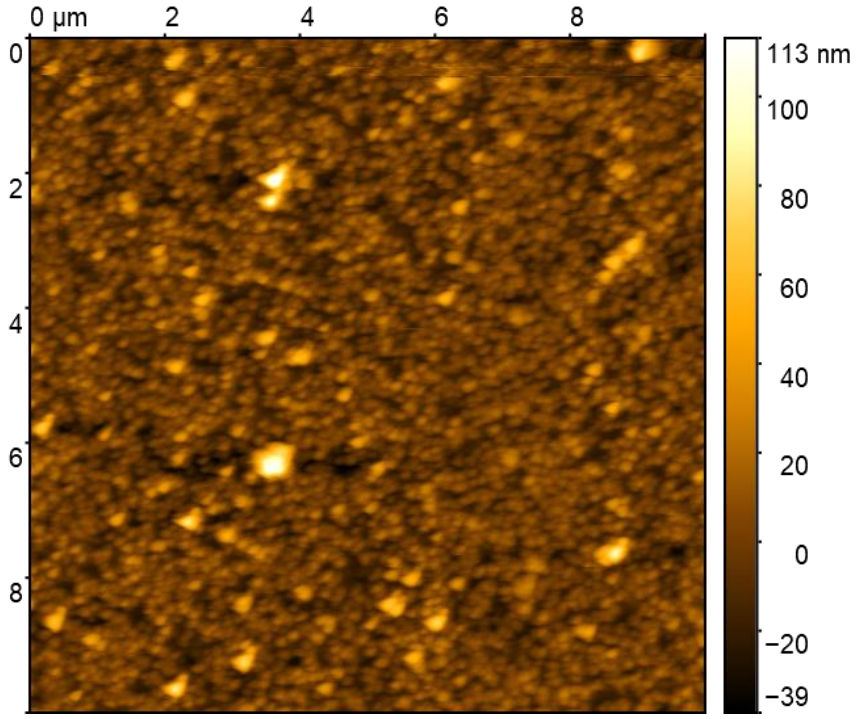

Figure 75: AFM Scan of GaN on ZnO LTCC. The surface roughness was observed to increase with GaN deposition.

Schottky contacts were deposited on The ZnO sample seen in Figure 75. Contacts were also deposited on sapphire samples produced at 700 °C and 650 °C. Cleaning of GaN sapphire samples is normally performed using an acid to etch the oxide layer and reduce contact resistance [241]. Acid cleaning was not used in this case since ZnO can easily be etched by these acids. Attempts to clean samples with (1:1) solutions of HCL resulted in the undercutting of GaN layers.

Figure 76 shows the result of a 1 minute etch on the 5 layer sample where a typical surface cleaning is 3 minutes [241]. The etching is seen the pronounce the edges of the underlying ZnO layer, indicating a etching process is occurring.

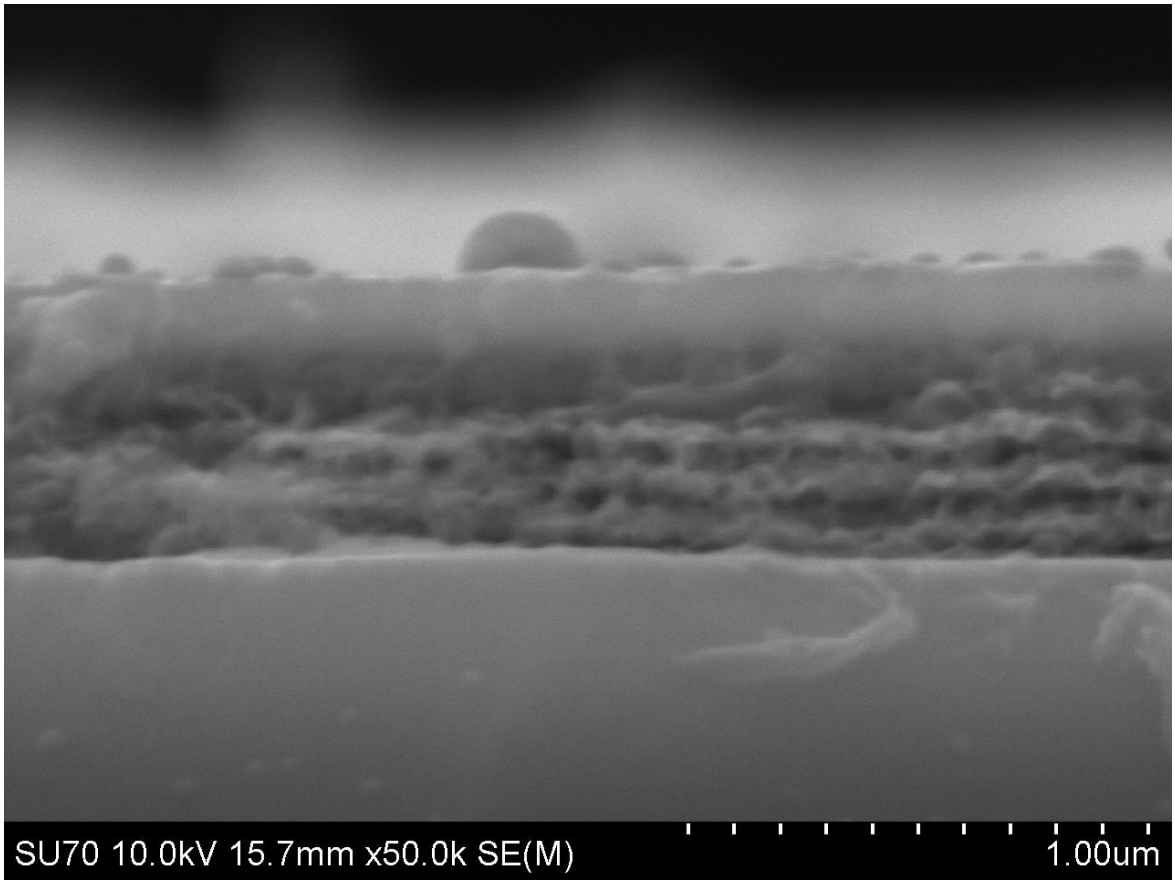

Figure 76: 5 dip ZnO on LTCC sample etched in 1:1 HCL for 1 min. The yellowish hue of the GaN layer is visibly removed from the edges of the sample. In the cross section the layering of the ZnO structure can be seen.

The contacts were Ni/Au pads with an area of ~1 mm^2 deposited through DC magnetron sputtering. Al was used at the ohmic contact sputtered through the same system. Since these contacts contain only a After the contacts have been applied an annealing was performed 500 °C for 10 mins to passivate surface donors. The increased roughness in the GaN on ZnO/LTCC,

increase in oxygen detected by XPS, and a broader XRD peak are all indicative that the GaN on ZnO is n-type.

In order to examine the junction characteristics of the samples an IV curve be measured and plotted using the methods described in 3.1.3 IV Curves to extract the ideality factor (η), barrier height (ϕ_b) and series resistance (R_s). The measured curves can be seen in Figure 77 and Figure 78. A 50-point moving average was applied to the data to reduce noise in calculated derivatives.

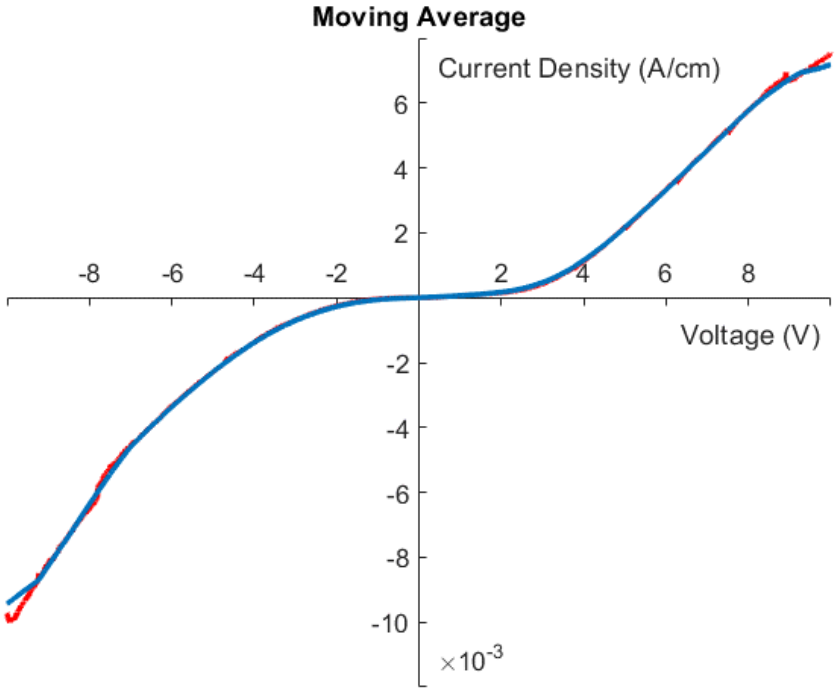

Figure 77: GaN sapphire IV curves for 650 ˚C growths.

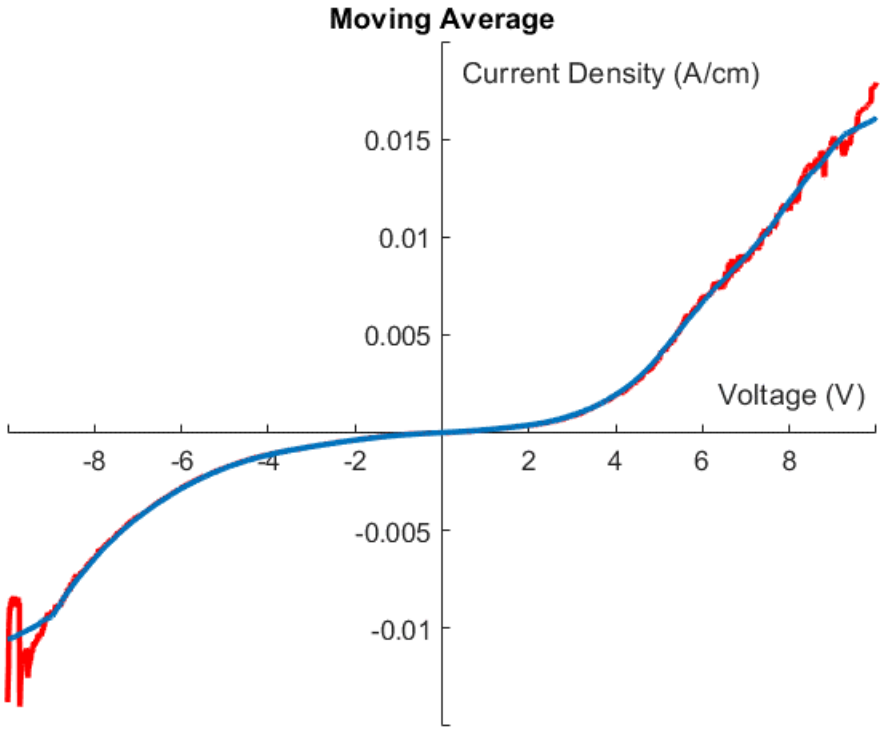

Figure 78: GaN sapphire IV curves for 700 ˚C growths.

The IV analysis outlined in section 3.1.3 IV Curves was performed on the data gathered in Figure 77 and Figure 78. Plots of $\frac{dV}{d(\ln(J))}$ vs J for the 650 °C and 700 °C GaN sapphire growths can be seen in Figure 80 and Figure 79. Linear fits are shown in red over selected regions of the IV curves in both cases.

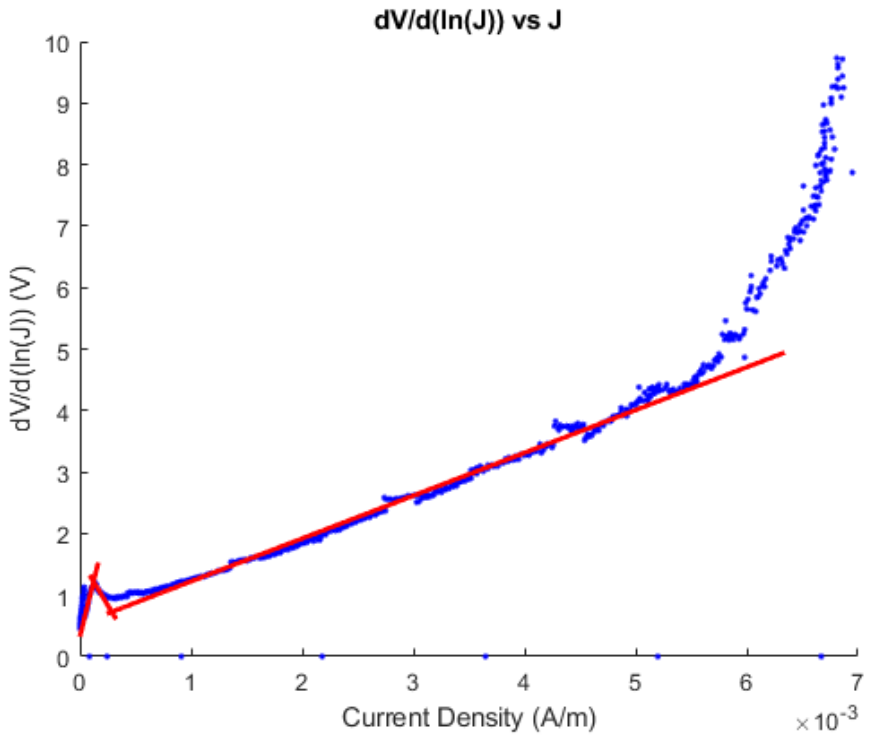

Figure 80: dV/d(ln(J)) curve for 650 ˚C sapphire growths.

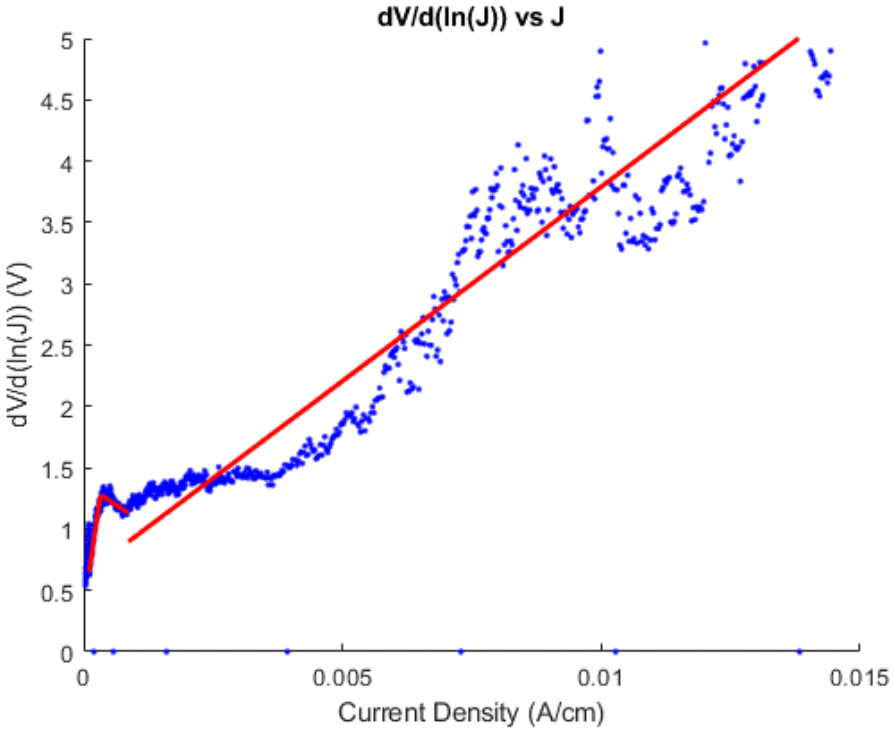

Figure 79: dV/d(ln(J)) curve for 700 ˚C sapphire growths.

Both the 650 °C (Figure 80) and 700 °C (Figure 79) growths show an initial linear regime followed by a region of negative resistance (the slope of the linear region is $\propto R_s$). This is short lived region of negative resistance is indicative of a tunneling mechanism. The high ideality factors and symmetry of the IV curve also indicate tunnelling is occurring through the junction.

The ideality factor and series resistance can be found using equation (3-10). The extracted parameters are listed in Table 10. The ideality factors are determined from least squares linear fits over the first linear regions before the observed negative resistance regions. The series resistances are found from the slope of the third region fit. The barrier heights are determined using the intercept of equation (3-11). A plot of $H(J)$ vs J for the 650 °C GaN sapphire growths and the 700 °C can be seen in Figure 81 and Figure 82 respectively.

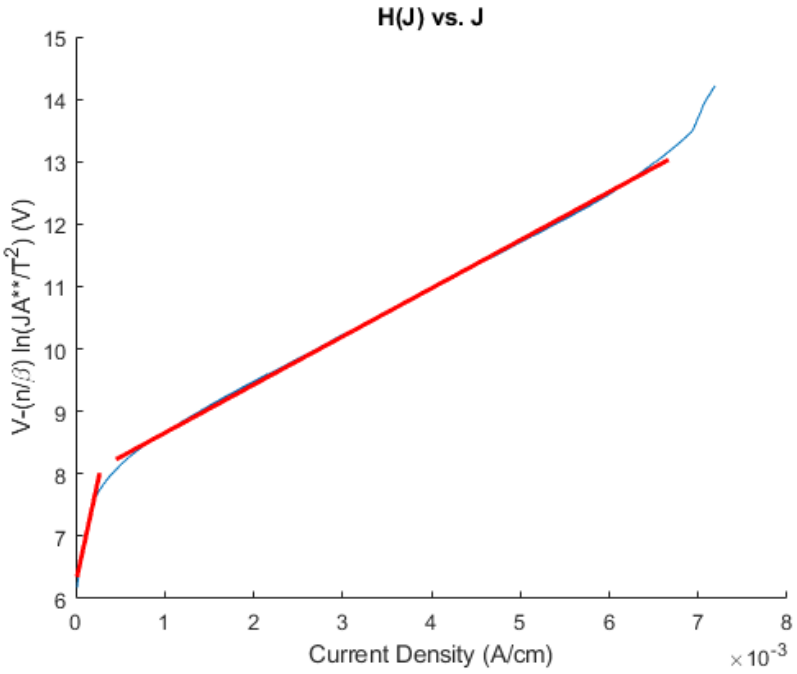

Figure 81: Plot of auxiliary function H(J) vs. the current density J for the 650 ˚C.

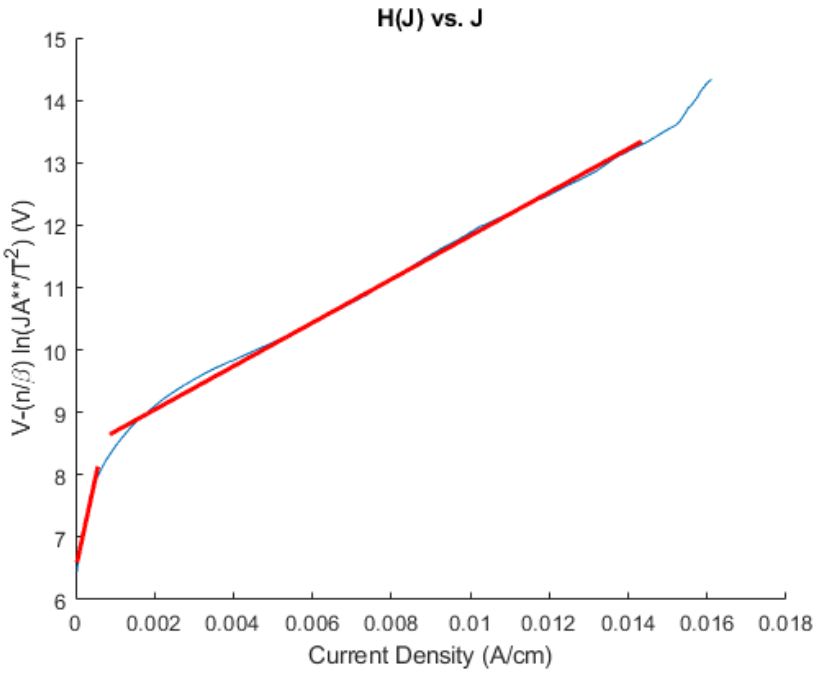

Figure 82: Plot of auxiliary function H(J) vs. the current density J for the 700 °C.

The energy barriers are calculated from the first linear region using a least squares fit. The slope of the second linear region is used to determine the series resistance $R_s{}^*$ in Table 10. The values of R_s and found $R_s{}^*$ found by equations (3-10) and (3-11) were found to be fairly close to one another. Both indicate a high series resistance due too the relatively thin device layers and defects in the device layers.

Table 10: Calculated diode parameters from Ni/Au Schottky diodes on Sapphire.

Temperature (°C)	Ideality Factor (η)	ϕ_B (eV)	R_s (Ω)	R_s^*(Ω)
650	16.04	0.5	69658	77249
700	13.65	0.47	31697	34848

The observed energy barriers are lower than the expected value of ~1.05 eV [242]. The energy barrier in both cases is close to 0.5 eV. A significantly lower energy barrier than expected from the Schottky-Mott model presented in section 3.1 could be explained by a high density of surface states which can lead too fermi level pinning, known to occur on defective GaN surfaces grown at low temperatures [242]. Several pieces of evidence such as the negative resistance observed in Figure 80 and Figure 79, the symmetry of the IV curves and high ideality factors indicate a tunneling mechanism dominates the current flow in both directions. A decrease in temperature can be expected to increase the presence of defects in the crystal, increasing the number of defect states on the surface as well decreasing carrier mobility in the layers.

In the case of Ni/Au on GaN/ZnO/LTCC no rectification could be demonstrated. Based on the results of the XPS, XRD, and AFM for these layers combined with the behaviour observed for sapphire, a higher density of surface states can be expected from the decrease in material quality from sapphire. The increased surface roughness (12.36 nm for GaN LTCC in Figure 75 vs 2.89 nm for GaN sapphire in Figure 46) and the increased oxygen content seen in Table 8 and Table 9

can both be expected to increase the junction leakage to the point of making the contact fully ohmic.

The measured IV curves for 30 to 115 dips can be seen in Figure 83. The sample with 115 coats representing did show some nonlinear behaviour around the origin, but quickly disappears and a similar analysis to the sapphire cannot be performed.

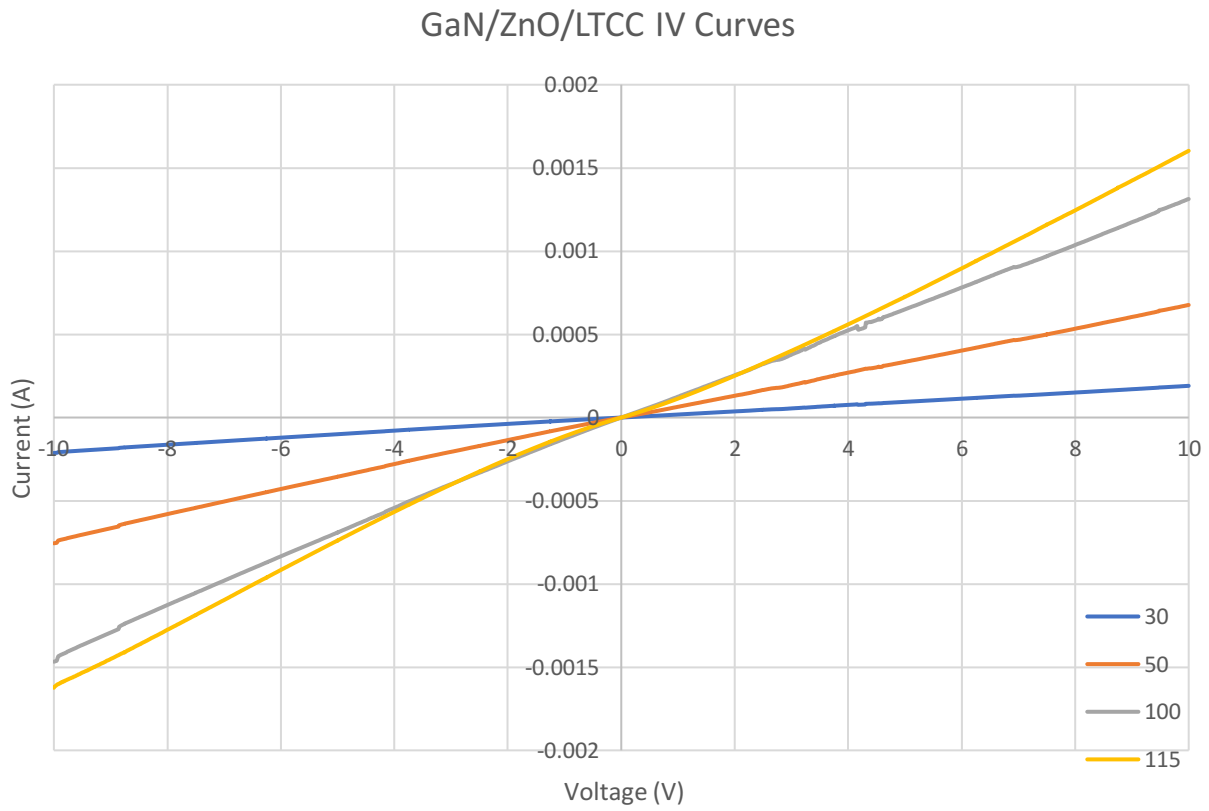

Figure 83: GaN/ZnO/LTCC IV curves for the samples from 7.4.1. ZnO The curves exhibit ohmic behaviour in all cases. In the case of 115 dips some nonlinearity can be seen but no rectification can be observed.

The resistance found from the inverse of the slope of these curves was determined using a linear least squares fit, summarized in Table 11.

Table 11: Summary of resistance values from Figure 84

Number of Dips	Resistance (Ω)	R^2
30	50922	0.9991
50	14335	0.9991
100	7383	0.9991
115	6466	0.9976

The resistance of the layers was found to decrease below what was observed for the series resistance in Table 10. The low resistance observed and its dependence on the ZnO thickness indicates current flow is occurring mainly in the ZnO buffer and not the resistive GaN epilayer. A possible solution to this could be to grow thicker layers of GaN, or the inclusion of an electron blocking layer in the device.

One useful aspect of LTCC which was illuded too earlier was the ability have vias and back contacts embedded in the structure with fine pitch. The vias are fill with a glass frit/metal mixture which is usually silver due too its high conductivity. Figure 84: ZnO coated silver via in the LTCC structure. 115 coatings (~7 μm) of material has been dip coated on the surface.Figure 84 shows an SEM cross section of a silver via coated in ZnO. Vias were found the have reliable vertical conduction after the GaN growth process. No extensive thermal cycling analysis was performed on these contacts, but they were found to maintain integrity after a 48h heat exposure at 600 °C.

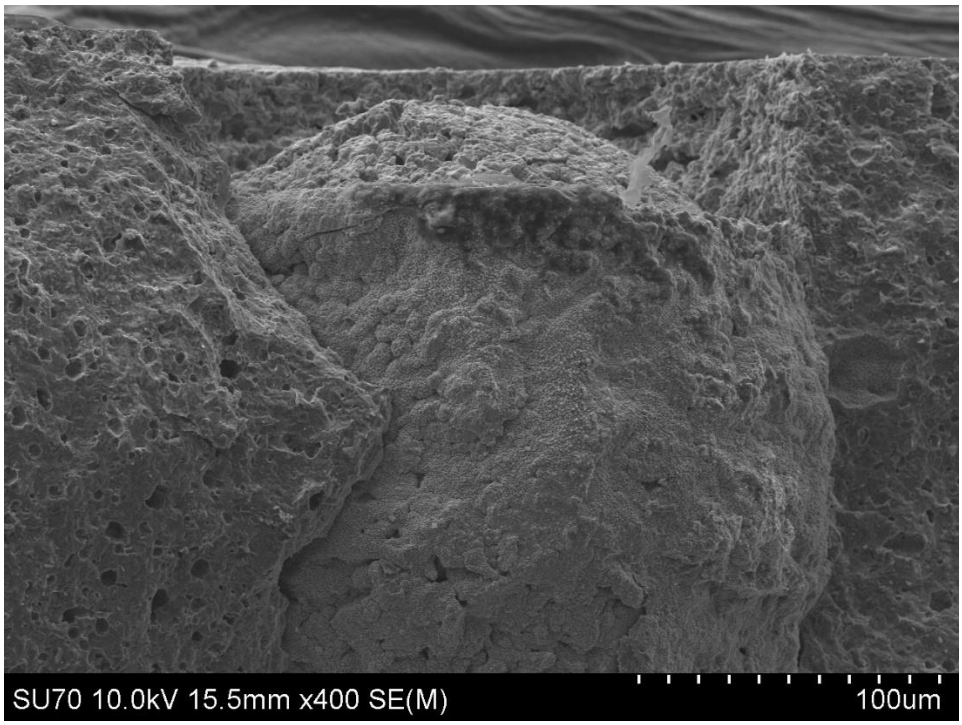

Figure 84: ZnO coated silver via in the LTCC structure. 115 coatings (~7 µm) of material has been dip coated on the surface.

The vias were found to introduce surface deviations on the scale of 10's of microns and a planarization over their surface was not possible using the number of coating explored in this work.

8.0 Conclusions

The prototype flow modulation epitaxy (FME) system at Lakehead has been used to demonstrate GaN Ni/Au Schottky junctions on sapphire substrates. These devices were shown to exhibit leaky junction characteristics (ideality constant >10 in both cases), presumably due too a high density of surface states present from defects and oxygen impurities, evidenced by the AFM and XPS data. A possible solution to this would be a grow significantly thicker device layers, which may allow further reduction of defects. However only a certain amount of group III material can be deposited at once in this layer by layer epitaxial process to avoid heterogenous nucleation, which can drastically reduce crystalline quality in the material.

The optimal loop time was found to 12s, leading to a growth rate of ~75 nm/hr. This is slow compared to μm/hr rates achievable with continuous thermal systems. A continuous growth in a plasma CVD style of system may be able to achieve higher growths rates but mixing of the group III precursors with the reactive plasma leads to powder formation, adduct formation, and additional impurity incorporation during growth. The limiting factor in the growth loop is the time needed for complete nitridation of the group III adlayer, therefore the loops may be shortened if a greater flux of reactive nitrogen species can reach the surface. A modification of the anode cathode gap in the head may be able to achieve this but is the subject of possible future work with the system.

Porous alumina, sol-gel silica, and sol-gel ZnO coatings were each found to homogenize the surface to a point where uniform coatings could be applied. All oxide coatings were observed to adhere well to the interface and delamination was not observed. The planarization of the

ceramics was found to require several microns (up to 7 μm was explored here) to fill the natural voids in the LTCC sintered glass structure.

Solution deposition processes represent a versatile technique which can be used to planarize the surface, however the layer by layer nature of spin or dip coating limits the thickness achievable for crystalline materials in a single deposition cycle. As with FME, heterogeneous nucleation in solution disrupts the crystalline order leading a polycrystalline texture if the layers are too thick. The thickness per cycle is therefore limited close to the lowest thermally stable crystallite size (60-70 nm for ZnO). To achieve filling of the surface pits, many dips are therefore required if we wish to maintain crystallinity through the layer. This may be necessary in the case where transparency or high conductivity is needed, both of which are related to the crystallinity of the ZnO. The ZnO (0002) WZ texture could be observed on the surface as early as 5 dips, therefore an alternative strategy would be an amorphous fill layer which provides smoothing in significantly fewer dips, while a thin ZnO layer provides texture.

The similar crystal structure of ZnO makes it a good candidate for GaN heteroepitaxy, however it can easily be etched by hydrogen, and the high vapour pressure of zinc also makes sublimation an issue for vacuum systems. A limit of 650 °C at 1400 mTorr was found in our system.

The GaN deposited on the ZnO buffers was unable to form Schottky junctions in this study. Comparatively to the sapphire growths the sample were rougher, more disordered and contained more oxygen. No Zn could be detected on the surface of the GaN through XPS measurements and ZnO decomposition is not seen in XRD or AFM measurements. Oxygen and water vapour contamination from the reactor and precursor gasses are expected to be only a few ppm and cannot explain the mass % observed by XPS. Oxides may therefore be forming during the post growth

storage environment, which was not explicitly tested. Cleaning of the native oxide was also observed to be a technological challenge as any acid treatment used to remove Ga_2O_3 may also remove the ZnO buffer, but at a much higher rate, leading to possible undercutting.

An alternative approach to this would be to increase the temperature to increase adatom and dislocation mobility in the layers but is only possible in the case of sapphire (or other thermally resilient materials) and not with glass materials such as LTCC. The use of oxide materials has been shown the planarize homogenize the surface, not however to a point where it is comparable to a CMP single crystal wafer. In light of the limited growth rate capabilities of the techniques explored in this work I believe that the performance of the LTCC/ZnO/GaN diodes could be increased using reactive sputtering techniques which may be able to provide higher growth rates for bulk layers.

Bibliography

[1] M. Levinshtein, S. Rumyantsev, and M. Shur, *Handbook Series on Semiconductor Parameters: Volume 1: Si, Ge, C (Diamond), GaAs, GaP, GaSb, InAs, InP, InSb*, vol. 1. WORLD SCIENTIFIC, 1996.

[2] H. Morkoç, *Handbook of Nitride Semiconductors and Devices*. Weinheim : [Chichester: Wiley-VCH ; John Wiley, distributor], 2008.

[3] H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Appl. Phys. Lett.*, vol. 48, no. 5, pp. 353–355, Feb. 1986, doi: 10.1063/1.96549.

[4] X. H. Wu, D. Kapolnek, E. J. Tarsa, B. Heying, S. Keller, B. P. Keller, U. K. Mishra, S. P. DenBaars, and J. S. Speck, "Nucleation Layer Evolution in Metal-organic Chemical Vapor Deposition Grown GaN," *Appl. Phys. Lett.*, vol. 68, no. 10, pp. 1371–1373, Mar. 1996, doi: 10.1063/1.116083.

[5] K. Hiramatsu, "Epitaxial lateral overgrowth techniques used in group III nitride epitaxy," *J. Phys. Condens. Matter*, vol. 13, no. 32, p. 6961, 2001, doi: 10.1088/0953-8984/13/32/306.

[6] T. Mukai, K. Takekawa, and S. Nakamura, "InGaN-Based Blue Light-Emitting Diodes Grown on Epitaxially Laterally Overgrown GaN Substrates," *Jpn. J. Appl. Phys.*, vol. 37, no. Part 2, No. 7B, pp. L839–L841, Jul. 1998, doi: 10.1143/JJAP.37.L839.

[7] T. Sasaki and T. Matsuoka, "Analysis of two-step-growth conditions for GaN on an AlN buffer layer," *J. Appl. Phys.*, vol. 77, no. 1, pp. 192–200, Jan. 1995, doi: 10.1063/1.359368.

[8] M. Broas, P. Sippola, T. Sajavaara, V. Vuorinen, A. Pyymaki Perros, H. Lipsanen, and M. Paulasto-Kröckel, "Structural and chemical analysis of annealed plasma-enhanced atomic layer deposition aluminum nitride films," *J. Vac. Sci. Technol. A*, vol. 34, no. 4, p. 041506, Jun. 2016, doi: 10.1116/1.4953029.
[9] C. Ozgit, I. Donmez, M. Alevli, and N. Biyikli, "Atomic layer deposition of GaN at low temperatures," *J. Vac. Sci. Technol. A*, vol. 30, no. 1, p. 01A124, Jan. 2012, doi: 10.1116/1.3664102.
[10] C. Ozgit-Akgun, E. Goldenberg, A. K. Okyay, and N. Biyikli, "Hollow cathode plasma-assisted atomic layer deposition of crystalline AlN, GaN and AlxGa1−xN thin films at low temperatures," *J. Mater. Chem. C*, vol. 2, no. 12, pp. 2123–2136, Feb. 2014, doi: 10.1039/C3TC32418D.
[11] N. Nepal, V. R. Anderson, J. K. Hite, and C. R. Eddy Jr., "Growth and characterization of III-N ternary thin films by plasma assisted atomic layer epitaxy at low temperatures," *Thin Solid Films*, vol. 589, pp. 47–51, Aug. 2015, doi: 10.1016/j.tsf.2015.04.068.
[12] N. Nepal, N. A. Mahadik, L. O. Nyakiti, S. B. Qadri, M. J. Mehl, J. K. Hite, and C. R. Eddy, "Epitaxial Growth of Cubic and Hexagonal InN Thin Films via Plasma-Assisted Atomic Layer Epitaxy," *Cryst. Growth Des.*, vol. 13, no. 4, pp. 1485–1490, Apr. 2013, doi: 10.1021/cg3016172.
[13] M. M. Zhong, F. W. Qin, Y. M. Liu, C. Wang, J. M. Bian, E. P. Wang, H. Wang, and D. Zhang, "Low-temperature growth of high c-orientated crystalline GaN films on amorphous Ni/glass substrates with ECR-PEMOCVD," *J. Alloys Compd.*, vol. 583, pp. 39–42, Jan. 2014, doi: 10.1016/j.jallcom.2013.08.153.
[14] D.-C. Park, H.-C. Ko, S. Fujita, and S. Fujita, "Growth of GaN on Indium Tin Oxide/Glass Substrates by RF Plasma-Enhanced Chemical Vapor Deposition Method," *Jpn. J. Appl. Phys.*, vol. 37, no. 3A, p. L294, Mar. 1998, doi: 10.1143/JJAP.37.L294.
[15] Y. Zhao, F. Qin, Y. Bai, Z. Ju, Y. Zhao, X. Zhang, S. Li, D. Zhang, J. Bian, and Y. Li, "Low temperature synthesis of GaN films on ITO substrates by ECR-PEMOCVD," *Vacuum*, vol. 92, pp. 77–80, Jun. 2013, doi: 10.1016/j.vacuum.2012.11.003.
[16] J. Bian, L. Miao, F. Qin, D. Zhang, W. Liu, and H. Liu, "Low-temperature ECR-PEMOCVD deposition of high-quality crystalline gallium nitride films: A comparative study of intermediate layers for growth on amorphous glass substrates," *Mater. Sci. Semicond. Process.*, vol. 26, pp. 182–186, Oct. 2014, doi: 10.1016/j.mssp.2014.04.030.
[17] A. Hassan, Y. Savaria, and M. Sawan, "GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review," *IEEE Access*, vol. 6, pp. 78790–78802, 2018, doi: 10.1109/ACCESS.2018.2885285.
[18] M. R. Werner and W. R. Fahrner, "Review on materials, microsensors, systems and devices for high-temperature and harsh-environment applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 249–257, Apr. 2001, doi: 10.1109/41.915402.
[19] M. Eberstein, C. Glitzky, M. Gemeinert, T. Rabe, W. A. Schiller, and C. Modes, "Design of LTCC with High Thermal Expansion," 2009, doi: 10.1111/J.1744-7402.2008.02316.X.
[20] J. Zhou, "Towards rational design of low-temperature co-fired ceramic (LTCC) materials," *J. Adv. Ceram.*, vol. 1, no. 2, pp. 89–99, Jun. 2012, doi: 10.1007/s40145-012-0011-3.
[21] D. Nowak and A. Dziedzic, "LTCC package for high temperature applications," *Microelectron. Reliab.*, vol. 51, no. 7, pp. 1241–1244, Jul. 2011, doi: 10.1016/j.microrel.2011.02.018.

[22] C. Jacq, Th. Maeder, and P. Ryser, “Sensors and packages based on LTCC and thick-film technology for severe conditions,” *Sadhana*, vol. 34, no. 4, pp. 677–687, Aug. 2009, doi: 10.1007/s12046-009-0031-z.
[23] D. Belavič, M. Hrovat, K. Makarovič, G. Dolanč, A. Pohar, S. Hočevar, and B. Malič, “3D LTCC structure for a large-volume cavity-type chemical microreactor,” *Microelectron. Int.*, vol. 32, no. 3, pp. 133–137, Jan. 2015, doi: 10.1108/MI-01-2015-0011.
[24] D. J. D. Smet, C. Nordquist, T. Turner, B. Rohrer, C. A. Walker, C. Ho, K. D. Patel, M. Okandan, S. B. Rohde, B. Wroblewski, K. Pfeifer, K. Peterson, and S. P. Buerger, “Macro-meso-microsystems integration in LTCC : LDRD report.,” 2007, doi: 10.2172/920804.
[25] M. Węglarski, P. Jankowski-Mihułowicz, G. Pitera, D. Jurków, and M. Dorczyński, “LTCC Flow Sensor with RFID Interface,” *Sensors*, vol. 20, no. 1, Art. no. 1, Jan. 2020, doi: 10.3390/s20010268.
[26] T. V. Shubina, S. V. Ivanov, V. N. Jmerik, D. D. Solnyshkov, V. A. Vekshin, P. S. Kop’ev, A. Vasson, J. Leymarie, A. Kavokin, H. Amano, K. Shimono, A. Kasic, and B. Monemar, “Mie resonances, infrared emission, and the band gap of InN,” *Phys. Rev. Lett.*, vol. 92, no. 11, p. 117407, Mar. 2004, doi: 10.1103/PhysRevLett.92.117407.
[27] M. Yoshimoto, H. Yamamoto, W. Huang, H. Harima, J. Saraie, A. Chayahara, and Y. Horino, “Widening of optical bandgap of polycrystalline InN with a few percent incorporation of oxygen,” *Appl. Phys. Lett.*, vol. 83, no. 17, pp. 3480–3482, Oct. 2003, doi: 10.1063/1.1622445.
[28] J. Tot, R. Dubreuil, B. Kadikoff, M. Nagorski, and D. Alexandrov, “Energy bandgap of InN,” In Press.
[29] V. Cimalla, “Label-Free Biosensors Based on III-Nitride Semiconductors,” in *Label-Free Biosensing: Advanced Materials, Devices and Applications*, M. J. Schöning and A. Poghossian, Eds. Cham: Springer International Publishing, 2018, pp. 59–102.
[30] C. G. Rodrigues, J. R. L. Fernandez, J. R. Leite, V. A. Chitta, V. N. Freire, A. R. Vasconcellos, and R. Luzzi, “Hole mobility in zincblende c–GaN,” *J. Appl. Phys.*, vol. 95, no. 9, pp. 4914–4917, May 2004, doi: 10.1063/1.1690865.
[31] C. Bayram and R. Liu, “Polarization-free integrated gallium-nitride photonics,” *Proc. SPIE-- Int. Soc. Opt. Eng.*, vol. 10111, 2017, doi: 10.1117/12.2251607.
[33] T. Yao and S.-K. Hong, Eds., *Oxide and Nitride Semiconductors: Processing, Properties, and Applications*. Berlin Heidelberg: Springer-Verlag, 2009.
[34] N. Grandjean, J. Massies, Y. Martinez, P. Vennéguès, M. Leroux, and M. Laügt, “GaN epitaxial growth on sapphire (0 0 0 1): the role of the substrate nitridation,” *J. Cryst. Growth*, vol. 178, no. 3, pp. 220–228, Jul. 1997, doi: 10.1016/S0022-0248(96)01191-8.
[35] S. Mohn, N. Stolyarchuk, T. Markurt, R. Kirste, M. P. Hoffmann, R. Collazo, A. Courville, R. Di Felice, Z. Sitar, P. Vennéguès, and M. Albrecht, “Polarity Control in Group-III Nitrides beyond Pragmatism,” *Phys. Rev. Appl.*, vol. 5, no. 5, May 2016, doi: 10.1103/PhysRevApplied.5.054004.
[36] R. Collazo, S. Mita, R. Schlesser, and Z. Sitar, “Polarity control of GaN thin films grown by metalorganic vapor phase epitaxy,” *Phys. Status Solidi C*, vol. 2, no. 7, pp. 2117–2120, 2005, doi: https://doi.org/10.1002/pssc.200461546.
[37] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck,

"Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, doi: 10.1063/1.369664.

[38] F. M. Yigletu, S. Khandelwal, T. A. Fjeldly, and B. Iñiguez, "Compact Charge-Based Physical Models for Current and Capacitances in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3746–3752, Nov. 2013, doi: 10.1109/TED.2013.2283525.

[39] U. T. Schwarz and M. Kneissl, "Nitride emitters go nonpolar," *Phys. Status Solidi RRL – Rapid Res. Lett.*, vol. 1, no. 3, pp. A44–A46, 2007, doi: https://doi.org/10.1002/pssr.200750018.

[40] Y.-L. Wang, B. H. Chu, K.-H. Chen, C. Y. Chang, T. P. Lele, Y. Tseng, S. J. Pearton, J. Ramage, D. Hooten, A. Dabiran, P. P. Chow, and F. Ren, "Real-time Detection of Botulinum Toxin with AlGaN/GaN High Electron Mobility Transistors," *ECS Trans.*, vol. 19, no. 3, p. 123, May 2009, doi: 10.1149/1.3120693.

[41] G. H. Chung, T. A. Vuong, and H. Kim, "Demonstration of hydrogen sensing operation of AlGaN/GaN HEMT gas sensors in extreme environment," *Results Phys.*, vol. 12, pp. 83–84, Mar. 2019, doi: 10.1016/j.rinp.2018.11.064.

[42] M. S. Z. Abidin, A. M. Hashim, M. E. Sharifabad, S. F. A. Rahman, and T. Sadoh, "Open-Gated pH Sensor Fabricated on an Undoped-AlGaN/GaN HEMT Structure," *Sensors*, vol. 11, no. 3, Art. no. 3, Mar. 2011, doi: 10.3390/s110303067.

[43] S. C. Hung, B. H. Chou, C. Y. Chang, C. F. Lo, K. H. Chen, Y. L. Wang, S. J. Pearton, A. Dabiran, P. P. Chow, G. C. Chi, and F. Ren, "Minipressure sensor using AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 94, no. 4, p. 043903, Jan. 2009, doi: 10.1063/1.3072606.

[44] M. A. Johar, M. A. Hassan, A. Waseem, J.-S. Ha, J. K. Lee, and S.-W. Ryu, "Stable and High Piezoelectric Output of GaN Nanowire-Based Lead-Free Piezoelectric Nanogenerator by Suppression of Internal Screening," *Nanomaterials*, vol. 8, no. 6, Art. no. 6, Jun. 2018, doi: 10.3390/nano8060437.

[45] S. Zhang and F. Yu, "Piezoelectric Materials for High Temperature Sensors," *J. Am. Ceram. Soc.*, vol. 94, no. 10, pp. 3153–3170, 2011, doi: https://doi.org/10.1111/j.1551-2916.2011.04792.x.

[46] T. Makino, Y. Segawa, M. Kawasaki, A. Ohtomo, R. Shiroki, K. Tamura, T. Yasuda, and H. Koinuma, "Band gap engineering based on MgxZn1−xO and CdyZn1−yO ternary alloy films," *Appl. Phys. Lett.*, vol. 78, no. 9, pp. 1237–1239, Feb. 2001, doi: 10.1063/1.1350632.

[47] M. A. Moram and M. E. Vickers, "X-ray diffraction of III-nitrides," *Rep. Prog. Phys.*, vol. 72, no. 3, p. 036502, 2009, doi: 10.1088/0034-4885/72/3/036502.

[48] Y. Z. Zhu, G. D. Chen, H. Ye, A. Walsh, C. Y. Moon, and S.-H. Wei, "Electronic structure and phase stability of MgO, ZnO, CdO, and related ternary alloys," *Phys. Rev. B*, vol. 77, no. 24, p. 245209, Jun. 2008, doi: 10.1103/PhysRevB.77.245209.

[49] W. J. Kim, J. H. Leem, M. S. Han, I.-W. Park, Y. R. Ryu, and T. S. Lee, "Crystalline properties of wide band gap BeZnO films," *J. Appl. Phys.*, vol. 99, no. 9, p. 096104, May 2006, doi: 10.1063/1.2195117.

[50] L. Liu and J. H. Edgar, "Substrates for gallium nitride epitaxy," *Mater. Sci. Eng. R Rep.*, vol. 37, no. 3, pp. 61–127, Apr. 2002, doi: 10.1016/S0927-796X(02)00008-6.

[51] H. Nian, S. H. Hahn, K.-K. Koo, E. W. Shin, and E. J. Kim, “Sol–gel derived N-doped ZnO thin films,” *Mater. Lett.*, vol. 63, no. 26, pp. 2246–2248, Oct. 2009, doi: 10.1016/j.matlet.2009.07.038.
[52] V. Musat, B. Teixeira, E. Fortunato, R. C. C. Monteiro, and P. Vilarinho, “Al-doped ZnO thin films by sol–gel method,” *Surf. Coat. Technol.*, vol. 180–181, pp. 659–662, Mar. 2004, doi: 10.1016/j.surfcoat.2003.10.112.
[53] A. A. Al-Ghamdi, O. A. Al-Hartomy, M. El Okr, A. M. Nawar, S. El-Gazzar, F. El-Tantawy, and F. Yakuphanoglu, “Semiconducting properties of Al doped ZnO thin films,” *Spectrochim. Acta. A. Mol. Biomol. Spectrosc.*, vol. 131, pp. 512–517, Oct. 2014, doi: 10.1016/j.saa.2014.04.020.
[54] M. Kashif, S. M. U. Ali, M. E. Ali, H. I. Abdulgafour, U. Hashim, M. Willander, and Z. Hassan, “Morphological, optical, and Raman characteristics of ZnO nanoflakes prepared via a sol–gel method,” *Phys. Status Solidi A*, vol. 209, no. 1, pp. 143–147, 2012, doi: https://doi.org/10.1002/pssa.201127357.
[55] N. Fathima, N. Pradeep, V. Uma, and J. Balakrishnan, “Growth and characterization of ZnO nanocones on flexible substrate by hydrothermal method,” *Mater. Today Proc.*, vol. 9, pp. 247–255, Jan. 2019, doi: 10.1016/j.matpr.2019.02.156.
[56] M. Taheri, H. Abdizadeh, and M. R. Golobostanfard, “Hierarchical ZnO nanoflowers and urchin-like shapes synthesized via sol-gel electrophoretic deposition with enhanced photocatalytic performance,” *Mater. Chem. Phys.*, vol. 220, pp. 118–127, Dec. 2018, doi: 10.1016/j.matchemphys.2018.08.043.
[57] J.-S. Huang and C.-F. Lin, “Influences of ZnO sol-gel thin film characteristics on ZnO nanowire arrays prepared at low temperature using all solution-based processing,” *J. Appl. Phys.*, vol. 103, no. 1, p. 014304, Jan. 2008, doi: 10.1063/1.2828172.
[59] W. Jo, S.-J. Kim, and D.-Y. Kim, “Analysis of the etching behavior of ZnO ceramics,” *Acta Mater.*, vol. 53, no. 15, pp. 4185–4188, Sep. 2005, doi: 10.1016/j.actamat.2005.05.017.
[60] J.-M. Lee, K.-K. Kim, C.-K. Hyun, H. Tampo, and S. Niki, “Microstructural Evolution of ZnO by Wet-Etching Using Acidic Solutions,” *J. Nanosci. Nanotechnol.*, vol. 6, no. 11, pp. 3364–3368, Nov. 2006, doi: 10.1166/jnn.2006.011.
[61] G. Neumann, “On the Defect Structure of Zinc-Doped Zinc Oxide,” *Phys. Status Solidi B*, vol. 105, no. 2, pp. 605–612, 1981, doi: 10.1002/pssb.2221050220.
[62] C. G. Van de Walle, “Hydrogen as a Cause of Doping in Zinc Oxide,” *Phys. Rev. Lett.*, vol. 85, no. 5, pp. 1012–1015, Jul. 2000, doi: 10.1103/PhysRevLett.85.1012.
[63] Z. Du, X. Liu, Y. Zhang, J. Shuai, and H. Li, “Robust AZO/i-ZnO bilayer front contact for high-performance thin film solar cells,” *RSC Adv.*, vol. 6, no. 109, pp. 108067–108074, Nov. 2016, doi: 10.1039/C6RA23605G.
[64] K. Ellmer and A. Klein, “ZnO and Its Applications,” in *Transparent Conductive Zinc Oxide: Basics and Applications in Thin Film Solar Cells*, K. Ellmer, A. Klein, and B. Rech, Eds. Berlin, Heidelberg: Springer, 2008, pp. 1–33.
[65] E. A. Secco, “Decomposition Of Zinc Oxide,” *Can. J. Chem.*, vol. 38, no. 4, pp. 596–601, Apr. 1960, doi: 10.1139/v60-084.
[66] J. Zemann, “Crystal structures, 2nd edition. Vol. 1 by R. W. G. Wyckoff,” *Acta Crystallogr.*, vol. 18, no. 1, pp. 139–139, 1965, doi: 10.1107/S0365110X65000361.

[67] S. I. Najafi, T. Touam, R. Sara, M. P. Andrews, and M. A. Fardad, “Sol-gel glass waveguide and grating on silicon,” *J. Light. Technol.*, vol. 16, no. 9, pp. 1640–1646, Sep. 1998, doi: 10.1109/50.712247.
[68] O. A. Shilova, “Synthesis and structure features of composite silicate and hybrid TEOS-derived thin films doped by inorganic and organic additives,” *J. Sol-Gel Sci. Technol.*, vol. 68, no. 3, pp. 387–410, Dec. 2013, doi: 10.1007/s10971-013-3026-5.
[69] X. Zhang, Y. Wu, S. He, and D. Yang, “Structural characterization of sol–gel composites using TEOS/MEMO as precursors,” *Surf. Coat. Technol.*, vol. 201, no. 12, pp. 6051–6058, Mar. 2007, doi: 10.1016/j.surfcoat.2006.11.012.
[70] A. Venkateswara Rao and S. D. Bhagat, “Synthesis and physical properties of TEOS-based silica aerogels prepared by two step (acid–base) sol–gel process,” *Solid State Sci.*, vol. 6, no. 9, pp. 945–952, Sep. 2004, doi: 10.1016/j.solidstatesciences.2004.04.010.
[71] K. Nowak, R. Tadaszak, T. Ryznar, L. Wozniak, A. Lukowiak, L. Golonka, and S. Patela, “Sol-gel-based optical waveguides on LTCC substrates,” in *2008 31st International Spring Seminar on Electronics Technology*, May 2008, pp. 518–522, doi: 10.1109/ISSE.2008.5276621.
[72] H. Bartsch, U. Brokmann, B. Goj, R. Weiss, E. Rädlein, and J. Müller, “Sol gel thin films on LTCC ceramic multilayers enable their use as thin film substrates,” in *2015 European Microelectronics Packaging Conference (EMPC)*, Sep. 2015, pp. 1–6.
[73] W. Lee and S.-J. Park, “Porous Anodic Aluminum Oxide: Anodization and Templated Synthesis of Functional Nanostructures,” *Chem. Rev.*, vol. 114, no. 15, pp. 7487–7556, Aug. 2014, doi: 10.1021/cr500002z.
[74] K. Nielsch, J. Choi, K. Schwirn, R. B. Wehrspohn, and U. Gösele, “Self-ordering Regimes of Porous Alumina: The 10 Porosity Rule,” *Nano Lett.*, vol. 2, no. 7, pp. 677–680, Jul. 2002, doi: 10.1021/nl025537k.
[75] M. Nakao, S. Oku, H. Tanaka, Y. Shibata, A. Yokoo, T. Tamamura, and H. Masuda, “Fabrication of GaAs hole array as a 2D-photonic crystal and their application to photonic bandgap waveguide,” *Opt. Quantum Electron.*, vol. 34, no. 1, pp. 183–193, Jan. 2002, doi: 10.1023/A:1013329631972.
[76] W. Zhou, J. Zhang, X. Li, Y. Liu, G. Min, Z. Song, and J. Zhang, “Replication of mold for UV-nanoimprint lithography using AAO membrane,” *Appl. Surf. Sci.*, vol. 255, no. 18, pp. 8019–8022, Jun. 2009, doi: 10.1016/j.apsusc.2009.05.006.
[77] Z. Zeng, X. Huang, Z. Yin, H. Li, Y. Chen, H. Li, Q. Zhang, J. Ma, F. Boey, and H. Zhang, “Fabrication of Graphene Nanomesh by Using an Anodic Aluminum Oxide Membrane as a Template,” *Adv. Mater.*, vol. 24, no. 30, pp. 4138–4142, 2012, doi: https://doi.org/10.1002/adma.201104281.
[78] H. Robatjazi, S. M. Bahauddin, L. H. Macfarlan, S. Fu, and I. Thomann, “Ultrathin AAO Membrane as a Generic Template for Sub-100 nm Nanostructure Fabrication,” *Chem. Mater.*, vol. 28, no. 13, pp. 4546–4553, Jul. 2016, doi: 10.1021/acs.chemmater.6b00722.
[79] K. Liu, P. R. Ohodnicki, X. Kong, S. S. Lee, and H. Du, “Plasmonic Au nanorods stabilized within anodic aluminum oxide pore channels against high-temperature treatment,” *Nanotechnology*, vol. 30, no. 40, p. 405704, Oct. 2019, doi: 10.1088/1361-6528/ab2a3f.
[80] Q. Hao, H. Huang, X. Fan, X. Hou, Y. Yin, W. Li, L. Si, H. Nan, H. Wang, Y. Mei, T. Qiu, and P. K. Chu, “Facile design of ultra-thin anodic aluminum oxide membranes for the

fabrication of plasmonic nanoarrays," *Nanotechnology*, vol. 28, no. 10, p. 105301, Jan. 2017, doi: 10.1088/1361-6528/aa596d.
[81] A. Saedi and M. Ghorbani, "Electrodeposition of Ni–Fe–Co alloy nanowire in modified AAO template," *Mater. Chem. Phys.*, vol. 91, no. 2, pp. 417–423, Jun. 2005, doi: 10.1016/j.matchemphys.2004.12.001.
[82] S. Thongmee, H. L. Pang, J. Ding, J. B. Yi, and J. Y. Lin, "Fabrication and magnetic properties of metal nanowires via AAO templates," in *2008 2nd IEEE International Nanoelectronics Conference*, Mar. 2008, pp. 1116–1120, doi: 10.1109/INEC.2008.4585678.
[83] N. Kumar, A. K. Srivastava, R. Nath, B. Kumar Gupta, and G. D. Varma, "Probing the highly efficient room temperature ammonia gas sensing properties of a luminescent ZnO nanowire array prepared via an AAO-assisted template route," *Dalton Trans.*, vol. 43, no. 15, pp. 5713–5720, 2014, doi: 10.1039/C3DT53305K.
[84] C. V. Manzano, J. P. Best, J. J. Schwiedrzik, A. Cantarero, J. Michler, and L. Philippe, "The influence of thickness, interpore distance and compositional structure on the optical properties of self-ordered anodic aluminum oxide films," *J. Mater. Chem. C*, vol. 4, no. 32, pp. 7658–7666, 2016, doi: 10.1039/C6TC01904H.
[85] S.-K. Hwang, S.-H. Jeong, H.-Y. Hwang, O.-J. Lee, and K.-H. Lee, "Fabrication of highly ordered pore array in anodic aluminum oxide," *Korean J. Chem. Eng.*, vol. 19, no. 3, pp. 467–473, May 2002, doi: 10.1007/BF02697158.
[86] L. Vojkuvka, L. F. Marsal, and J. Pallares, "Study of Porous Alumina Porosity after Pore Widening Process," in *2007 Spanish Conference on Electron Devices*, Jan. 2007, pp. 41–43, doi: 10.1109/SCED.2007.383991.
[87] R. S. Sabry and R. Alobaid, "Effect of Preparation Conditions on Anodic Aluminum Oxide (AAO) Shape's and Size," vol. 3, no. 12, p. 7, 2012.
[88] C. Bienert and A. Roosen, "Characterization and improvement of LTCC composite materials for application at elevated temperatures," *J. Eur. Ceram. Soc.*, vol. 30, no. 2, pp. 369–374, Jan. 2010, doi: 10.1016/j.jeurceramsoc.2009.05.023.
[89] H. W. Stetson, "Method of making multilayer circuits," US3189978 A, Jun. 22, 1965.
[90] Y. Imanaka, *Multilayered Low Temperature Cofired Ceramics (LTCC) Technology*. Springer US, 2005.
[91] M. T. Sebastian and H. Jantunen, "Low loss dielectric materials for LTCC applications: a review," *Int. Mater. Rev.*, vol. 53, no. 2, pp. 57–90, Mar. 2008, doi: 10.1179/174328008X277524.
[92] N. Gutzeit, A. Schulz, M. Fischer, T. Thelemann, and J. Müller, "Picosecond Laser Structuring Technology for LTCC - the Improvement of Fine Line Structuring," in *2019 22nd European Microelectronics and Packaging Conference Exhibition (EMPC)*, Sep. 2019, pp. 1–5, doi: 10.23919/EMPC44848.2019.8951813.
[93] "White Papers | PRFI | Technology Overview LTCC," *PRFI*. https://www.prfi.com/resources/white-papers/ (accessed Nov. 26, 2020).
[94] N. Ding, L. M. Xu, B. J. Wu, and G. R. Gu, "The Preparation of the Highly Preferred Orientation of AlN Thin Films on ZnO Substrates," *Advanced Materials Research*, 2013. https://www.scientific.net/AMR.669.181 (accessed Nov. 27, 2020).
[95] A. Bittner, A. Ababneh, H. Seidel, and U. Schmid, "Influence of the crystal orientation on the electrical properties of AlN thin films on LTCC substrates," *Appl. Surf. Sci.*, vol. 257, no. 3, pp. 1088–1091, Nov. 2010, doi: 10.1016/j.apsusc.2010.08.019.

[96] H. Bartsch, R. Grieseler, J. Mánuel, J. Pezoldt, and J. Müller, “Magnetron Sputtered AlN Layers on LTCC Multilayer and Silicon Substrates,” *Coatings*, vol. 8, no. 8, Art. no. 8, Aug. 2018, doi: 10.3390/coatings8080289.
[97] J. W. Lee, J. J. Cuomo, Y. S. Cho, and R. L. Keusseyan, “Aluminum Nitride Thin Films on an LTCC Substrate,” *J. Am. Ceram. Soc.*, vol. 88, no. 7, pp. 1977–1980, doi: 10.1111/j.1551-2916.2005.00250.x.
[98] P. Panda, R. Ramaseshan, N. Ravi, G. Mangamma, F. Jose, S. Dash, K. Suzuki, and H. Suematsu, “Reduction of residual stress in AlN thin films synthesized by magnetron sputtering technique,” *Mater. Chem. Phys.*, vol. 200, pp. 78–84, Oct. 2017, doi: 10.1016/j.matchemphys.2017.07.072.
[99] M. Gierczak, P. Markowski, and A. Dziedzic, “Design, fabrication and characterization of LTCC-based electromagnetic microgenerators,” *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 113, p. 012011, Feb. 2016, doi: 10.1088/1757-899X/113/1/012011.
[100] H. Cobas Gomez, R. Mansini Cardoso, J. de Novais Schianti, A. Marim de Oliveira, and M. R. Gongora-Rubio, “Fab on a Package: LTCC Microfluidic Devices Applied to Chemical Process Miniaturization,” *Micromachines*, vol. 9, no. 6, Jun. 2018, doi: 10.3390/mi9060285.
[101] A. C. Schmitz, A. T. Ping, M. A. Khan, Q. Chen, J. W. Yang, and I. Adesida, “Schottky barrier properties of various metals on n-type GaN,” *Semicond. Sci. Technol.*, vol. 11, no. 10, p. 1464, 1996, doi: 10.1088/0268-1242/11/10/002.
[102] G. Greco, F. Iucolano, and F. Roccaforte, “Ohmic contacts to Gallium Nitride materials,” *Appl. Surf. Sci.*, vol. 383, no. Supplement C, pp. 324–345, Oct. 2016, doi: 10.1016/j.apsusc.2016.04.016.
[103] A. Motayed, A. v. Davydov, W. J. Boettinger, D. Josell, A. j. Shapiro, I. Levin, T. Zheleva, and G. L. Harris, “Realization of improved metallization-Ti/Al/Ti/W/Au ohmic contacts to n-GaN for high temperature application,” *Phys. Status Solidi C*, vol. 2, no. 7, pp. 2536–2539, May 2005, doi: 10.1002/pssc.200461604.
[104] Y. Sun, X. M. Shen, J. Wang, D. G. Zhao, G. Feng, Y. Fu, S. M. Zhang, Z. H. Zhang, Z. H. Feng, Y. X. Bai, and H. Yang, “Thermal annealing behaviour of Ni/Au on n-GaN Schottky contacts*,” *J. Phys. Appl. Phys.*, vol. 35, no. 20, pp. 2648–2651, Oct. 2002, doi: 10.1088/0022-3727/35/20/326.
[105] S. Young Moon, J. Ho Son, K. Jin Choi, J.-L. Lee, and H. W. Jang, “Indium as an efficient ohmic contact to N-face n-GaN of GaN-based vertical light-emitting diodes,” *Appl. Phys. Lett.*, vol. 99, no. 20, p. 202106, Nov. 2011, doi: 10.1063/1.3662421.
[106] “Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe | Wiley,” *Wiley.com*. https://www.wiley.com/en-us/Properties+of+Advanced+Semiconductor+Materials%3A+GaN%2C+AIN%2C+InN%2C+BN%2C+SiC%2C+SiGe-p-9780471358275 (accessed Nov. 28, 2020).
[107] S.-C. Lee, M.-W. Ha, J.-Y. Lim, J.-C. Her, K.-S. Seo, and M.-K. Han, “Suppression of Leakage Current of Ni/Au Schottky Barrier Diode Fabricated on AlGaN/GaN Heterostructure by Oxidation,” *Jpn. J. Appl. Phys.*, vol. 45, no. 4B, pp. 3398–3400, Apr. 2006, doi: 10.1143/JJAP.45.3398.
[108] M.-W. Ha, M.-K. Han, and C.-K. Hahn, “Effects of post-oxidation on leakage current of high-voltage AlGaN/GaN Schottky barrier diodes on Si(111) substrates,” *Solid-State Electron.*, vol. 81, pp. 1–4, Mar. 2013, doi: 10.1016/j.sse.2012.11.006.

[109] “Nitride Semiconductors and Devices | Hadis Morkoç | Springer.” https://www.springer.com/gp/book/9783540640387 (accessed Dec. 13, 2020).
[110] S. K. Cheung and N. W. Cheung, “Extraction of Schottky diode parameters from forward current-voltage characteristics,” *Appl. Phys. Lett.*, vol. 49, no. 2, pp. 85–87, 1986.
[111] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, “Band parameters for III–V compound semiconductors and their alloys,” *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815–5875, Jun. 2001, doi: 10.1063/1.1368156.
[112] J. Wu, W. Walukiewicz, W. Shan, K. M. Yu, J. W. A. Iii, S. X. Li, E. E. Haller, H. Lu, and W. J. Schaff, “Temperature dependence of the fundamental band gap of InN,” *J. Appl. Phys.*, vol. 94, no. 7, pp. 4457–4460, Oct. 2003, doi: 10.1063/1.1605815.
[113] J. Watson and G. Castro, “A review of high-temperature electronics technology and applications,” *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 12, pp. 9226–9235, Dec. 2015, doi: 10.1007/s10854-015-3459-4.
[114] A. Hassan, Y. Savaria, and M. Sawan, “Electronics and Packaging Intended for Emerging Harsh Environment Applications: A Review,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 26, no. 10, pp. 2085–2098, Oct. 2018, doi: 10.1109/TVLSI.2018.2834499.
[115] A. Kurtz, A. A. Ned, and A. Epstein, “Improved Ruggedized SOI Transducers Operational Above 600 ° C,” 2004. /paper/Improved-Ruggedized-SOI-Transducers-Operational-600-Kurtz-Ned/6368d5485d57df21aef4d24689d636d6f25071a5 (accessed Dec. 09, 2020).
[116] D. Maier, M. Alomari, N. Grandjean, J.- Carlin, M.- Diforte-Poisson, C. Dua, S. Delage, and E. Kohn, “InAlN/GaN HEMTs for Operation in the 1000 $^\circ \hboxC$ Regime: A First Experiment,” *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 985–987, Jul. 2012, doi: 10.1109/LED.2012.2196972.
[117] “GaN and Related Materials II,” *Routledge & CRC Press*. https://www.routledge.com/GaN-and-Related-Materials-II/Pearton/p/book/9789056996864 (accessed Dec. 12, 2020).
[118] J. S. Foresi and T. D. Moustakas, “Metal contacts to gallium nitride,” *Appl. Phys. Lett.*, vol. 62, no. 22, pp. 2859–2861, May 1993, doi: 10.1063/1.109207.
[119] H. S. Venugopalan, S. E. Mohney, B. P. Luther, S. D. Wolter, and J. M. Redwing, “Interfacial reactions between nickel thin films and GaN,” *J. Appl. Phys.*, vol. 82, no. 2, pp. 650–654, Jul. 1997, doi: 10.1063/1.365593.
[120] Q. Z. Liu, L. S. Yu, F. Deng, S. S. Lau, and J. M. Redwing, “Ni and Ni silicide Schottky contacts on n-GaN,” *J. Appl. Phys.*, vol. 84, no. 2, pp. 881–886, Jun. 1998, doi: 10.1063/1.368151.
[121] A. Kumar, M. Latzel, S. Christiansen, V. Kumar, and R. Singh, “Effect of rapid thermal annealing on barrier height and 1/f noise of Ni/GaN Schottky barrier diodes,” *Appl. Phys. Lett.*, vol. 107, no. 9, p. 093502, Aug. 2015, doi: 10.1063/1.4929829.
[122] M. F. Khan, F. A. Ghavanini, S. Haasl, L. Löfgren, K. Persson, C. Rusu, K. Schjølberg-Henriksen, and P. Enoksson, “Methods for characterization of wafer-level encapsulation applied on silicon to LTCC anodic bonding,” *J. Micromechanics Microengineering*, vol. 20, no. 6, p. 064020, Jun. 2010, doi: 10.1088/0960-1317/20/6/064020.
[123] AMETEK, “Coining 82AU 18In Solder Data Sheet,” [Online]. Available: https://www.ametek-ecp.com/-/media/ametek-ecp/v2/files/cw_datasheets_sds_cfsi/datasheets/au82in18%20data%20sheet.pdf?la=en.

[124] C. Faust-Ellsaesser, T. Proepper, K. Riester, and J. Duerr, “Life-time modeling of DBC-based MOSFET-power modules,” in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, Mar. 2016, pp. 1–5.
[125] S. Kasap and P. Capper, Eds., *Springer Handbook of Electronic and Photonic Materials*. .
[126] H. Iwanaga, A. Kunishige, and S. Takeuchi, “Anisotropic thermal expansion in wurtzite-type crystals,” *J. Mater. Sci.*, vol. 35, no. 10, pp. 2451–2454, May 2000, doi: 10.1023/A:1004709500331.
[128] L. Landau and B. Levich, “Dragging of a Liquid by a Moving Plate,” in *Dynamics of Curved Fronts*, P. Pelcé, Ed. San Diego: Academic Press, 1988, pp. 141–153.
[129] “Physics and Applications of DIP Coating and Spin Coating | MRS Online Proceedings Library (OPL) | Cambridge Core.” https://www.cambridge.org/core/journals/mrs-online-proceedings-library-archive/article/physics-and-applications-of-dip-coating-and-spin-coating/CDF5D7C6BF44B3F923D6E2B6719D512F (accessed Nov. 02, 2020).
[130] T. Schneller, R. Waser, M. Kosec, and D. Payne, Eds., *Chemical Solution Deposition of Functional Oxide Thin Films*. Wien: Springer-Verlag, 2013.
[131] M. Faustini, B. Louis, P. A. Albouy, M. Kuemmel, and D. Grosso, “Preparation of Sol−Gel Films by Dip-Coating in Extreme Conditions,” *J. Phys. Chem. C*, vol. 114, no. 17, pp. 7637–7645, May 2010, doi: 10.1021/jp9114755.
[132] “Dip Coating Theory | Dip Coating Thin Films, Complete Guide,” *Ossila*. https://www.ossila.com/pages/dip-coating-theory-film-thickness (accessed Nov. 02, 2020).
[133] “Spin Coating, A Complete Guide to Theory and Techniques,” *Ossila*. https://www.ossila.com/pages/spin-coating (accessed Oct. 02, 2019).
[134] L. Znaidi, “Sol–gel-deposited ZnO thin films: A review,” *Mater. Sci. Eng. B*, vol. 174, no. 1, pp. 18–30, Oct. 2010, doi: 10.1016/j.mseb.2010.07.001.
[135] M. H. Nateq and R. Ceccato, “Enhanced Sol–Gel Route to Obtain a Highly Transparent and Conductive Aluminum-Doped Zinc Oxide Thin Film,” *Materials*, vol. 12, no. 11, p. 1744, Jan. 2019, doi: 10.3390/ma12111744.
[136] D. T. Speaks, “Effect of concentration, aging, and annealing on sol gel ZnO and Al-doped ZnO thin films,” *Int. J. Mech. Mater. Eng.*, vol. 15, no. 1, p. 2, Jan. 2020, doi: 10.1186/s40712-019-0113-6.
[137] “Physical Properties of Solvents.” Sigma Aldrich, Accessed: Nov. 04, 2020. [Online]. Available: https://www.sigmaaldrich.com/content/dam/sigma-aldrich/docs/Aldrich/General_Information/labbasics_pg144.pdf.
[138] M. S. Tokumoto, V. Briois, C. V. Santilli, and S. H. Pulcinelli, “Preparation of ZnO Nanoparticles: Structural Study of the Molecular Precursor,” *J. Sol-Gel Sci. Technol.*, vol. 26, no. 1, pp. 547–551, Jan. 2003, doi: 10.1023/A:1020711702332.
[139] P. Hosseini Vajargah, H. Abdizadeh, R. Ebrahimifard, and M. R. Golobostanfard, “Sol–gel derived ZnO thin films: Effect of amino-additives,” *Appl. Surf. Sci.*, vol. 285, pp. 732–743, Nov. 2013, doi: 10.1016/j.apsusc.2013.08.118.
[140] L. Spanhel, “Colloidal ZnO nanostructures and functional coatings: A survey,” *J. Sol-Gel Sci. Technol.*, vol. 39, no. 1, pp. 7–24, Jul. 2006, doi: 10.1007/s10971-006-7302-5.
[141] L. Znaidi, G. J. A. A. Soler Illia, S. Benyahia, C. Sanchez, and A. V. Kanaev, “Oriented ZnO thin films synthesis by sol–gel process for laser application,” *Thin Solid Films*, vol. 428, no. 1, pp. 257–262, Mar. 2003, doi: 10.1016/S0040-6090(02)01219-1.

[142] M. Ohyama, H. Kouzuka, and T. Yoko, “Sol-gel preparation of ZnO films with extremely preferred orientation along (002) plane from zinc acetate solution,” *Thin Solid Films*, vol. 306, no. 1, pp. 78–85, Aug. 1997, doi: 10.1016/S0040-6090(97)00231-9.
[143] N. Kaneva and C. Dushkin, “Preparation of nanocrystalline thin films of ZnO by sol-gel dip coating,” *Bulg. Chem. Commun.*, vol. 43, pp. 259–263, Jan. 2011.
[144] W. R. Saleh, N. M. Saeed, W. A. Twej, and M. Alwan, “Synthesis Sol-Gel Derived Highly Transparent ZnO Thin Films for Optoelectronic Applications,” *Adv. Mater. Phys. Chem.*, vol. 2, no. 1, Art. no. 1, Mar. 2012, doi: 10.4236/ampc.2012.21002.
[145] F. Maldonado and A. Stashans, “Al-doped ZnO: Electronic, electrical and structural properties,” *J. Phys. Chem. Solids*, vol. 71, no. 5, pp. 784–787, May 2010, doi: 10.1016/j.jpcs.2010.02.001.
[146] M. U. Shahid, K. M. Deen, A. Ahmad, M. A. Akram, M. Aslam, and W. Akhtar, “Formation of Al-doped ZnO thin films on glass by sol–gel process and characterization,” *Appl. Nanosci.*, vol. 6, no. 2, pp. 235–241, Feb. 2016, doi: 10.1007/s13204-015-0425-7.
[147] P. Banerjee, W.-J. Lee, K.-R. Bae, S. B. Lee, and G. W. Rubloff, “Structural, electrical, and optical properties of atomic layer deposition Al-doped ZnO films,” *J. Appl. Phys.*, vol. 108, no. 4, p. 043504, Aug. 2010, doi: 10.1063/1.3466987.
[148] P. Praserthdam, J. Phungphadung, P. Somrang, A. Kunyanucharat, P. Silveston, and W. Tanakulrungsank, “Critical nanoparticle size for thermal stability,” *J. Mater. Sci. Lett.*, vol. 22, no. 22, pp. 1587–1589, Nov. 2003, doi: 10.1023/A:1026332424083.
[149] “Dip Coating: Practical Guide to Theory and Troubleshooting,” *Ossila*. https://www.ossila.com/pages/dip-coating (accessed Mar. 16, 2021).
[150] J. Meng and Y. Jaluria, “Numerical Simulation of GaN Growth in a Metalorganic Chemical Vapor Deposition Process,” *J. Manuf. Sci. Eng.*, vol. 135, no. 061013, Nov. 2013, doi: 10.1115/1.4025781.
[151] T. Yoshida, Y. Oshima, K. Watanabe, T. Tsuchiya, and T. Mishima, “Ultrahigh-speed growth of GaN by hydride vapor phase epitaxy,” *Phys. Status Solidi C*, vol. 8, no. 7–8, pp. 2110–2112, 2011, doi: https://doi.org/10.1002/pssc.201000953.
[152] D. J. G. Speight, *Lange’s Handbook of Chemistry, Seventeenth Edition*. McGraw-Hill Education, 2017.
[153] K. Rönnby, S. C. Buttera, P. Rouf, S. T. Barry, L. Ojamäe, and H. Pedersen, “Methylamines as Nitrogen Precursors in Chemical Vapor Deposition of Gallium Nitride,” *J. Phys. Chem. C*, vol. 123, no. 11, pp. 6701–6710, Mar. 2019, doi: 10.1021/acs.jpcc.9b00482.
[154] J.-H. Boo, S.-B. Lee, Y.-S. Kim, J. T. Park, K.-S. Yu, and Y. Kim, “Growth of AlN and GaN Thin Films on Si(100) Using New Single Molecular Precursors by MOCVD Method,” *Phys. Status Solidi A*, vol. 176, no. 1, pp. 711–717, 1999, doi: https://doi.org/10.1002/(SICI)1521-396X(199911)176:1<711::AID-PSSA711>3.0.CO;2-Y.
[155] D. K. Gaskill, N. Bottka, and M. C. Lin, “Growth of GaN films using trimethylgallium and hydrazine,” *Appl. Phys. Lett.*, vol. 48, no. 21, pp. 1449–1451, May 1986, doi: 10.1063/1.96886.
[156] “GaN on SiC HEMTs and MMICs - Cree Wolfspeed | DigiKey.” https://www.digikey.ca/en/product-highlight/c/cree-wolfspeed/gan-on-sic-hemts-and-mmics (accessed Jan. 08, 2021).

[157] "XLamp XT-E High-Efficacy White LEDs - Cree | DigiKey." https://www.digikey.ca/en/product-highlight/c/cree/xlamp-xt-e-high-efficacy-white-leds (accessed Jan. 08, 2021).
[158] D. Kum and D. Byun, "The effect of substrate surface roughness on GaN growth using MOCVD process," *J. Electron. Mater.*, vol. 26, no. 10, pp. 1098–1102, Oct. 1997, doi: 10.1007/s11664-997-0001-3.
[159] G. Namkoong, W. A. Doolittle, A. S. Brown, M. Losurdo, P. Capezzuto, and G. Bruno, "Role of Sapphire Nitridation Temperature on GaN Growth by Plasma Assisted Molecular Beam Epitaxy: Part I. Impact of the Nitridation Chemistry on Material Characteristics," *J. Appl. Phys.*, vol. 91, no. 4, pp. 2499–2507, Jan. 2002, doi: 10.1063/1.1435834.
[160] A. Wierzbicka, Z. R. Zytkiewicz, S. Kret, J. Borysiuk, P. Dluzewski, M. Sobanska, K. Klosek, A. Reszka, G. Tchutchulashvili, A. Cabaj, and E. Lusakowska, "Influence of substrate nitridation temperature on epitaxial alignment of GaN nanowires to Si(111) substrate," *Nanotechnology*, vol. 24, no. 3, p. 035703, Dec. 2012, doi: 10.1088/0957-4484/24/3/035703.
[161] T. Ito, M. Sumiya, Y. Takano, K. Ohtsuka, and S. Fuke, "Influence of Thermal Annealing on GaN Buffer Layers and the Property of Subsequent GaN Layers Grown by Metalorganic Chemical Vapor Deposition," *Jpn. J. Appl. Phys.*, vol. 38, no. 2R, p. 649, Feb. 1999, doi: 10.1143/JJAP.38.649.
[162] C. Y. Hwang, M. J. Schurman, W. E. Mayo, Y. C. Lu, R. A. Stall, and T. Salagaj, "Effect of structural defects and chemical impurities on hall mobilities in low pressure MOCVD grown GaN," *J. Electron. Mater.*, vol. 26, no. 3, pp. 243–251, Mar. 1997, doi: 10.1007/s11664-997-0158-9.
[163] C. Pelosi, G. Attolini, C. Bocchi, P. Franzosi, C. Frigeri, M. Berti, A. V. Drigo, and F. Romanato, "The role of the V/III ratio in the growth and structural properties of metalorganic vapor phase epitaxy GaAs/Ge heterostructures," *J. Electron. Mater.*, vol. 24, no. 11, pp. 1723–1730, Nov. 1995, doi: 10.1007/BF02676841.
[164] S. Nakamura, Y. Harada, and M. Seno, "Novel metalorganic chemical vapor deposition system for GaN growth," *Appl. Phys. Lett.*, vol. 58, no. 18, pp. 2021–2023, May 1991, doi: 10.1063/1.105239.
[165] C. Sone, M. Hong Kim, H. Jin Kim, and E. Yoon, "Effects of hydrogen on carbon incorporation in GaN grown by remote plasma-enhanced metal-organic chemical vapor deposition," *J. Cryst. Growth*, vol. 189–190, pp. 321–324, Jun. 1998, doi: 10.1016/S0022-0248(98)00278-4.
[166] Y. Lu, H. Kondo, K. Ishikawa, O. Oda, K. Takeda, M. Sekine, H. Amano, and M. Hori, "Epitaxial growth of GaN by radical-enhanced metalorganic chemical vapor deposition (REMOCVD) in the downflow of a very high frequency (VHF) N2/H2 excited plasma – effect of TMG flow rate and VHF power," *J. Cryst. Growth*, vol. 391, pp. 97–103, Apr. 2014, doi: 10.1016/j.jcrysgro.2014.01.014.
[167] Y. Horikoshi, "Flow Rate Modulated Vapor Epitaxy," in *Reference Module in Materials Science and Materials Engineering*, Elsevier, 2016.
[168] R. S. Q. Fareed, R. Jain, R. Gaska, M. S. Shur, J. Wu, W. Walukiewicz, and M. A. Khan, "High quality InN/GaN heterostructures grown by migration enhanced metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 84, no. 11, pp. 1892–1894, Mar. 2004, doi: 10.1063/1.1686889.

[169] Q. Fareed, R. Gaska, and M. S. Shur, "Migration Enhanced Metal Organic Chemical Vapor Deposition of AlN/GaN/InN-Based Heterostructures," in *International Semiconductor Device Research Symposium, 2003*, Dec. 2003, pp. 402–403, doi: 10.1109/ISDRS.2003.1272154.
[170] H. Lu, W. J. Schaff, J. Hwang, H. Wu, W. Yeo, A. Pharkya, and L. F. Eastman, "Improvement on epitaxial grown of InN by migration enhanced epitaxy," *Appl. Phys. Lett.*, vol. 77, no. 16, pp. 2548–2550, Oct. 2000, doi: 10.1063/1.1318235.
[171] K. Kusakabe, K. Kishino, A. Kikuchi, T. Yamada, D. Sugihara, and S. Nakamura, "Reduction of threading dislocations in migration enhanced epitaxy grown GaN with N-polarity by use of AlN multiple interlayer," *J. Cryst. Growth*, vol. 230, no. 3–4, pp. 387–391, Sep. 2001, doi: 10.1016/S0022-0248(01)01248-9.
[172] C. Adelmann, J. Brault, J.-L. Rouvière, H. Mariette, G. Mula, and B. Daudin, "Atomic-layer epitaxy of GaN quantum wells and quantum dots on (0001) AlN," *J. Appl. Phys.*, vol. 91, no. 8, pp. 5498–5500, Mar. 2002, doi: 10.1063/1.1458049.
[173] X. Liu, S. Ramanathan, A. Longdergan, A. Srivastava, E. Lee, T. E. Seidel, J. T. Barton, D. Pang, and R. G. Gordon, "ALD of Hafnium Oxide Thin Films from Tetrakis(ethylmethylamino)hafnium and Ozone," *J. Electrochem. Soc.*, vol. 152, no. 3, p. G213, Jan. 2005, doi: 10.1149/1.1859631.
[174] J. Sumakeris, Z. Sitar, K. S. Ailey-Trent, K. L. More, and R. F. Davis, "Layer-by-layer epitaxial growth of GaN at low temperatures," *Thin Solid Films*, vol. 225, no. 1, pp. 244–249, Mar. 1993, doi: 10.1016/0040-6090(93)90163-J.
[175] H. Eichhorn, K. H. Schoenbach, and T. Tessnow, "Paschen's law for a hollow cathode discharge," *Appl. Phys. Lett.*, vol. 63, no. 18, pp. 2481–2483, Nov. 1993, doi: 10.1063/1.110455.
[176] K. S. A. Butcher, D. Alexandrov, P. Terziyska, V. Georgiev, and D. Georgieva, "Initial experiments in the migration enhanced afterglow growth of gallium and indium nitride," *Phys. Status Solidi C*, vol. 9, no. 3–4, pp. 1070–1073, Mar. 2012, doi: 10.1002/pssc.201100209.
[177] "Nitrogen Data Sheet." Praxair, [Online]. Available: https://www.lindeus.com/-/media/corporate/praxairus/documents/specification-sheets-and-brochures/gases/nitrogen/nitrogen-n2-spec-sheet-ss-p4631.pdf?la=en.
[178] J. C. Zhang, D. G. Zhao, J. F. Wang, Y. T. Wang, J. Chen, J. P. Liu, and H. Yang, "The influence of AlN buffer layer thickness on the properties of GaN epilayer," *J. Cryst. Growth*, vol. 268, no. 1–2, pp. 24–29, Jul. 2004, doi: 10.1016/j.jcrysgro.2004.04.102.
[179] W.-C. Huang, C.-M. Chu, Y.-Y. Wong, K.-W. Chen, Y.-K. Lin, C.-H. Wu, W.-I. Lee, and E.-Y. Chang, "Investigations of GaN growth on the sapphire substrate by MOCVD method with different AlN buffer deposition temperatures," *Mater. Sci. Semicond. Process.*, vol. 45, no. Supplement C, pp. 1–8, Apr. 2016, doi: 10.1016/j.mssp.2016.01.008.
[180] S. Figge, T. Böttcher, S. Einfeldt, and D. Hommel, "In Situ and Ex Situ Evaluation of the Film Coalescence for GaN Growth on GaN Nucleation Layers," *J. Cryst. Growth*, vol. 221, no. 1, pp. 262–266, Dec. 2000, doi: 10.1016/S0022-0248(00)00696-5.
[181] W. Wang, Y. Lin, Y. Li, X. Li, L. Huang, Y. Zheng, Z. Lin, H. Wang, and G. Li, "High-efficiency vertical-structure GaN-based light-emitting diodes on Si substrates," *J. Mater. Chem. C*, vol. 6, no. 7, pp. 1642–1650, Feb. 2018, doi: 10.1039/C7TC04478J.
[182] O. Kelekci, P. Tasli, S. S. Cetin, M. Kasap, S. Ozcelik, and E. Ozbay, "Investigation of AlInN HEMT Structures with Different AlGaN Buffer Layers Grown on Sapphire

Substrates by MOCVD," *Curr. Appl. Phys.*, vol. 12, no. 6, pp. 1600–1605, Nov. 2012, doi: 10.1016/j.cap.2012.05.040.
[183] A. Able, W. Wegscheider, K. Engl, and J. Zweck, "Growth of crack-free GaN on Si(111) with graded AlGaN buffer layers," *J. Cryst. Growth*, vol. 276, no. 3, pp. 415–418, Apr. 2005, doi: 10.1016/j.jcrysgro.2004.12.003.
[184] Y. Sato, A. Kurosaki, and S. Sato, "Low-temperature growth of GaN and InxGa1−xN films on glass substrates," *J. Cryst. Growth*, vol. 189–190, pp. 42–46, Jun. 1998, doi: 10.1016/S0022-0248(98)00153-5.
[185] "Direct growth of single-crystalline III–V semiconductors on amorphous substrates." https://www.ncbi.nlm.nih.gov/pmc/articles/PMC4737854/ (accessed Oct. 08, 2019).
[186] J. H. Choi, H. Y. Ahn, Y. S. Lee, K. Park, T.-H. Kim, K. S. Cho, C. W. Baik, S. I. Kim, H. Yoo, E. H. Lee, B. L. Choi, S.-D. Kim, Y.-W. Kim, M. Kim, and S. Hwang, "GaN light-emitting diodes on glass substrates with enhanced electroluminescence," *J. Mater. Chem.*, vol. 22, no. 43, pp. 22942–22948, Oct. 2012, doi: 10.1039/C2JM34405J.
[187] J. H. Choi, A. Zoulkarneev, S. I. Kim, C. W. Baik, M. H. Yang, S. S. Park, H. Suh, U. J. Kim, H. Bin Son, J. S. Lee, M. Kim, J. M. Kim, and K. Kim, "Nearly single-crystalline GaN light-emitting diodes on amorphous glass substrates," *Nat. Photonics*, vol. 5, no. 12, pp. 763–769, Dec. 2011, doi: 10.1038/nphoton.2011.253.
[188] J. J. Jiménez, J. M. Mánuel, H. Bartsch, J. Breiling, R. García, H. O. Jacobs, J. Müller, J. Pezoldt, and F. M. Morales, "Comprehensive (S)TEM characterization of polycrystalline GaN/AlN layers grown on LTCC substrates," *Ceram. Int.*, Feb. 2019, doi: 10.1016/j.ceramint.2019.01.250.
[189] M. Godlewski, A. Szczerbakow, K. Kopalko, E. Lusakowska, K. S. A. Butcher, E. M. Goldys, T. L. Tansley, and A. Barski, "Atomic layer epitaxy of ZnO for substrates for GaN epitaxy," in *2002 Conference on Optoelectronic and Microelectronic Materials and Devices. COMMAD 2002. Proceedings (Cat. No.02EX601)*, Sydney, NSW, Australia, 2002, pp. 13–16, doi: 10.1109/COMMAD.2002.1237178.
[190] K. S. A. Butcher, and P. P.- Chen, M. Godlewski, A. Szczerbakow, E. M. Goldys, T. L. Tansley, and J. A. Freitas, "Glass substrates for GaN using ZnO buffer layers," in *COMMAD 2000 Proceedings. Conference on Optoelectronic and Microelectronic Materials and Devices*, Dec. 2000, pp. 535–538, doi: 10.1109/COMMAD.2000.1023005.
[191] J. W. Lee, S. W. Park, and J. B. Yoo, "The Application of a Low Temperature GaN Buffer Layer to Thick GaN Film Growth on ZnO/Si Substrate," *Phys. Status Solidi A*, vol. 176, no. 1, pp. 583–587, 1999, doi: https://doi.org/10.1002/(SICI)1521-396X(199911)176:1<583::AID-PSSA583>3.0.CO;2-6.
[192] X. Wei, R. Zhao, M. Shao, X. Xu, and J. Huang, "Fabrication and properties of ZnO/GaN heterostructure nanocolumnar thin film on Si (111) substrate," *Nanoscale Res. Lett.*, vol. 8, no. 1, p. 112, Feb. 2013, doi: 10.1186/1556-276X-8-112.
[193] K. Tang, S. Huang, S. Gu, S. Zhu, J. Ye, Z. Xu, and Y. Zheng, "The roles of buffer layer thickness on the properties of the ZnO epitaxial films," *Appl. Surf. Sci.*, vol. 388, pp. 557–564, Dec. 2016, doi: 10.1016/j.apsusc.2015.10.123.
[194] T. Ueda, T.-F. Huang, S. Spruytte, H. Lee, M. Yuri, K. Itoh, T. Baba, and J. S. Harris, "Vapor phase epitaxy growth of GaN on pulsed laser deposited ZnO buffer layer," *J. Cryst. Growth*, vol. 187, no. 3, pp. 340–346, May 1998, doi: 10.1016/S0022-0248(97)00886-5.

[195] M. A. L. Johnson, S. Fujita, W. H. Rowland, W. C. Hughes, J. W. Cook, and J. F. Schetzina, “MBE growth and properties of ZnO on sapphire and SiC substrates,” *J. Electron. Mater.*, vol. 25, no. 5, pp. 855–862, May 1996, doi: 10.1007/BF02666649.
[196] J. M. Mánuel, J. J. Jiménez, F. M. Morales, B. Lacroix, A. J. Santos, R. García, E. Blanco, M. Domínguez, M. Ramírez, A. M. Beltrán, D. Alexandrov, J. Tot, R. Dubreuil, V. Videkov, S. Andreev, B. Tzaneva, H. Bartsch, J. Breiling, J. Pezoldt, M. Fischer, and J. Müller, “Engineering of III-Nitride Semiconductors on Low Temperature Co-fired Ceramics,” *Sci. Rep.*, vol. 8, no. 1, p. 6879, May 2018, doi: 10.1038/s41598-018-25416-6.
[197] H. Bartsch, J. Pezoldt, F. M. M. Sanchez, J. J. J. Rios, J. M. M. Delgado, J. Breiling, and J. Müller, “LTCC as substrate - enabling semiconductor and packaging integration,” in *2019 22nd European Microelectronics and Packaging Conference Exhibition (EMPC)*, Sep. 2019, pp. 1–4, doi: 10.23919/EMPC44848.2019.8951794.
[198] H. Zhou, F. Chai, J. Fang, L. Shi, C. Cai, and S. Yuan, “Highly efficient colloid–solution deposition planarization of Hastelloy substrate for IBAD-MgO film,” *Res. Chem. Intermed.*, vol. 42, no. 5, pp. 4751–4758, May 2016, doi: 10.1007/s11164-015-2314-9.
[199] I. Martynova, D. Tsymbarenko, A. Kamenev, V. Amelichev, A. Molodyk, N. Kuzmina, and A. Kaul, “Solution deposition of ultrasmooth alumina on long-length metallic substrate for 2G superconducting tapes,” *Mater. Res. Bull.*, vol. 78, pp. 64–71, Jun. 2016, doi: 10.1016/j.materresbull.2016.02.014.
[200] A. C. Wulff, Y. Zhao, O. Mishin, and J.-C. Grivel, “Effect of Initial Surface Quality on Final Roughness and Texture of Annealed Ni-5at.%W Tapes Coated with a Gd2Zr2O7 Buffer Layer,” 2012, doi: 10.1007/S10948-011-1303-5.
[201] A. Vannozzi, A. Augieri, G. Celentano, A. Rufoloni, S. Rubanov, and T. Petrisor, “Development and characterization of biaxially-textured lanthanum zirconate film grown on cold-rolled Ni-W substrate by chemical solution deposition,” *J. Alloys Compd.*, vol. 735, pp. 454–463, Feb. 2018, doi: 10.1016/j.jallcom.2017.11.149.
[202] A. T. Elshafiey, K. M. DaVico, A. K. Rishinaramangalam, A. Rashidi, A. Aragon, D. Feezell, B. P. Gunning, C. Sheehan, and V. Matias, “GaN/InGaN Blue Light-Emitting Diodes on Polycrystalline Molybdenum Metal Foils by Ion Beam-Assisted Deposition,” *Phys. Status Solidi A*, vol. 217, no. 7, p. 1900800, 2020, doi: https://doi.org/10.1002/pssa.201900800.
[203] M. Vilardell, J. Fornell, J. Sort, R. Vlad, J. C. Fernández, J. Puig, A. Usoskin, A. Palau, T. Puig, X. Obradors, and A. Calleja, “Inkjet-Printed Chemical Solution Y2O3 Layers for Planarization of Technical Substrates,” *Coatings*, vol. 7, no. 12, Art. no. 12, Dec. 2017, doi: 10.3390/coatings7120227.
[204] B. Peng, D. Gong, W. Zhang, J. Jiang, L. Shu, and Y. Zhang, “Effects of Sputtering Parameters on AlN Film Growth on Flexible Hastelloy Tapes by Two-Step Deposition Technique,” *Materials*, vol. 9, no. 8, Art. no. 8, Aug. 2016, doi: 10.3390/ma9080686.
[205] “Fabrication and characterization of coated Hastelloy C-276 Alloy by SDP technology - IOPscience.” https://iopscience.iop.org/article/10.1088/2053-1591/ab6ad7 (accessed Dec. 09, 2020).
[206] B. A. Albiss and I. M. Obaidat, “Applications of YBCO-coated conductors: a focus on the chemical solution deposition method,” *J. Mater. Chem.*, vol. 20, no. 10, pp. 1836–1845, Feb. 2010, doi: 10.1039/B917294G.
[207] J. E. Northrup, “Theory of the (12_10) prismatic stacking fault in GaN,” *Appl. Phys. Lett.*, vol. 72, no. 18, pp. 2316–2318, May 1998, doi: 10.1063/1.121347.

[208] *Introduction to Dislocations*. Elsevier, 2011.
[209] X. J. Ning, F. R. Chien, P. Pirouz, J. W. Yang, and M. A. Khan, "Growth defects in GaN films on sapphire: The probable origin of threading dislocations," *J. Mater. Res.*, vol. 11, no. 3, pp. 580–592, Mar. 1996, doi: 10.1557/JMR.1996.0071.
[210] M. Albrecht, J. L. Weyher, B. Lucznik, I. Grzegory, and S. Porowski, "Nonradiative recombination at threading dislocations in n-type GaN: Studied by cathodoluminescence and defect selective etching," *Appl. Phys. Lett.*, vol. 92, no. 23, p. 231909, Jun. 2008, doi: 10.1063/1.2928226.
[211] J. W. P. Hsu, M. J. Manfra, D. V. Lang, S. Richter, S. N. G. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer, and R. J. Molnar, "Inhomogeneous spatial distribution of reverse bias leakage in GaN Schottky diodes," *Appl. Phys. Lett.*, vol. 78, no. 12, pp. 1685–1687, Mar. 2001, doi: 10.1063/1.1356450.
[212] J. W. P. Hsu, M. J. Manfra, R. J. Molnar, B. Heying, and J. S. Speck, "Direct imaging of reverse-bias leakage through pure screw dislocations in GaN films grown by molecular beam epitaxy on GaN templates," *Appl. Phys. Lett.*, vol. 81, no. 1, pp. 79–81, Jun. 2002, doi: 10.1063/1.1490147.
[213] J. Wang, H. You, H. Guo, J. Xue, G. Yang, D. Chen, B. Liu, H. Lu, R. Zhang, and Y. Zheng, "Do all screw dislocations cause leakage in GaN-based devices?," *Appl. Phys. Lett.*, vol. 116, no. 6, p. 062104, Feb. 2020, doi: 10.1063/1.5135960.
[214] I. Arslan and N. D. Browning, "Role of Oxygen at Screw Dislocations in GaN," *Phys. Rev. Lett.*, vol. 91, no. 16, p. 165501, Oct. 2003, doi: 10.1103/PhysRevLett.91.165501.
[215] E. J. Miller, D. M. Schaadt, E. T. Yu, C. Poblenz, C. Elsass, and J. S. Speck, "Reduction of reverse-bias leakage current in Schottky diodes on GaN grown by molecular-beam epitaxy using surface modification with an atomic force microscope," p. 7.
[216] O. Weidemann, E. Monroy, E. Hahn, M. Stutzmann, and M. Eickhoff, "Influence of thermal oxidation on the electronic properties of Pt Schottky contacts on GaN grown by molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. 86, no. 8, p. 083507, Feb. 2005, doi: 10.1063/1.1868863.
[217] C. Stampfl and C. G. Van de Walle, "Energetics and electronic structure of stacking faults in AlN, GaN, and InN," *Phys. Rev. B*, vol. 57, no. 24, pp. R15052–R15055, Jun. 1998, doi: 10.1103/PhysRevB.57.R15052.
[218] J. Lähnemann, U. Jahn, O. Brandt, T. Flissikowski, P. Dogan, and H. T. Grahn, "Luminescence associated with stacking faults in GaN," *J. Phys. Appl. Phys.*, vol. 47, no. 42, p. 423001, Oct. 2014, doi: 10.1088/0022-3727/47/42/423001.
[219] V. Potin, P. Ruterana, and G. Nouet, "HREM study of stacking faults in GaN layers grown over sapphire substrate," p. 7.
[220] "Structural defects in GaN revealed by transmission electron microscopy - IOPscience." https://iopscience.iop.org/article/10.7567/JJAP.53.100205 (accessed Dec. 14, 2020).
[221] A. F. Wright, "Basal-plane stacking faults and polymorphism in AlN, GaN, and InN," *J. Appl. Phys.*, vol. 82, no. 10, pp. 5259–5261, Nov. 1997, doi: 10.1063/1.366393.
[222] G. Miceli and A. Pasquarello, "Energetics of native point defects in GaN: A density-functional study," *Microelectron. Eng.*, vol. 147, pp. 51–54, Nov. 2015, doi: 10.1016/j.mee.2015.04.015.
[223] I. C. Diallo and D. O. Demchenko, "Native Point Defects in GaN: A Hybrid-Functional Study," *Phys. Rev. Appl.*, vol. 6, no. 6, p. 064002, Dec. 2016, doi: 10.1103/PhysRevApplied.6.064002.

[224] J. L. Lyons and C. G. Van de Walle, “Computationally predicted energies and properties of defects in GaN,” *Npj Comput. Mater.*, vol. 3, no. 1, Art. no. 1, Mar. 2017, doi: 10.1038/s41524-017-0014-2.
[225] J. L. Lyons, A. Janotti, and C. G. Van de Walle, “Effects of carbon on the electrical and optical properties of InN, GaN, and AlN,” *Phys. Rev. B*, vol. 89, no. 3, p. 035204, Jan. 2014, doi: 10.1103/PhysRevB.89.035204.
[226] J. L. Lyons, A. Janotti, and C. G. Van de Walle, “Carbon impurities and the yellow luminescence in GaN,” *Appl. Phys. Lett.*, vol. 97, no. 15, p. 152108, Oct. 2010, doi: 10.1063/1.3492841.
[227] D. M. Hofmann, D. Kovalev, G. Steude, B. K. Meyer, A. Hoffmann, L. Eckey, R. Heitz, T. Detchprom, H. Amano, and I. Akasaki, “Properties of the yellow luminescence in undoped GaN epitaxial layers,” *Phys. Rev. B*, vol. 52, no. 23, pp. 16702–16706, Dec. 1995, doi: 10.1103/PhysRevB.52.16702.
[228] F. A. Ponce, D. P. Bour, W. Götz, and P. J. Wright, “Spatial distribution of the luminescence in GaN thin films,” *Appl. Phys. Lett.*, vol. 68, no. 1, pp. 57–59, Jan. 1996, doi: 10.1063/1.116756.
[229] C. G. Van de Walle, C. Stampfl, and J. Neugebauer, “Theory of doping and defects in III–V nitrides,” *J. Cryst. Growth*, vol. 189–190, pp. 505–510, Jun. 1998, doi: 10.1016/S0022-0248(98)00340-6.
[230] J. C. Zolper, R. G. Wilson, S. J. Pearton, and R. A. Stall, “Ca and O ion implantation doping of GaN,” *Appl. Phys. Lett.*, vol. 68, no. 14, pp. 1945–1947, Apr. 1996, doi: 10.1063/1.115634.
[231] H. Wang, “Calculation of shallow donor levels in GaN,” p. 6.
[232] A. F. Wright, “Substitutional and interstitial oxygen in wurtzite GaN,” *J. Appl. Phys.*, vol. 98, no. 10, p. 103531, Nov. 2005, doi: 10.1063/1.2137446.
[233] “A first-principles study of carbon-related energy levels in GaN. II. Complexes formed by carbon and hydrogen, silicon or oxygen: Journal of Applied Physics: Vol 121, No 19.” https://aip.scitation.org/doi/10.1063/1.4983453 (accessed Dec. 15, 2020).
[234] K. C. Mishra, P. C. Schmidt, S. Laubach, and K. H. Johnson, “Localization of oxygen donor states in gallium nitride from first-principles calculations,” *Phys. Rev. B*, vol. 76, no. 3, p. 035127, Jul. 2007, doi: 10.1103/PhysRevB.76.035127.
[235] T. Suzuki, C. Harada, H. Goto, T. Minegishi, A. Setiawan, H. J. Ko, M.-W. Cho, and T. Yao, “Relation between interdiffusion and polarity for MBE growth of GaN epilayers on ZnO substrates,” *Curr. Appl. Phys.*, vol. 4, no. 6, pp. 643–646, Nov. 2004, doi: 10.1016/j.cap.2004.01.039.
[236] S.-K. Hong, H.-J. Ko, Y. Chen, T. Hanada, and T. Yao, “Control and characterization of ZnO/GaN heterointerfaces in plasma-assisted MBE-grown ZnO films on GaN/Al2O3,” *Appl. Surf. Sci.*, vol. 159–160, pp. 441–448, Jun. 2000, doi: 10.1016/S0169-4332(00)00053-2.
[237] S. Nakamura, “Zn-doped InGaN growth and InGaN/AlGaN double-heterostructure blue-light-emitting diodes,” *J. Cryst. Growth*, vol. 145, no. 1, pp. 911–917, Dec. 1994, doi: 10.1016/0022-0248(94)91163-0.
[238] J. L. Lyons, A. Janotti, and C. G. V. de Walle, “Impact of Group-II Acceptors on the Electrical and Optical Properties of GaN,” *Jpn. J. Appl. Phys.*, vol. 52, no. 8S, p. 08JJ04, Aug. 2013, doi: 10.7567/JJAP.52.08JJ04.

[239] “Handbook of Charged Particle Optics,” *Routledge & CRC Press*. https://www.routledge.com/Handbook-of-Charged-Particle-Optics/Orloff/p/book/9781420045543 (accessed Mar. 09, 2021).
[240] “Scanning Probe Microscopy - Atomic Force Microscopy and Scanning Tunneling Microscopy | Bert Voigtlaender | Springer.” https://www.springer.com/gp/book/9783662452394 (accessed Dec. 21, 2020).
[241] L. L. Smith, S. W. King, R. J. Nemanich, and R. F. Davis, “Cleaning of GaN surfaces,” *J. Electron. Mater.*, vol. 25, no. 5, pp. 805–810, May 1996, doi: 10.1007/BF02666640.
[242] M. L. Lee, J. K. Sheu, and S. W. Lin, “Schottky barrier heights of metal contacts to n-type gallium nitride with low-temperature-grown cap layer,” *Appl. Phys. Lett.*, vol. 88, no. 3, p. 032103, Jan. 2006, doi: 10.1063/1.2166477.