# Reduction of Switching Losses and Passive Components Rating in Series-Connected Current Source Inverters

by

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# AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

# Abstract

The current source inverter (CSI) is widely used in medium voltage drives due to its simple configuration, reliable short-circuit protection, and low *dv/dt* issue. Conventional series-connected current source inverters (SC-CSI) are constituted of several current source inverters (CSIs) connected in series through multi-winding transformers to enhance the power capacity. It is very promising in high-voltage applications. Switching losses of the semiconductor switches significantly impact the power efficiency of SC-CSIs. Therefore, inverter design must consider these losses, which depend on factors, such as switching frequency, modulation schemes and semiconductor parameters.

This thesis aims to reduce the switching losses of conventional SC-CSIs by decreasing the switching frequency from 540 Hz to 360 Hz and eventually to 60 Hz. In Chapter 2, the switching frequency is reduced to 360 Hz for the switching loss reduction. The active damping control is implemented to mitigate the increase in filter capacitance caused by the lower switching frequency. Chapter 3 is to further reduce the switching losses by reducing the switching frequency to 60 Hz. However, this strategy results in a significant increase in the passive components. To address this issue, the multi-winding transformer is replaced with a phase-shifting transformer, as the active damping method applied in Chapter 2 is no longer effective at this reduced frequency. The switching losses and the passive components of SC-CSIs are investigated with switching frequencies of 540Hz, 360Hz and 60 Hz. Simulations are conducted using MATLAB/SIMULINK to verify the investigation.

# ACKNOWLEDGMENTS

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Finally, but most importantly, I wish to thank my parents. Their unwavering faith in me, continual financial support, and emotional sustenance have been my pillars of strength throughout my educational journey.

# Publications

[1] X. Xia, Z. Wang and Q. Wei, "Passive Components Investigation for Series-Connected Current Source Inverters," *2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Shanghai, China, 2023.

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# List of Symbols

| | |
|---|---|
| DC | direct current |
| AC | alternating current |
| CSI | current source inverter |
| SC-CSI | series-connected current source inverter |
| VSI | voltage source inverter |
| PWM | pulse width modulation |
| GCT | gate commutated thyristor |
| IGBT | insulated-gate bipolar transistor |
| GTO | gate turn-off thyristor |
| SVM | space vector modulation |
| SQ1 | sequence 1 of space vector modulation |
| PF | power factor |
| PLL | phase-locked loop |
| HPF | high-pass filter |
| THD | total harmonic distortion |
| 360-Hz SC-CSI | series-connected current source inverter with a switching frequency of 360 Hz |
| 60-Hz SC-CSI | series-connected current source inverter with a switching frequency of 60 Hz |
| $L_{dc}$ | DC inductor |
| $R_1$, $R_2 \ldots R_n$, $R_g$ | grid-side resistor |

| | |
|---|---|
| $C_f$ | output capacitor |
| $L_1$, $L_2 \ldots L_n$, $L_g$ | grid-side inductor |
| $i_{w1}$, $i_{w2} \ldots i_{wn}$ | inverter output current |
| $V_{in}$ | input voltage |
| $v_g$ | grid voltage |
| $v_1$, $v_2 \ldots v_n$ | input voltage of current source inverter |
| $v_{dc}$ | input voltage of series-connected current source inverter |
| $I_{dc}$ | input current of current source inverter |
| $S_1$, $S_2 \ldots S_6$ | switches in current source inverter |
| $I_{ref}$ | reference current vector in space vector modulation |
| $m_a$ | modulation index |
| $f_{sw}$ | switching frequency |
| $f_s$ | sampling frequency |
| $P_{sw\_IGBT}$ | switching loss of IGBTs |
| $P_{swD}$ | switching loss of diodes |
| $E_{rr}$ | reverse recovery energy loss |
| $R_p$ | damping resistor |
| $i_{w\_ref}$ | reference inverter output current |
| $f_c$ | cut-off frequency of high-pass filter |
| n | number of current source inverters |
| $m$ | harmonic order |

# Chapter 1

# Introduction

Current source inverter (CSI) and voltage source inverter (VSI) are the two topologies that are widely used in medium voltage drives and power conversion applications. In contrast to VSI, CSI generates the defined three-phase pulse width modulated (PWM) AC current from a DC current supply. The CSI offers several advantages over the VSI, including a simple configuration, reliable short-circuit protection, and a low *dv/dt* issue [1][3]. Consequently, CSI is a promising candidate for energy storage systems [4], [5], renewable energies [6]-[8] and energy transmission systems [9]. Some other topologies have been developed based on the conventional CSI. For instance, the current source H7 inverter (CH7 CSI) proposed in [10] aims to avoid open circuit problems, while the CH7 CSI introduced in [11] focuses on reducing leakage current. Furthermore, the four-leg CSIs introduced in [12] were designed for common mode voltage suppression. Additionally, the connection of several CSIs in series or parallel can lead to the creation of series-connected current source inverters (SC-CSIs) and parallel-connected current source inverters, respectively. These configurations can efficiently enhance the power capacity of the system [13]-[16]. Compared to the parallel connection approach, the SC-CSI is promising for high-voltage applications [17], [18].

In this chapter, the topology and modulation scheme of the conventional CSI and conventional SC-CSI are reviewed, and the switching loss characteristics are introduced in CSIs and SC-CSIs.

## 1.1 The Current Source Inverter

The conventional grid-connected CSI topology is shown in Figure 1-1. The switches with a reverse voltage blocking capability can be used in the inverter, such as gate commutated thyristors (GCTs), symmetric gate turn-off thyristor (GTO), insulated-gate bipolar transistor (IGBT) with series diode and

metal-oxide-semiconductor field-effect transistor (MOSFET) with series diode. The inverter generates the defined output current $i_w$ from the input DC supply. The DC inductor $L_{dc}$ at the input of the inverter is to make the input current smooth and continuous [1]. The output capacitor $C_f$ has two functions: assist the commutation of the switches, and the other acts as a filter capacitor to improve the harmonic performance of the output current. $V_g$ refers to the grid phase voltage, $R_g$ is the line-side resistance ranging from.0.005pu to 0.015pu [1]. $L_g$ is the line-side inductance ranging from 0.1up to 0.15p [1], which works with $C_f$ to form the LC filter to improve the harmonic performance of the line current.

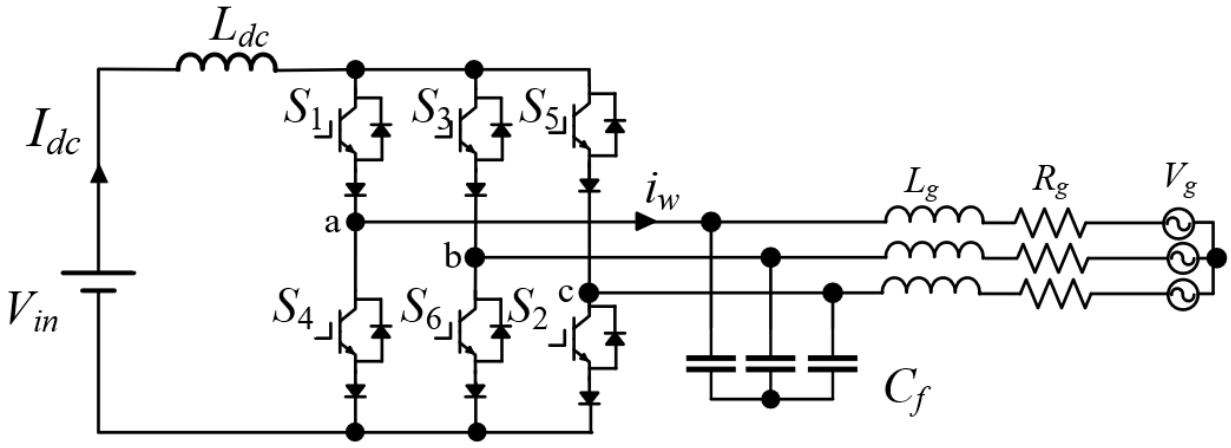


Figure-1-1 The conventional grid-tied CSI using IGBTs with series diodes.

There are several advantages of CSI compared to VSI. Unlike VSI which requires freewheeling diodes for reverse conduction capabilities, the absence of these diodes in CSI contributes to a simplified converter topology. The CSI produces the defined PWM current instead of PWM voltage in VSI, leading to no *dv/dt* issue. The large DC inductor $L_{dc}$ at the input of the inverter limits the rate of the DC current rating, which provides sufficient time for the protection circuit to function in case a short circuit occurs.

## 1.2 The Conventional Series- Connected CSI

The conventional SC-CSI is composed of several CSIs connected in series at the input and in parallel at the output through multi-winding transformers. The configuration of a grid-tied conventional n-SC-CSI is shown in Figure 1-2. In this topology, the power and voltage rating of the system is multiplied by the number of the CSI modules n. It is important to note that all the employed CSIs in this configuration are identical in terms of their topology, modulation, and control. The multi-winding transformer is an essential component to provide a separate current path for each inverter output current and ensure voltage matching, if needed, before and after the transformer [19]. Here, $L_n$ refers to the combination of linkage inductance of the multi-winding transformer, grid-side inductance, and any additional inductance.

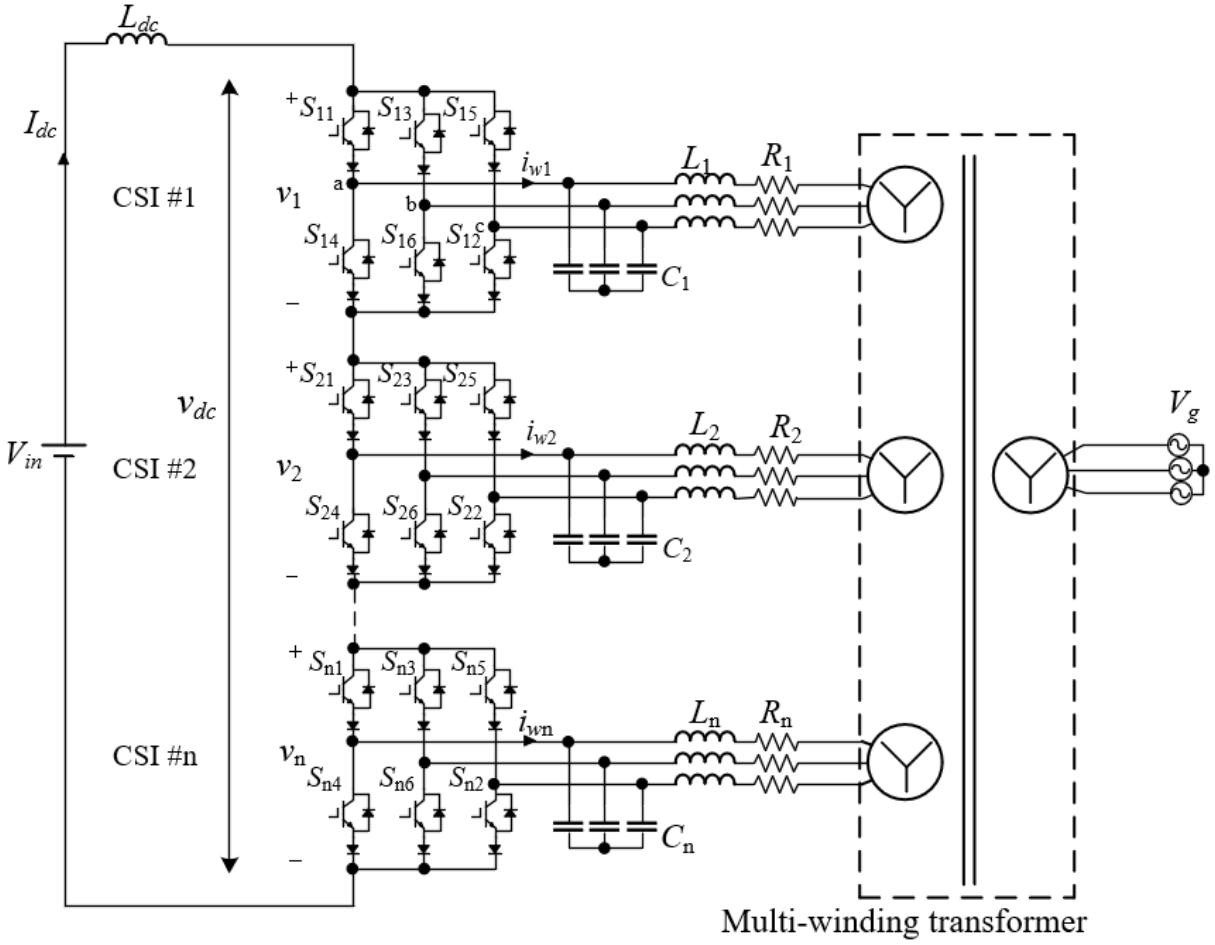


Figure 1-2 The conventional grid-tied n-SC-CSI.

## 1.3 Voltage Stress of Switches

The voltage stress is significant to be considered for the semiconductor switches selection and power losses of the system. The equivalent circuit of the n-SC-CSI is shown in Figure 1-3 for the switch voltage stress analysis. In each switching state, one upper switch and one lower switch are activated in each CSI. During the operation when switch 1 ($S_1$) and switch 6 ($S_6$) are on, the inverter output current of each CSI flows through to phase a and phase b of the grid. As a result, the input voltage of each CSI aligns with the line-to-line grid voltage $V_{ab}$. Therefore, the voltage stress experienced by each switch in SC-CSIs is the same, equal to $V_{ab}$. It is important to note that the power rating of the selected switches must have the capability to withstand this voltage stress. For example, when designing the inverter for a 4160V/1MVA grid connection system, the switches such as the 6500V IGBT with a 6500V Diode series connected can be selected as they can handle the required 4160V voltage stress.

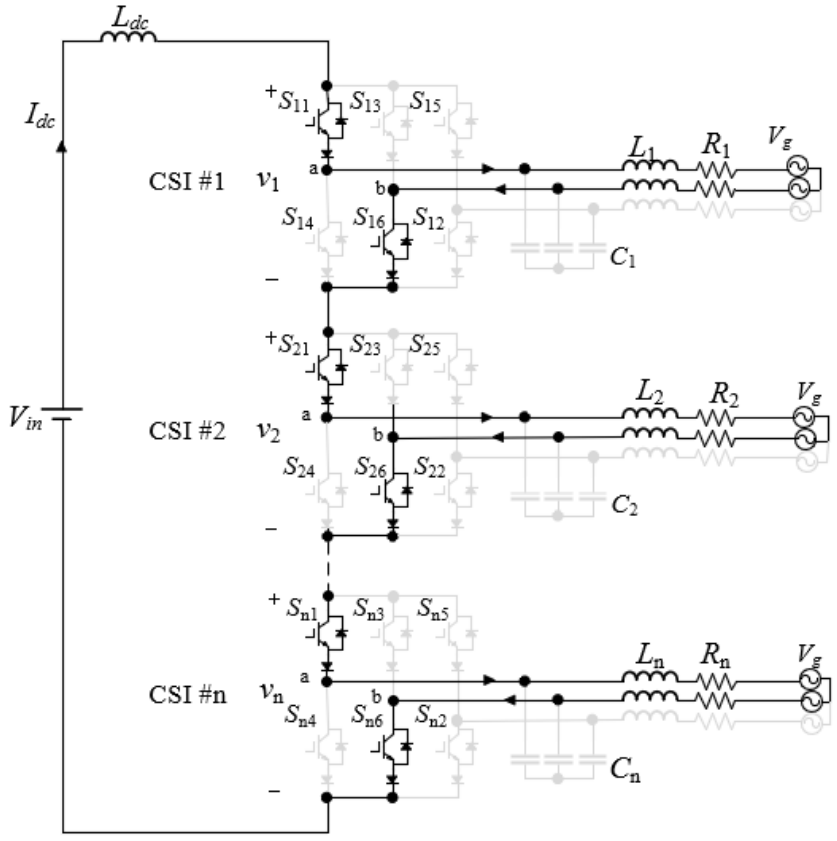


Figure 1-3 Equivalent circuit of a n-SC-CSI when $S_1$ and $S_6$ on.

## 1.4 Space Vector Modulation

Space vector modulation (SVM) is a widely used PWM technique in CSIs by manipulating the amplitude and phase of the current reference vectors. SVM features the fast dynamic response, enables the smooth and efficient operation of CSI, contributing to their application in medium voltage drives [20]-[22] and energy conversion systems [4], [11].

TABLE 1-1 Switching states and space vectors of SVM [1].

| Type | Switching state | On-state switch | Space Vector |
|---|---|---|---|
| Zero states | [1 4] | $S_{11}$,$S_{14}$ | $\overrightarrow{I_0}$ |
| | [3 6] | $S_{13}$,$S_{16}$ | |
| | [5 2] | $S_{15}$,$S_{12}$ | |
| Active states | [6 1] | $S_{16}$,$S_{11}$ | $\overrightarrow{I_1}$ |
| | [1 2] | $S_{11}$,$S_{12}$ | $\overrightarrow{I_2}$ |
| | [2 3] | $S_{12}$,$S_{13}$ | $\overrightarrow{I_3}$ |
| | [3 4] | $S_{13}$,$S_{14}$ | $\overrightarrow{I_4}$ |
| | [4 5] | $S_{14}$,$S_{15}$ | $\overrightarrow{I_5}$ |
| | [5 6] | $S_{15}$,$S_{16}$ | $\overrightarrow{I_6}$ |

The PWM switching pattern used in CSI must adhere to the specific constraint: At any instant, only two switches are conducting, one in the top half of the bridge and the other in the bottom half [1]. According to this constraint, SVM defines nine switching states, with three zero states and six active switching states, as listed in TABLE 1-1. The nine switching states can be represented using six active vectors and three zero vectors in one fundamental cycle. The typical space vector diagram for CSI is shown in Figure 1-4, where $\overrightarrow{I_1}$ to $\overrightarrow{I_6}$ are the space vectors and $\overrightarrow{I_{ref}}$ is the reference current rotating with the speed $\omega$.

$$\omega = 2\pi f_1 \tag{1-1}$$

where $f_1$ is fundamental frequency of the inverter. The length of $\overrightarrow{I_{ref}}$ represents the magnitude of the output current, which can be determined by the magnitude modulation index ($m_a$), given as

$$m_a = \frac{I_{ref}}{I_{dc}} = \frac{\hat{I}_w}{I_{dc}} \tag{1-2}$$

where $\hat{I}_w$ refers to the peak value of the fundamental frequency of inverter output current, $I_{dc}$ is the DC input current. The reference current vector can be defined by two nearby active vectors and one zero vector in each sector of the hexagon. The dwell time represents the duty cycle time of the switch within the sampling period and can be calculated by [1]:

$$\begin{cases} T_1 = \sin(-\frac{\pi}{6} - \theta + \frac{\pi}{3}k) m_a T_s \\ T_2 = \sin(\frac{\pi}{2} + \theta - \frac{\pi}{3}k) m_a T_s \end{cases} \tag{1-3}$$

where $T_s$ is the sampling period, $T_1$ and $T_2$ are the dwell times for vectors $\overrightarrow{I_k}$, and $\overrightarrow{I_{k+1}}$, $\theta$ is the angle between the reference current and α-axis, and k is the sector number. The dwell time of zero vector $T_0$ depends on the selection of the switching sequences. For instance, $T_0$ for SQ1 ($\overrightarrow{I_k}$ , $\overrightarrow{I_{k+1}}$, $\overrightarrow{I_0}$) can be calculated as

$$T_0 = T_s - T_1 - T_2 \tag{1-4}$$

The calculated $T_1$ and $T_1$+$T_2$ are then compared to the sawtooth waveform with the sampling frequency ($f_s$=1/$T_s$) for vector selection. The two requirements must be satisfied for SVM switching sequence design with minimum switching frequencies: 1) Transitions between switching states should involve only two switches, with one switching on and the other switching off. 2) Shifting $\overrightarrow{I_{ref}}$ from one sector to the next should involve the minimum number of switching.

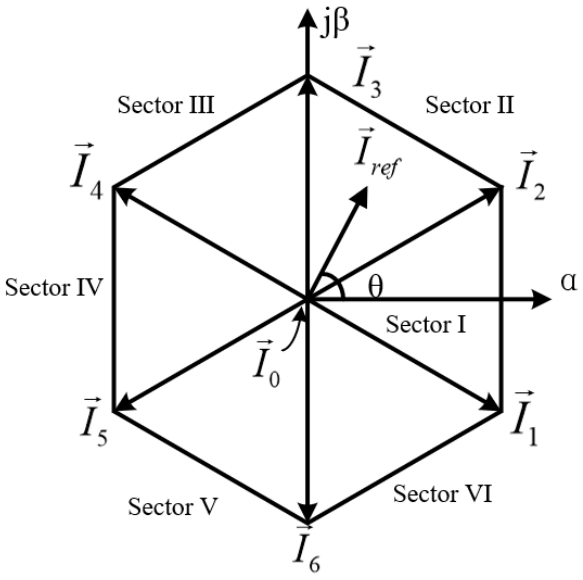


Figure 1-4 Space vector diagram.

SVM with a switching frequency around 500 Hz is commonly employed in a high-power inverter to ensure that the inverter output current is close to the sinusoidal waveform [3]. In this thesis, the term "conventional CSIs" and "conventional SC-CSIs" refer to inverters that employ SVM with a switching frequency of 540 Hz. Figure 1-5 provides the overview of the switching patterns and output inverter current of a conventional CSI with 540 Hz SVM (SQ1). Each switch is activated when its corresponding gating signal ($v_{g1}$-$v_{g6}$) is in a high state. The inverter fundamental frequency is set at 60 Hz. There are nine pules within each half cycle of the inverter output current $i_w$, with respect to the 540 Hz switching frequency. The harmonic spectrum of the $i_w$ is illustrated in Figure 1-6. It reveals that the dominant harmonic current pairs are the 17th and 19th orders, as well as the 23rd and 25th orders. These harmonics play a significant role in shaping the waveform of the inverter output current and need to be addressed for achieving harmonic limits from the grid code.

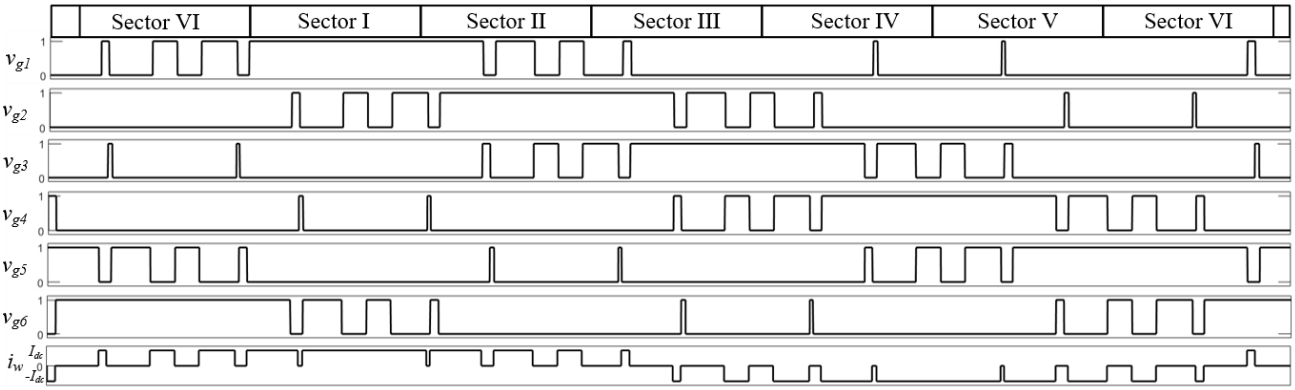


Figure 1-5 Switching sequence of SQ1 SVM, $f_{sw}$=540 Hz, $m_a$=1.0.

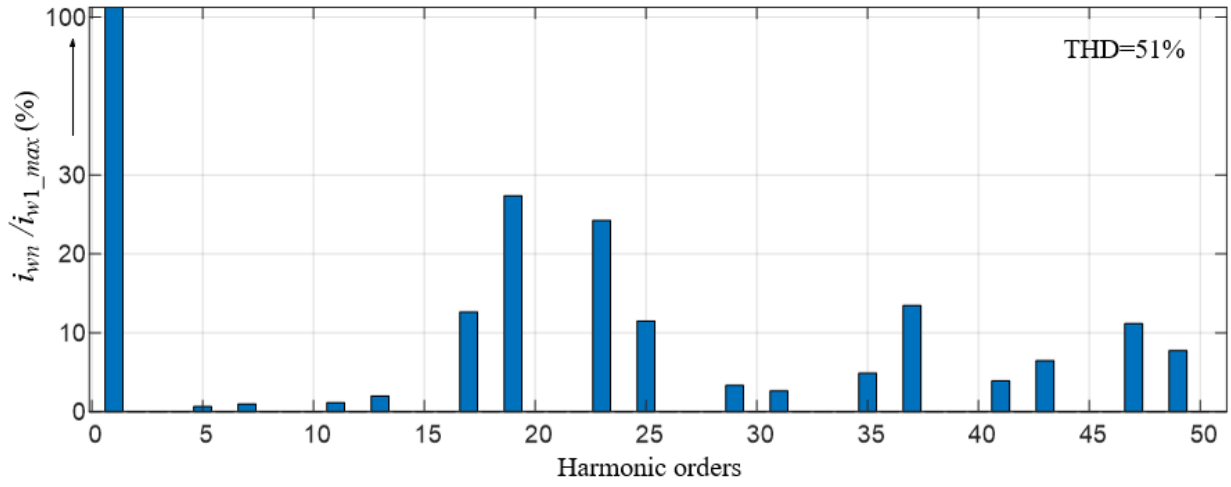


Figure 1-6 Harmonic spectrum of the inverter output current $i_w$.

## 1.5 Grid Connection Control

The grid connection control, as known as power factor (PF) control, refers to the control strategy used in the grid-tied converters to regulate the active and reactive power to the grid. In grid-tied converter systems, it is crucial to match the power factor desired from the grid-side for efficient power transfer.

Since the conventional SC-CSI employs the identical CSIs connected in series, the same active and reactive power is experienced by each CSI module. Therefore, the control scheme reviewed in this section

focuses on the conventional single CSI with a unity power factor (PF=1.0). The principle of PF control is to regulate the active and reactive power of the grid-tied converter by adjusting their modulation index and delay angle.

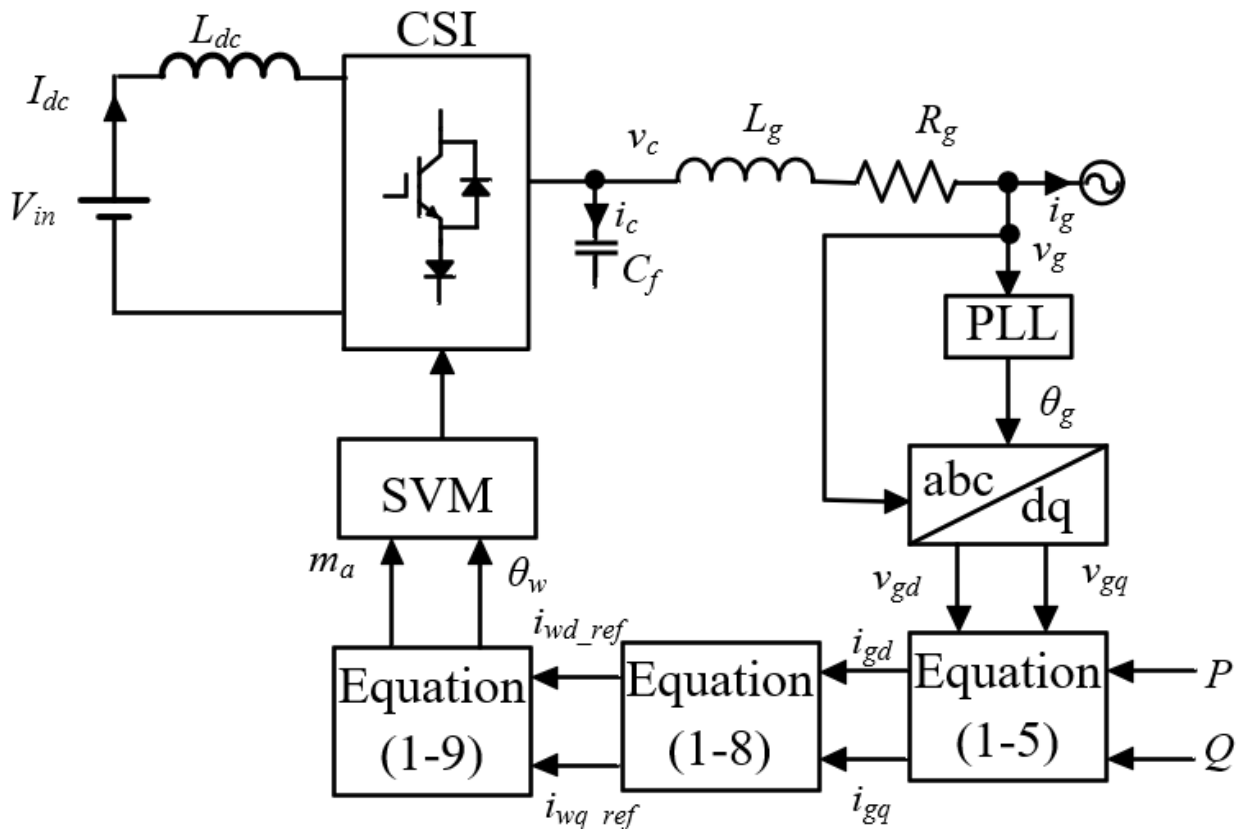


Figure 1-7 Block diagram of PF control.

Figure 1-7 shows a block diagram of the PF control algorithm. The digital phase-locked loop (PLL) block detects the grid reference angle ($\theta_g$.) By applying the voltage orientation within the synchronous reference frame, the grid voltage is aligned to the d-axis. The active and reactive power in dq-axis can be defined as [23]

$$P = \frac{3}{2} v_{gd} i_{gd}$$
$$Q = -\frac{3}{2} v_{gd} i_{gq} \tag{1-5}$$

where $v_{gd}$, $v_{gq}$, $i_{gd}$ and $i_{gq}$ are the grid voltage and current in dq-axis respectively. The capacitor current under steady state can be calculated as

$$\begin{cases} i_{cd} = -\omega C_f v_{cq} \\ i_{cq} = \omega C_f v_{cd} \end{cases} \tag{1-6}$$

where $C_f$ is the predesigned filter capacitor to comply with the grid code, $v_{cd}$ and $v_{cq}$ are the steady state capacitor voltage, which can be calculated as

$$\begin{aligned} v_{cd} &= (R_g - \omega L_g) i_{qs} + v_{dg} \\ v_{cq} &= \omega L_g i_{dg} + R_g i_{qg} \end{aligned} \tag{1-7}$$

The reference inverter output current ($i_{w\_ref}$) can be determined by combining Equation (1-6) and Equation (1-7).

$$\begin{aligned} i_{wd\_ref} &= (1 - \omega^2 L_g C_f) i_{gd} - \omega R_g C_f i_{gq} \\ i_{wq\_ref} &= \omega C_f v_{gd} + \omega R_g C_f i_{gd} + (1 - \omega^2 L_g C_f) i_{gq} \end{aligned} \tag{1-8}$$

The reference modulation index can be obtained by normalizing the $i_{w\_ref}$ with $I_{dc}$. The delay angle ($\theta_w$) is defined as the phase displacement between grid voltage and reference inverter output current.

$$\begin{aligned} m_a &= \frac{\sqrt{i_{wd}^{\ 2} + i_{wq}^{\ 2}}}{I_{dc}} \\ \theta_w &= \tan^{-1}\left(\frac{i_{wq}}{i_{wd}}\right) \end{aligned} \tag{1-9}$$

The reference modulation index and delay angle are implemented into SVM to generate the reference inverter output current. The phasor diagram of the control algorithm is shown in Figure 1-8.

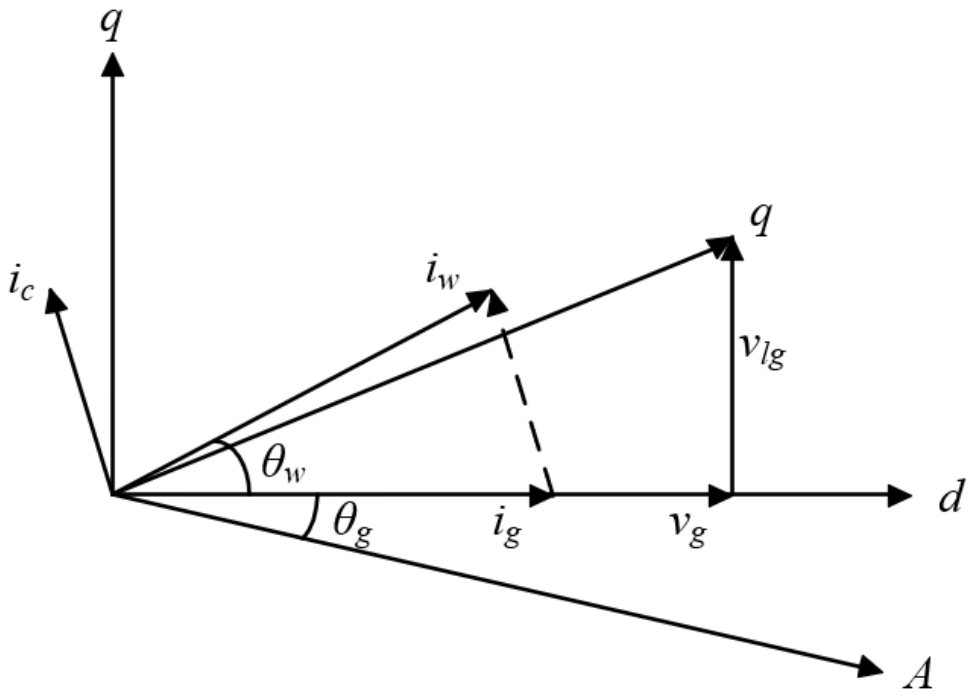


Figure 1-8 Phasor diagram of the PF control.

## 1.6 Passive Components Design

The DC inductor and the output filter capacitor are two critical passive components used in SC-CSIs. These components play a significant role in the operation performance, costs, and losses of the SC-CSIs. This section reviews the filter capacitor and DC inductor design in conventional grid-tied SC-CSIs.

### 1.6.1 DC Inductor

The DC inductor at the input of the SC-CSIs makes the DC current smooth and continuous [1]. However, it is typically bulky and costly [24]. The equivalent circuit of an n-SC-CSI is shown in Figure 1-9 for a better analysis of the DC inductor design.

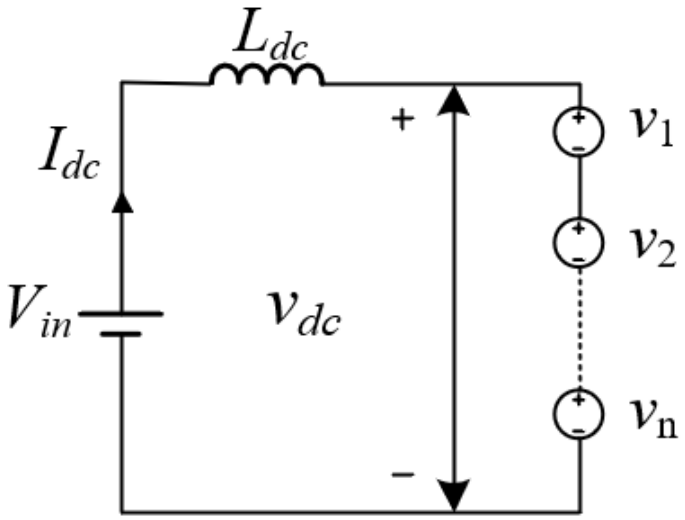


Figure 1-9 Equivalent circuit of a n-SC-CSI [24].

According to the voltage-second principle, the DC inductor $L_{dc}$ can be calculated by

$$L_{dc} = \frac{\left| V_{in} - \frac{1}{\Delta t}\int_{t}^{t+\Delta t} v_{dc}\,dt \right| \Delta t}{\Delta I_{dc}} \tag{1-10}$$

where $\Delta I_{dc}$ is DC current ripple, $\Delta t$ is dwell time, $v_{dc}$ is the sum of input voltage of each CSI module. Since all the employed CSI modules are identical, $v_{dc}$ can be defined as

$$v_{dc} = v_1 + v_2 + ...v_n = nv_1 \tag{1-11}$$

where n refers to the number of CSI modules. $v_1$-$v_n$ refers to the input voltage of each CSI module, which can be obtained by the line-to-line grid voltage $v_g$ and phase angle $\theta$ [13].

$$\begin{cases} v_a = v_g \cos\theta \\ v_b = v_g \cos(\theta - \frac{2\pi}{3}) \\ v_c = v_g \cos(\theta + \frac{2\pi}{3}) \end{cases} \tag{1-12}$$

$$\begin{cases} [S_6, S_1]: v_n = v_{ab} = \sqrt{3} V_g \cos(\theta + \frac{\pi}{6}) \\ [S_1, S_2]: v_n = v_{ac} = \sqrt{3} V_g \cos(\theta - \frac{\pi}{6}) \\ [S_2, S_3]: v_n = v_{bc} = \sqrt{3} V_g \cos(\theta - \frac{\pi}{2}) \\ [S_3, S_4]: v_n = v_{ab} = \sqrt{3} V_g \cos(\theta - \frac{5\pi}{6}) \\ [S_4, S_5]: v_n = v_{ca} = \sqrt{3} V_g \cos(\theta + \frac{5\pi}{6}) \\ [S_5, S_6]: v_n = v_{cb} = \sqrt{3} V_g \cos(\theta + \frac{\pi}{2}) \end{cases} \tag{1-13}$$

The calculation of DC inductance can be performed for each switching state by substituting Equation (1-11) and Equation (1-12) into Equation (1-10). Since the value of $v_{dc}$ and $\Delta t$ is repeated for each sector in SVM, $L_{dc}$ can be determined in any selected sector. Using the conventional two-CSI system as an example, the waveform of $v_{in}$ and $v_{dc}$ in sector I is shown in Figure 1-10. Equation (1-14) represents the nine inductance value calculations obtained in sector I, considering a switching frequency of 540 Hz. From these calculations, the largest inductance value is selected to make sure the DC current ripple is equal to or below the required level [24].

$$\begin{cases} [S1,\ S6]: L_{dc1} = \dfrac{\left| \left\{ V_{in} - \dfrac{1}{T_1} \displaystyle\int_0^{T_1} 2\cos(\theta + \frac{\pi}{6}) \right\} d\theta \right| T_1}{\triangle I_{dc}} \\ [S1,\ S2]: L_{dc2} = \dfrac{\left| \left\{ V_{in} - \dfrac{1}{T_2} \displaystyle\int_{T_1}^{T_1+T_2} 2\cos(\theta - \frac{\pi}{6}) \right\} d\theta \right| T_2}{\triangle I_{dc}} \\ [S1,\ S4]: L_{dc3} = \dfrac{\left| \{ V_{in} - 0 \} d\theta \right| T_0}{\triangle I_{dc}} \\ \vdots \\ [S1,\ S4]: L_{dc9} = \dfrac{\left| \{ V_{in} - 0 \} d\theta \right| T_0}{\triangle I_{dc}} \\ L_{dc} = \max \{ L_{dc1}, L_{dc2}, L_{dc3} ..... L_{dc9} \} \end{cases} \tag{1-14}$$

Since the employed CSI modules are identical in conventional SC-CSIs, the input voltage ($V_{in}$) and total CSI input voltage ($v_{dc}$) are multiplied by the number of applied CSI modules (n). Therefore, with the constant current ripple ($\Delta I_{dc}$), the DC inductance required in the n-CSI system is n times that of the single CSI system.

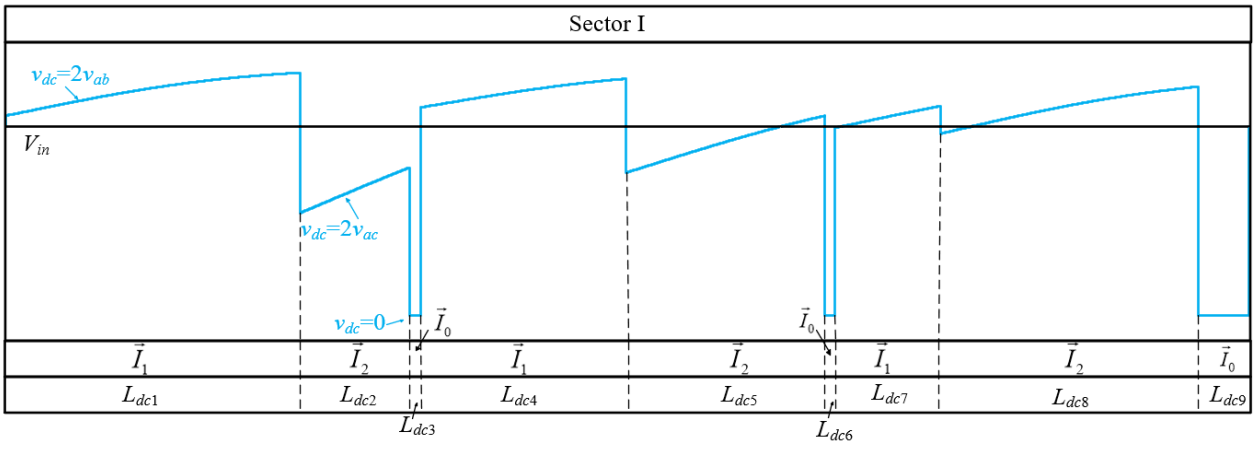


Figure 1-10 Waveforms of $V_{in}$ and $v_{dc}$ in Sector I for a conventional two-CSI system using SQ1 SVM, $f_{sw}$=540 Hz.

## 1.6.2 Filter Capacitor

Figure 1-11 shows the simplified single phase output LC filter of a single CSI module. The filter capacitor ($C_f$) at the output of CSI works in conjunction with the inductance ($L_g$) forms the CL harmonic filter. Note that $L_g$ includes the grid-side inductance and leakage inductance of transformers, typically ranging from 0.1pu to 0.15 pu. This CL circuit exhibits light damping due to the presence of a small grid-side resistance ($R_g$) ranging from 0.005pu to 0.01 pu. The transfer function of the filter can be derived as

$$\frac{I_g(j\omega)}{I_w(j\omega)} = \frac{1}{(j\omega)^2 L_g C_f + j\omega R_g C_f + 1} \tag{1-15}$$

The value of the output capacitance is designed to comply with the strict grid code such as IEEE 519-2014 [25]. These grid codes specify the permissible harmonic levels that must be adhered to by the

system. The harmonic requirement set by IEEE 519-2014 is listed in TABLE 1-2. THD in the table refers to the total harmonic distortion, provides an assessment of the overall distortion level present in the waveform, and can be defined as

$$\mathrm{THD} = \frac{\sqrt{I_2^{\,2} + I_3^{\,2} + I_4^{\,2} + I_5^{\,2} + \cdots}}{I_1} \times 100\% \tag{1-16}$$

where $I_1$ is the fundamental frequency current, $I_2$, $I_3$, $I_4$ etc., are the harmonic currents. To satisfy the minimum requirement for each harmonic and ensure with the grid code, the filter capacitance for each harmonic needs to be calculated using Equation (1-14). Among all the calculated capacitance values, the largest one must be selected to meet the grid code.

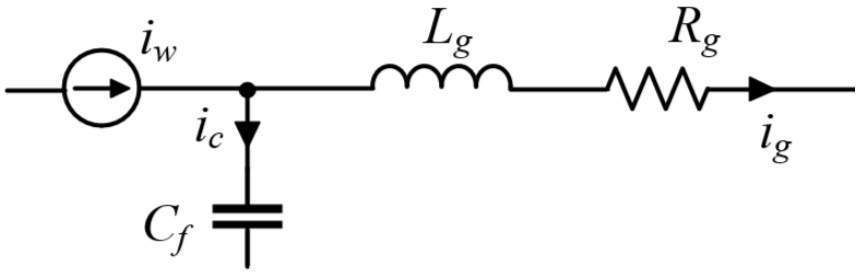


Figure 1-11 The output LC filter of a single CSI.

TABLE 1-2 Grid current harmonic requirement from IEE 519-2014 [25].

| **Harmonic Order** | 3≤h<11 | 11≤h<17 | 17≤h<23 | 23≤h<35 | 35≤h<50 | THD |
|---|---|---|---|---|---|---|
| $\boldsymbol{I_h/I_1}$ **(%)** | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

## 1.7 Switching Losses of SC-CSIs

The switching losses occur during the transition periods when the power switches turn on or off, resulting in energy dissipation and increasing the system power losses [26],[27]. The switching losses of IGBTs and series diodes are considered in SC-CSIs. The switching losses for each switch employed in conventional SC-CSIs are the same as all the CSI modules are identical in switch selection, modulation scheme and switching frequency. The switching losses of a single IGBT can be calculated as [19],[28]

$$P_{sw\_IGBT} = f_{sw}(E_{on} + E_{off})(\frac{i}{I_{nom}})(\frac{v}{V_{nom}}) \tag{1-17}$$

where $f_{sw}$ is the switching frequency of the device, $I_{nom}$ and $V_{nom}$ are the rated current and voltage, $v$ and $i$ are instantaneous voltage and current, respectively. $E_{on}$ and $E_{off}$ are the turn-on and turn-off energy which can be found in the spice datasheet.

Switching losses of diodes primarily occur during the turn-off period due to the reverse recovery current [27]. Diode reverse recovery is caused by the stored charge in the p-n junction that must be removed during the turn-off period, resulting in energy dissipation. The turn-off losses of a single diode can be calculated by [28],[29]

$$\begin{aligned} P_{swD} &= f_{sw}E_{rr} \\ E_{rr} &= \frac{1}{4}Q_{rr}V_b\left(\frac{I_F}{I_{Fnom}}\right) \end{aligned} \tag{1-18}$$

where $E_{rr}$ is the reverse recovery energy loss, $Q_{rr}$ is reverse recovery charges, $V_b$ is the reverse blocking voltage, $I_F$ is the forward current, $I_{Fnom}$ is the rated forward current. The total switching losses of one switch time can be defined as the sum of the switching loss of an IGBT and a series diode, which can be obtained by

$$P_{sw} = 6\mathrm{n} \times (P_{sw\_IGBT} + P_{swD}) \tag{1-19}$$

Where n is the number of CSI modules employed in SC-CSIs.

Existing methods to decrease switching losses and improve the power efficiency of CSIs involve replacing reverse-voltage-blocking (RB) switches with alternative switching devices, including wide-bandgap (WBG) semiconductor devices [30] and bidirectional (BD) switches [31],[32]. However, based on the literature evidence, replacing the switches does not result in significant reductions in switching losses compared to conventional CSIs with RB switches; these approaches focus more on reducing conduction losses. Alternatively, a straightforward approach to reducing switching losses is directly lowering the switching frequency. However, the reduction of the switching frequency will lead to poor harmonic performance in the inverter output current, thereby increasing the requirement of the passive components, such as filter capacitor and DC inductor.

## 1.8 Challenges and Research Objectives

Switching losses of the semiconductor switches significantly impact the power efficiency and overall performance of SC-CSIs. To achieve higher efficiency and reduce power losses, this thesis focuses on the reduction of switching losses in SC-CSIs by lowering the switching frequency of the inverters. However, this approach presents a challenge in the form of a trade-off, as the reduced switching frequency results in a significant increase in passive components. Therefore, the main objective of the thesis is to address this trade-off by investigating alternative methods and configurations that can mitigate the impact of increased passive components while still achieving substantial switching losses reduction. The thesis investigates the percentage reduction in switching losses and passive components for each SC-CSI configuration compared to the conventional SC-CSIs.

## 1.9 Thesis Organization

The organization of the rest of the thesis can be summarized as follows:

- Chapter 2 investigates the switching losses and filter capacitance of SC-CSIs with switching frequencies of 540 Hz and 360 Hz. The active damping is implemented to 360-Hz SC-CSI to mitigate the increase in filter capacitance caused by the reduced switching frequency.
- Chapter 3 introduced SC-CSIs with a switching frequency of 60 Hz to further reduce the switching losses. The phase-shifting transformer is implemented to address the significant increase of the passive components since the active damping method used in Chapter 2 does not work as expected.
- Chapter 4 summarizes the findings and contributions of the thesis. Discusses the limitations of the research and areas for future work. Provides recommendations for future studies and research to further enhance the performance and practicality of SC-CSIs.

# Chapter 2

# The Series-Connected CSI with $f_{sw}$=360 Hz with Active Damping

As mentioned before, the conventional SC-CSIs in this thesis refer to the inverters that utilize SVM with a switching frequency of 540 Hz. Reducing the switching frequency is one of the approaches to reducing switching losses. This chapter reduces the switching frequency from 540 Hz to 360 Hz for the switching loss reduction. However, the lower switching frequency results in the poorer quality of the inverter output current waveforms. In particular, when using SVM with a switching frequency of 360 Hz, the dominant harmonic orders in the inverter output current shift to the 11th and 13th orders rather than the previously dominant 17th and 19th orders. The presence of these dominant low-order harmonic currents necessitates the use of larger filter capacitors at the output of the CSIs to improve harmonic performance and meet grid code requirements.

Nevertheless, decreasing the switching frequency while significantly increasing the filter capacitor size is not an accepted trade-off. To address this issue, the active damping control technique is introduced to reduce the required filter capacitance. By implementing the active damping control in the 360-Hz SC-CSIs, the required filter capacitance is efficiently reduced compared to the 360 Hz SC-CSIs without active damping. This chapter investigates and compares the switching losses and filter capacitor size between conventional SC-CSIs and 360-Hz SC-CSIs with active damping. Simulation is conducted by MATLAB/SIMULINK to analyze the performance of active damping and its impact on filter capacitance reduction.

## 2.1 Active Damping Control

The two categories of damping methods for LC resonance are passive damping and active damping [1],[33],[40]. The passive damping method adds the physical damping resistor to the system for damping

performance. However, this method also introduces additional power losses, particularly in high-power applications. On the other hand, active damping utilizes a control algorithm to emulate a virtual resistor, thereby achieving the desired damping performance without dissipating additional power losses. This control algorithm can be implemented by adjusting the modulation index and the delay angle of SVM. Additionally, active damping has the capability to reduce the THD in the grid current by damping the harmonic currents around the resonance frequency, as presented in [41]. This helps improve power quality and ensure compliance with harmonic requirements.

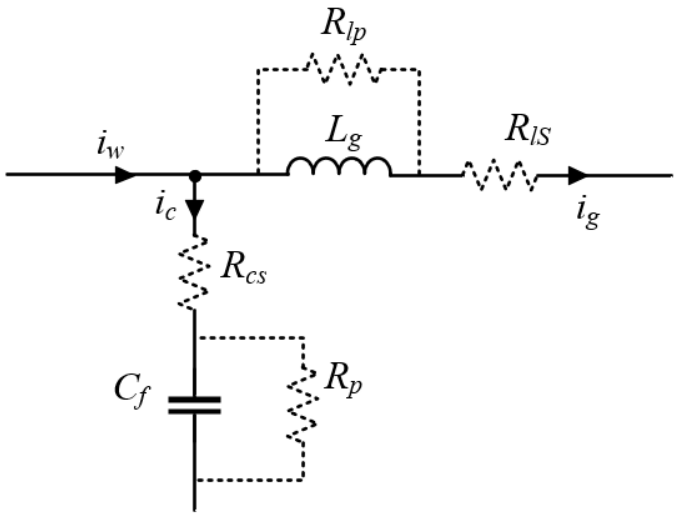


Figure 2-1 Possible locations of virtual resistors in an LC filter circuit [34].

The possible locations to implement a damping resistor in an LC filter are shown in Figure 2-1[37]. For CSIs, the most convenient location of the virtual resistor is in parallel to the output filter capacitor. This choice is advantageous because the CSI can easily generate the damping current that flows parallel to the capacitor. The equivalent circuit of the active damping approach in a single CSI is shown in Figure 2-2. Here, $i_{w\_ref}$ represents the new reference inverter output current, which contains both the original CSI output current ($i_w$) and damping current ($i_p$). The damping current can be obtained by dividing the measured capacitor voltage ($v_c$) by the virtual resistor ($R_p$).

$$i_p = v_c / R_p \tag{2-1}$$

Even though the lower virtual resistance leads to better damping performance, it is recommended to be selected above 1 per unit. This consideration ensures control loop stability and maintains reasonable gain and phase margins, as presented in [41].

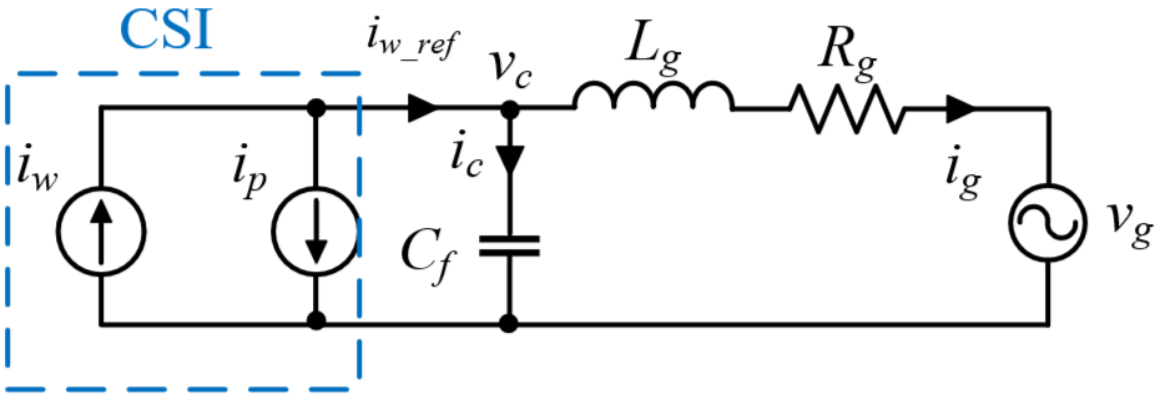


Figure 2-2 Equivalent circuit of a single CSI with active damping control.

Similar to the PF control introduced in Chapter 1, the operation principle of the active damping control is to generate the new reference inverter output current by adjusting the modulation index and the delay angle of the inverter. It is important to note that the PF control algorithm is based on the fundamental components of current and voltage. To prevent interference between the active damping control and PF control, the active damping control procedure should only focus on the harmonic components. In other words, the active damping control will only be activated if harmonic currents are present in the system.

Figure 2-3 shows the block diagram of the active damping control combined with PF control. The three-phase capacitor voltage ($v_c$) is detected and transformed into the synchronous reference frame ($v_{c\_dq}$), which contains fundamental current and significant harmonic currents absorbed from the inverter output current. In the synchronous reference frame, the fundamental component of the measured capacitor voltage is a DC quantity, which can be easily removed by a high-pass filter (HPF) with a low cut-off frequency. The transfer function of a simple first order HPF can be expressed as

$$H(s) = \frac{s}{s + 2\pi f_c} \tag{2-2}$$

where $f_c$ is the cut-off frequency of the filter. The damping current in the synchronous reference frame ($i_{p\_d,q}$) is obtained by dividing voltage ($v'_{c\_d,q}$) by virtual resistor ($R_p$). The damping current is subtracted from the PF control output current ($i'_{w\_d,q}$) to obtain the new reference inverter output current ($i_{w\_ref\_d,q}$).

$$i_{w\_ref\_d,q} = i'_{w\_d,q} - i_{p\_d,q} \tag{2-3}$$

The new reference inverter output current consists of two components: the fundamental component obtained from the PF control and the harmonic component obtained from the active damping control. Finally, the delay angle and modulation index can be determined by $i_{w\_ref\_d,q}$, and implemented into SVM to generate the switching signals.

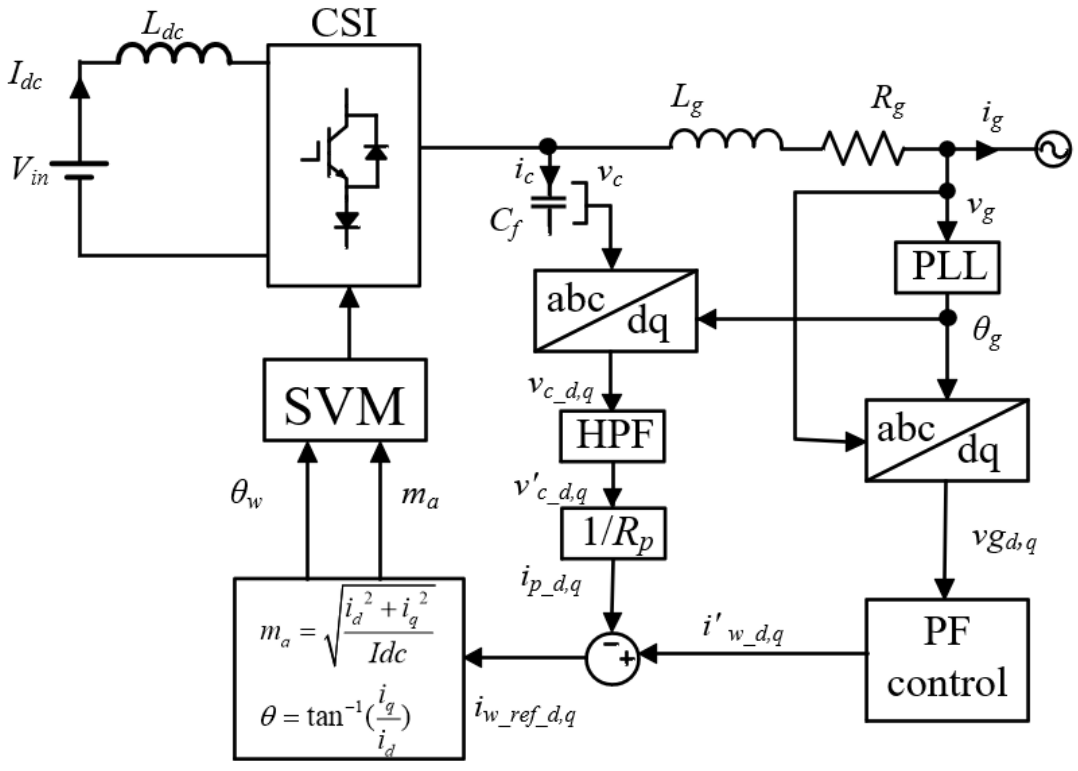


Figure 2-3 Block diagram of active damping control.

## 2.2 Switching Losses Investigation

Since active damping is applied through a control algorithm, which does not change the switching sequence of the switches in CSIs, the implementation of active damping does not alter the switching losses of IGBTs and diodes in inverters under the same switching frequency conditions. The switching losses of the two-CSI, three-CSI, and five-CSI systems with switching frequencies of 540 Hz and 360 Hz are calculated. To ensure that the switches can handle the voltage stress, suitable switches need to be selected. For this analysis, the switches used in each topology are chosen as a 6500 V IGBT (FZ750R65KE3) with a 6800 V diode (D711N68T) connected in series. The spice parameters for these components, obtained from the datasheets, are provided in TABLE 2-1.

TABLE 2-1 Parameters of the IGBT and diode.

| **Device Type** | IGBT | Diode |
|---|---|---|
| **Part Number** | FZ750R65KE3 | D711N68T |
| **Voltage Rating (V)** | 6500 | 6800 |
| **Current Rating (A)** | 750 | 770 |
| **Forward Voltage (V)** | 3.0 | 1.77 |
| **Turn-on Time (μs)** | 0.8 | - |
| **Turn-off Time (μs)** | 1.5 | - |
| $E_{on}$ **(J)** | 0.5 | - |
| $E_{off}$ **(J)** | 0.9 | - |
| **Recovered Charge (mAs)** | - | 5 |

The switching losses of IGBTs and didoes can be calculated by using Equation (1-17) and Equation (1-18). By applying these equations, the switching losses of the SC-CSIs with switching frequencies of 540

Hz and 360 Hz can be determined. The calculated switching losses are presented in TABLE 2-2. It can be observed that reducing the switching frequency to 360 Hz results in a significant reduction in switching losses compared to 540 Hz. In the two-CSI, three-CSI, and five-CSI systems, a percentage reduction of 33% is achieved. This reduction in switching losses contributes to improved overall system efficiency and performance.

TABLE 2-2 Calculated switching losses of SC-CSIs.

| **Topology** | **Device Switching Losses (W)** | | **Total Switching Losses (W)** | **Percentage Reduction (%)** |
|---|---|---|---|---|
| Two-CSI system $f_{sw}$= 540 Hz | IGBTs | 8768 | 22382 | 33 |
| | Diodes | 13614 | | |
| Two-CSI system $f_{sw}$= 360 Hz | IGBTs | 5845 | 14921 | |
| | Diodes | 9076 | | |
| Three-CSI system $f_{sw}$= 540 Hz | IGBTs | 13152 | 33574 | 33 |
| | Diodes | 20422 | | |
| Three-CSI system $f_{sw}$= 360 Hz | IGBTs | 8768 | 22382 | |
| | Diodes | 13614 | | |
| Five-CSI system $f_{sw}$= 540 Hz | IGBTs | 21920 | 55957 | 33 |
| | Diodes | 34037 | | |
| Five-CSI system $f_{sw}$= 360 Hz | IGBTs | 21920 | 37304 | |
| | Diodes | 34037 | | |

## 2.3 Filter Capacitance Investigation

The new reference inverter output current contains both the fundamental component obtained from the PF control and the harmonic components obtained by the capacitor harmonic current. As a result, the harmonic currents present in the new reference inverter output current differ from the conventional approach. To achieve this, the harmonic damping current, which has the same phase angle as the capacitor

voltage, is subtracted from the original harmonic current. This subtraction helps in mitigating the undesired harmonic content and improves the overall harmonic performance of the system.

The calculated filter capacitance for SC-CSIs with switching frequencies of 540 Hz and 360 Hz, to comply with the grid code, are listed in TABLE 2-3 for comparison. This calculation considers the total grid-side inductance of 0.2 pu, grid-side resistance of 0.01 pu, and virtual resistance of 1 pu. In the two-CSI, three-CSI, and five-CSI systems with a switching frequency of 360 Hz, the filter capacitance increases by 114%, 180%, and 197%, respectively, compared to the SC-CSIs with a switching frequency of 540 Hz. Furthermore, the calculated filter capacitance for SC-CSIs with a switching frequency of 360 Hz, with and without active damping, is listed in TABLE 2-4. Approximately 20% reduction is achieved by implementing active damping to SC-CSIs. However, even with this reduction, the capacitance values remain larger than those employed in conventional SC-CSIs. The capacitance experiences an increase of 68%, 120%, and 130% in 360-Hz two-CSI, three-CSI, and five-CSI systems with active damping, respectively, in comparison to conventional SC-CSIs. To visualize the comparison of the filter capacitance in SC-CSIs, a bar diagram is provided in Figure 2-4 for easy and clear comparison between different configurations.

TABLE 2-3 Calculated filter capacitance for SC-CSIs with switching frequency of 540 Hz and 360 Hz.

| **Topology** | **Power Rating** | **Filter Capacitance** | **Percentage Increase** |
|---|---|---|---|
| Two-CSI system $f_{sw}$= 540 Hz | 4160 V/2 MVA | 70 µF (0.23 pu) | 114% |
| Two-CSI system $f_{sw}$= 360 Hz | 4160 V/2 MVA | 150 µF (0.5pu) | |
| Three-CSI system $f_{sw}$= 540 Hz | 4160 V/3 MVA | 110 µF (0.24 pu) | 180% |
| Three-CSI system $f_{sw}$= 360 Hz | 4160 V/3 MVA | 310 µF (0.67 pu) | |
| Five-CSI system $f_{sw}$= 540 Hz | 4160 V/5 MVA | 235 µF (0.3pu) | 197% |
| Five-CSI system $f_{sw}$= 360 Hz | 4160 V/5 MVA | 700 µF (0.91 pu) | |

TABLE 2-4 Calculated filter capacitance for SC-CSIs with switching frequency of 360Hz with and without active damping.

| Switching Frequency=360 Hz | | | |
|---|---|---|---|
| **Topology** | **Power Rating** | **Filter Capacitance** | **Percentage Reduction** |
| Two-CSI system No damping | 4160 V/2 MVA | 150 µF (0.5pu) | 21% |
| Two-CSI system With active damping | 4160 V/2 MVA | 118 µF (0.38pu) | |
| Three-CSI system No damping | 4160 V/3 MVA | 310 µF (0.67 pu) | 20% |
| Three-CSI system With active damping | 4160 V/3 MVA | 250 µF (0.54 pu) | |
| Five-CSI system No damping | 4160 V/5 MVA | 700 µF (0.91 pu) | 22% |
| Five-CSI system With active damping | 4160 V/5 MVA | 545 µF (0.77 pu) | |

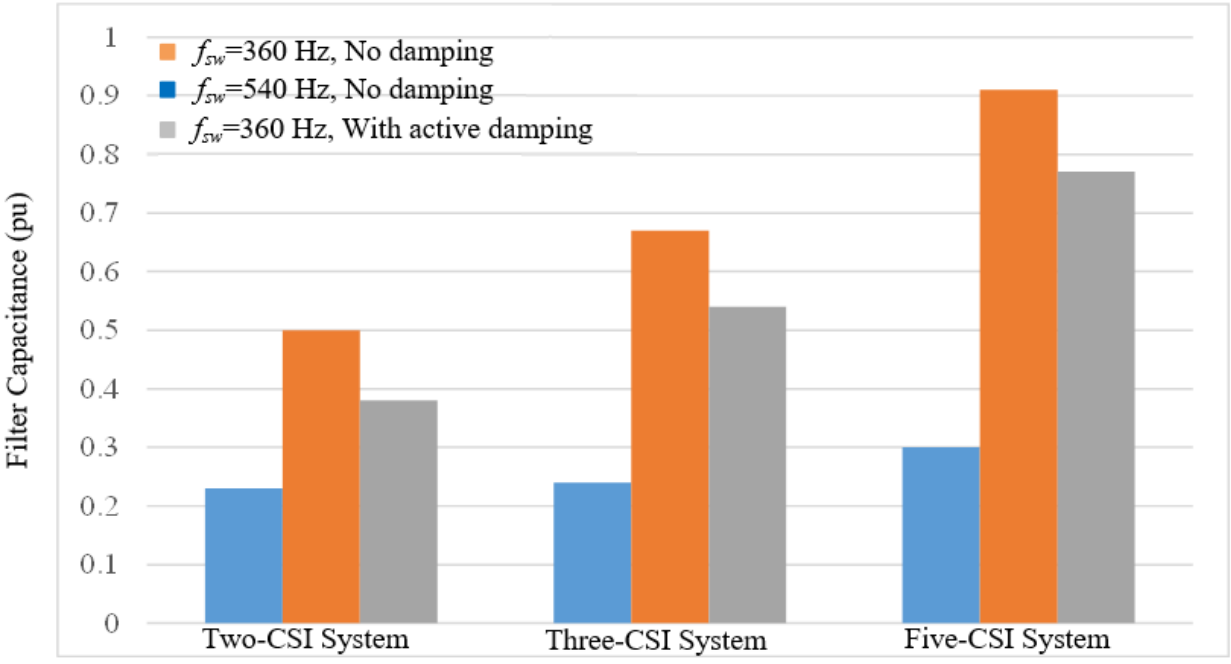


Figure 2-4 Comparison of filter capacitance of SC-CSIs.

## 2.4 Simulation Investigation

The simulation is conducted for a two-CSI system with and without active damping control to verify the active damping performance and filter capacitance reduction. The simulation parameters are provided in TABLE 2-5. Since the active damping control does not influence the properties and performance of the DC inductance, the DC voltage and large DC inductance are replaced by a DC current source, the simulation circuit is shown in Figure 2-5.

TABLE 2-5 Simulation parameters of a two-CSI system with active damping.

| | |
|---|---|
| **Topology** | Two-CSI System |
| **Switching Frequency** | 360 Hz |
| **Power Rating** | 4160 V/2 MVA |
| **Grid Voltage** | 4160 V |
| **DC Input Current** | 300 A |
| **Grid-Side Inductance** | 4.6 mH (0.2 pu) |
| **Grid-Side Resistance** | 0.08 Ω (0.01 pu) |
| **Virtual Resistance** | 10 Ω (1.2 pu) |
| **Filter Capacitance** | 118 μF (0.38 pu) |

The simulated waveforms of inverter output currents, capacitor voltages and grid current in a two-CSI system with a switching frequency of 360 Hz, without active damping, are presented in Figure 2-6. The inverter output currents of CSI#1 ($i_{w1}$) and CSI#2 ($i_{w2}$) exhibit six pulses in each positive and negative half cycle and have identical magnitudes and phase angles. The peak value of $i_{w1}$ and $i_{w2}$ equals to the product of the DC input current and a constant modulation index, which is calculated based on PF control. The grid current demonstrates good harmonic performance, ensuring compliance with the grid codes. The harmonic spectrums of the inverter output current of CSI#1 and grid current are shown in Figure 2-7. The dominant harmonic pairs in $i_{w1}$ are the 11th, 13th and 17th, and 19th orders. The design of the filter capacitance primarily focuses on suppressing the 13th harmonic current to comply with the grid codes.

With the calculated capacitor value, the grid current satisfies all the individual harmonic limits required by grid code.

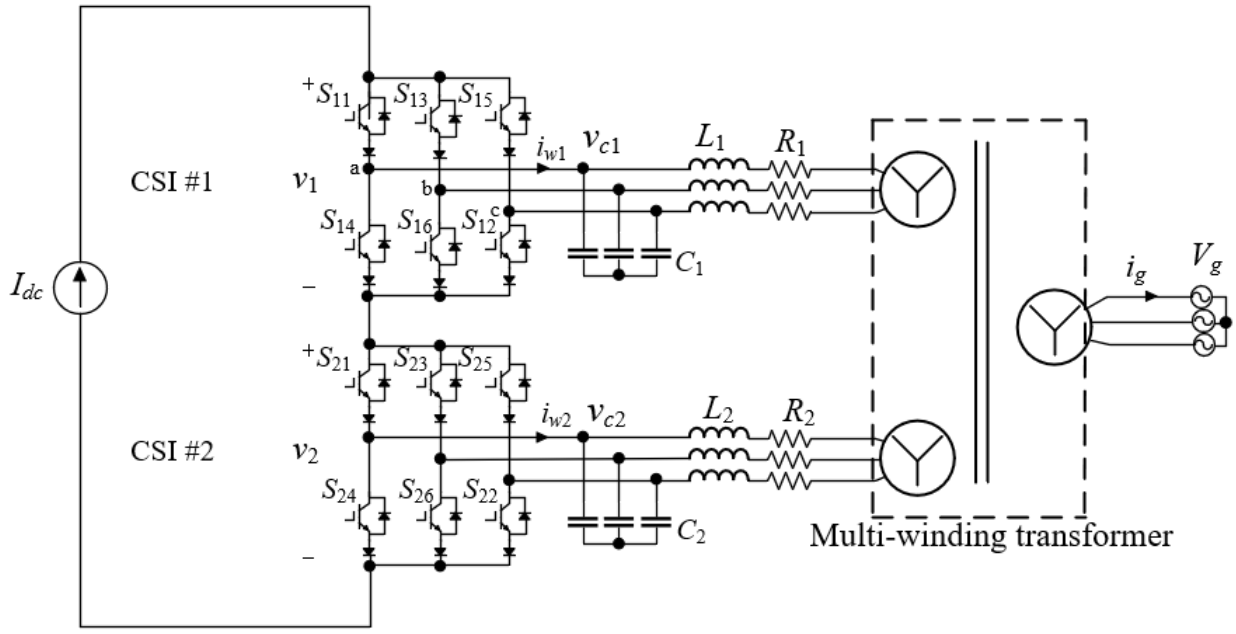


Figure 2-5 Simulation circuit for two-CSI systems.

The simulated waveforms of $i_{w1}$, $i_{w2}$, and $i_g$ for the two-CSI system with a switching frequency of 360 Hz, with active damping, are shown in Figure 2-8. Due to the new reference inverter output current containing both fundamental and harmonic components, the modulation index is not a constant value but varied with the harmonic damping current. This variation leads to the peak value of the inverter output current ($i_{w1}$, $i_{w2}$) being different from the DC input current. The harmonic spectrum of $i_{w1}$ and $i_g$ are shown in Figure 2-9. It can be observed that the 13th harmonic current in $i_{w1}$ is reduced to 23% with active damping compared to 28% without active damping. Since the 13th harmonic is the primary consideration for the filter capacitance design, the reduction in the 13th harmonic current results in a reduced filter capacitance requirement to comply with the grid code. The spectrum of the grid current ($i_g$) confirms that all individual harmonic currents satisfy the grid code requirements with the calculated filter capacitance.

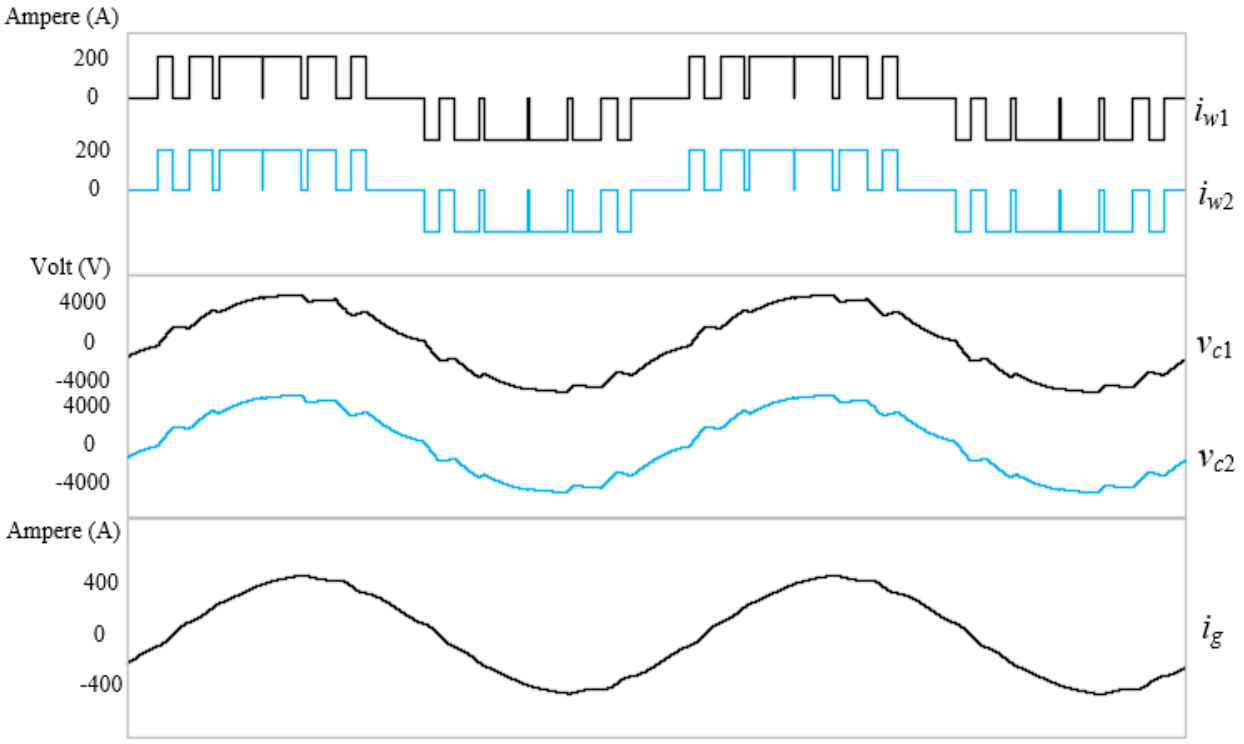


Figure 2-6 Simulated waveforms for a two-CSI system without active damping, $f_{sw}$=360 Hz.

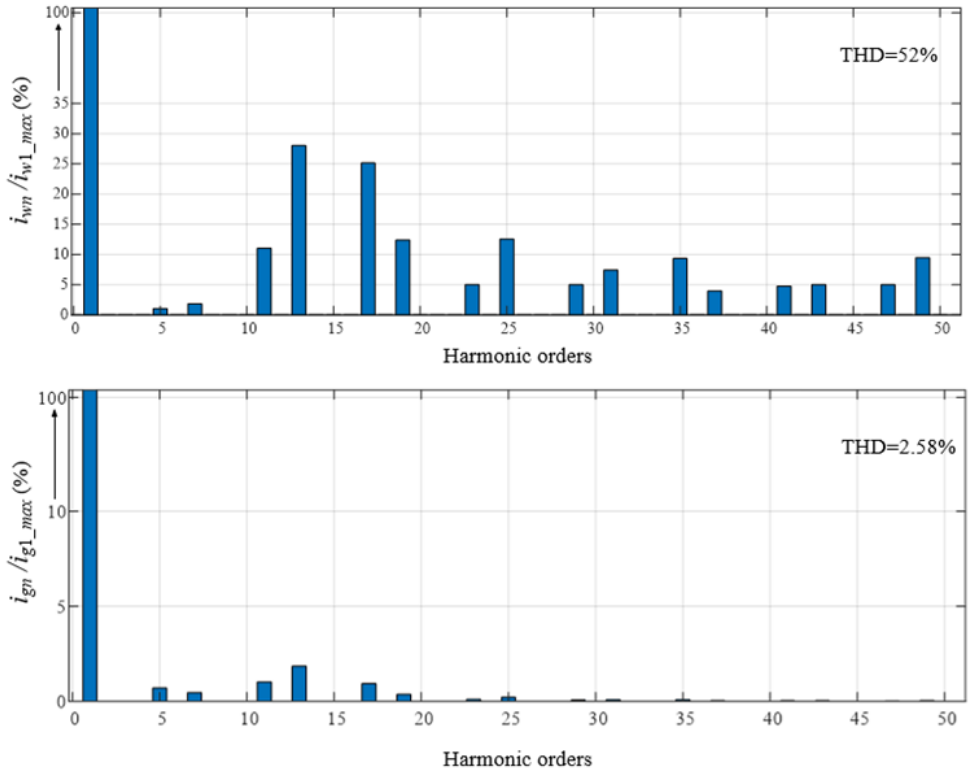


Figure 2-7 Harmonic spectrums of the inverter output current and grid current without active damping.

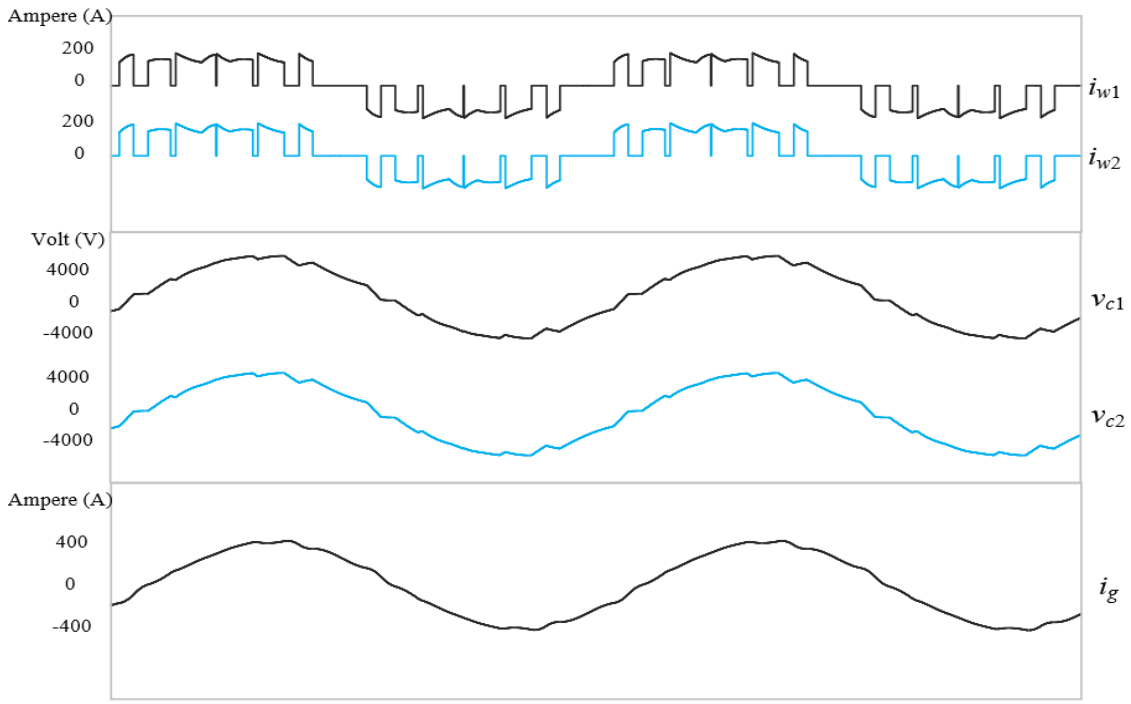


Figure 2-8 Simulated waveforms for a two-CSI system with active damping, $f_{sw}$=360 Hz.

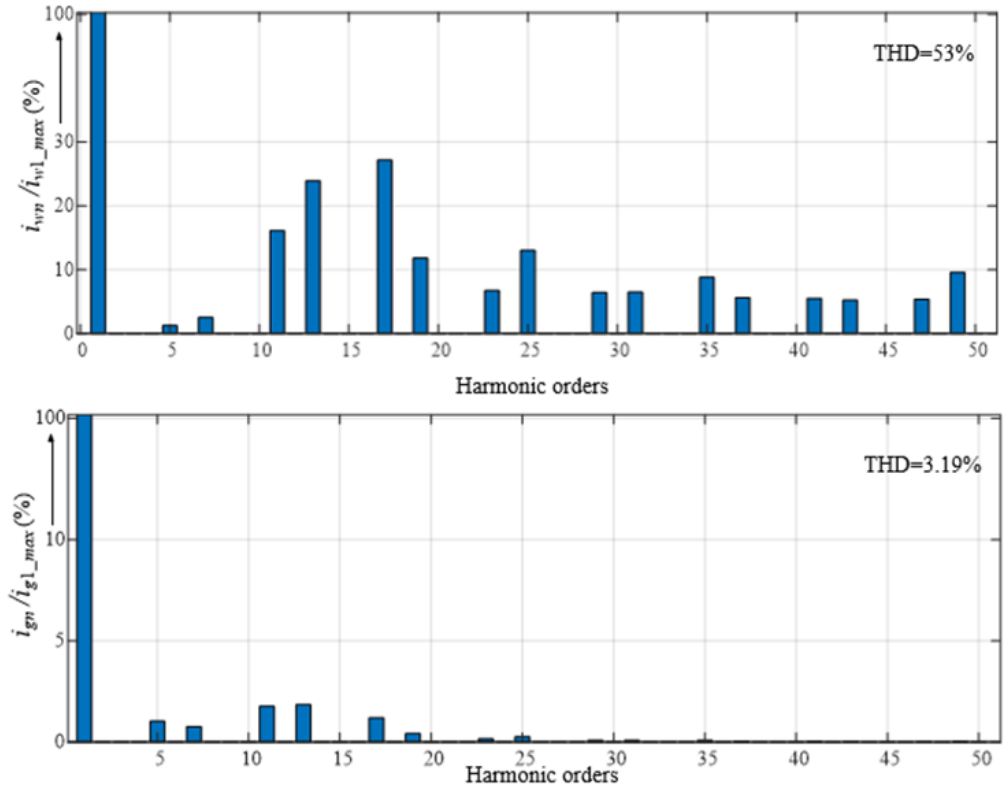


Figure 2-9 Harmonic spectrums of the inverter output current and grid current with active damping.

## 2.5 Summary

In this chapter, the switching frequency of SC-CSIs was reduced from 540 Hz to 360 Hz to reduce switching losses. The reduction in switching frequency resulted in a significant reduction of 33% in switching losses. However, this lower switching frequency led to more significant low-order harmonic components in the inverter output current. As a result, larger filter capacitors were required to comply with the grid codes, with capacitance increases of 114%, 180%, and 197% for two-CSI, three-CSI, and five-CSI systems, respectively, with a switching frequency of 360 Hz. To address this issue, active damping control is implemented into the SC-CSIs by emulating the virtual resistor in parallel with the filter capacitor. By generating a new reference inverter output current through PF control and active damping control, the dominant harmonic components in the original inverter output current were reduced, leading to the reduction in the required filter capacitance to meet grid code requirements. However, even with active damping, the reduced capacitance remained significantly larger than the capacitance used in conventional SC-CSIs.

In conclusion, while reducing the switching frequency from 540 Hz to 360 Hz effectively reduces switching losses in SC-CSIs, the filter capacitance substantially increases even with active damping. Therefore, this approach is not recommended to be used in practice.

# Chapter 3

# The Series-Connected CSI with Square Wave Operation

The method to reduce the switching frequency used in Chapter 2 does not work as well as expected due to the large size of filter capacitance even with active damping method. To further reduce the switching frequency without the trade-off of increasing passive components, the SC-CSI with 60-Hz square wave operation introduced in [42] is a good candidate for switching loss reduction. This topology replaces the multi-winding transformer with a phase-shifting transformer to mitigate the significant increase in passive components caused by the low switching frequency. This chapter introduces the operation of 60-Hz SC-CSIs, and the switching losses and the passive components are investigated. The simulation is conduced to analyze the performance of the 60-Hz SC-CSIs and the reduction of the passive components.

## 3.1 60-Hz SC-CSI Topology

The 60-Hz SC-CSI introduced in [42] is shown in Figure 3-1. The differences between 60-Hz SC-CSIs and conventional SC-CSIs are

1) 60-Hz square wave operation is applied to each CSI to enable 60 Hz switching frequency of the switches.

2) Phase-shifting modulation is applied to each CSI module, which results in the reduction of the DC inductor.

3) The phase-shifting transformer provides the phase displacement between its primary and secondary current for low-order harmonic elimination, significantly reducing the required filter capacitor size.

The passive components employed in this topology, such as LC filter and DC inductance, exhibit similar performance characteristics as those used in conventional SC-CSIs. The following sections will provide a detailed introduction to the square wave operation, phase-shifting transformer, and phase-shifting

modulation, offering a comprehensive understanding of their functionality and advantages within 60-Hz SC-CSIs.

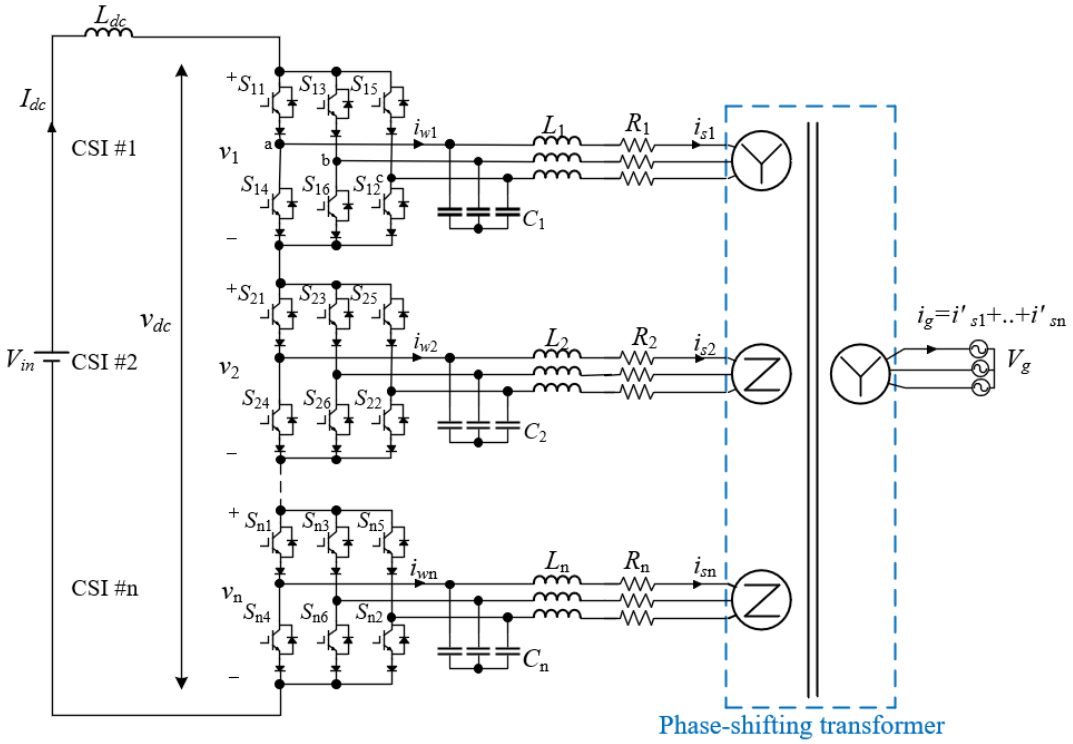


Figure 3-1 Topology of a 60-Hz n-SC-CSI.

## 3.2 Square Wave Operation and Phase-Shifting Modulation

Square wave operation is one of the several modulation schemes used in power converters that enable the fundamental switching frequency [43]. In 60-Hz SC-CSIs, all switches operate with a fundamental switching frequency of 60 Hz. The switching scheme of the square wave operation is shown in TABLE 3-1. To satisfy the switching constraints of the current source converter, each switch conducts for 120° and has a phase displacement of 60° from each other. However, the 60-Hz operation features substantial low-order harmonics, such as 5th and 7th harmonics, into the inverter output current waveform. These low-order harmonics require very bulky and costly harmonic filters at the output to improve harmonic performance. The example of the inverter output current waveform and its harmonic spectrum is presented

in Figure 3-2. From the Fourier series expression represented as Equation (3-1), the highest DC current utilization ($i_{w1,max}/I_{dc}$) is at 0.78.

$$i_{w1}(t) = \sum_{n=1,5,7....}^{\infty} \left[ \frac{4I_{dc}}{n\pi} \cos(\frac{\pi}{6} n) \sin(n\omega t) \right] \tag{3-1}$$

TABLE 3-1 Modulation scheme of square wave operation.

| **Gating signals for CSI #1** | | | | | | | |
|---|---|---|---|---|---|---|---|
| ***θ*** | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{15}$ | $S_{16}$ | $i_{w1}$ |
| 0-60° | 1 | 0 | 0 | 0 | 0 | 1 | $I_{dc}$ |
| 60°-120° | 1 | 1 | 0 | 0 | 0 | 0 | $I_{dc}$ |
| 120°-180° | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 180°-240° | 0 | 0 | 1 | 1 | 0 | 0 | $-I_{dc}$ |
| 240°-300° | 0 | 0 | 0 | 1 | 1 | 0 | $-I_{dc}$ |
| 300°-360° | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

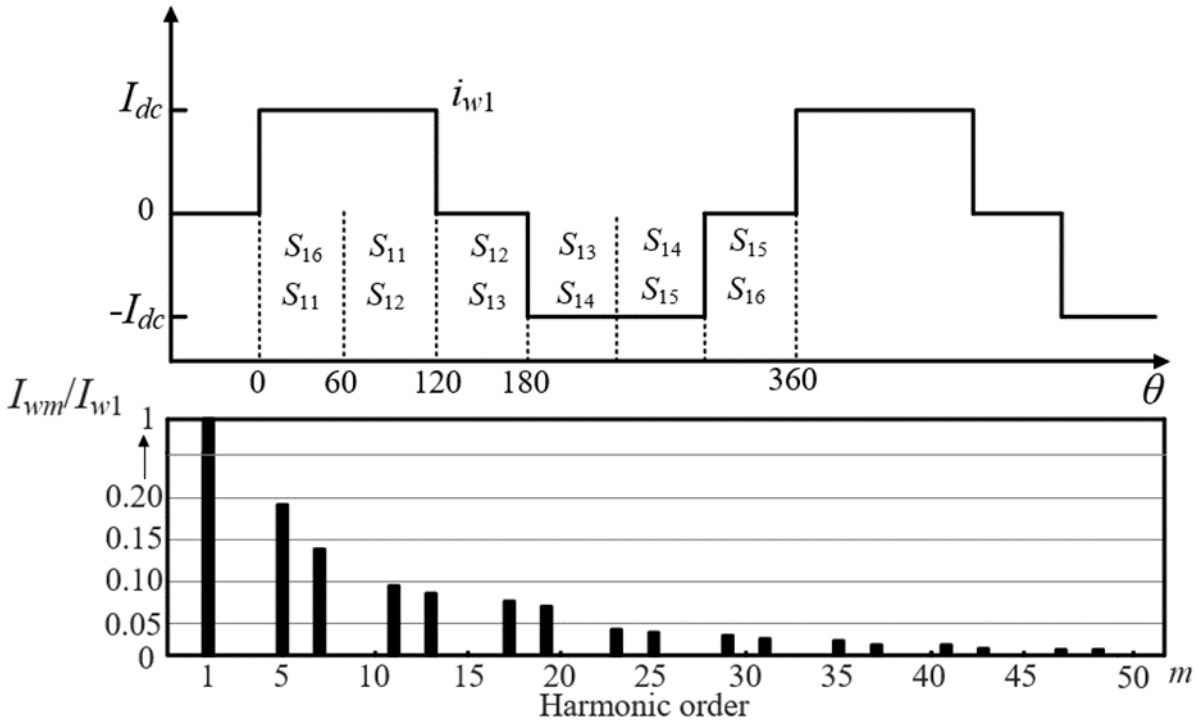


Figure 3-2 Waveform of inverter output current and its harmonic spectrum [42].

The phase-shifting modulation provides the phase displacement between each CSI output current. The phase-shifting angle between CSI #1 and CSI #n is $\delta$, which can be calculated by:

$$\delta = \frac{60(\mathrm{n}-1)}{\mathrm{n}} \tag{3-2}$$

where n is the number of CSI modules. For example, $\delta$=30° in a two-CSI system. The LC filter output current in CSI#1 and CSI#2 can be expressed as

$$\begin{aligned} i_{s1} &= \sum_{m=1,5,7\ldots} I_m \sin(m\omega t) \\ i_{s2} &= \sum_{m=1,5,7\ldots} I_m \sin(m\omega t + 30^\circ) \end{aligned} \tag{3-3}$$

where $i_{s1}$ and $i_{s2}$ are the filter output current of CSI#1 and CSI#2, respectively, m is the harmonic order.

Note that the phase-shifting modulation may cause the complexity of the control algorithm, particularly in terms of voltage or current detection prior to the phase-shifting transformer. For instance, the active damping control introduced in Chapter 2 relies on the measured capacitor voltage of CSIs. In conventional SC-CSIs, where the capacitor voltage of each CSI is identical, and in phase, the active damping control can be easily implemented using the detected capacitor voltage from any CSI module. However, in the case of 60-Hz SC-CSIs, the capacitor voltages of CSIs experience a phase displacement provided by the phase-shifting modulation. Considering the phase displacement among capacitor voltages in 60-Hz SC-CSIs makes the control algorithm more complex than conventional SC-CSIs.

## 3.3 Phase-Shifting Transformer

In 60-Hz SC-CSIs, phase-shifting transformers are employed instead of the multi-winding transformers used in conventional SC-CSIs. These phase-shifting transformers introduce a phase shift angle ($\delta$) between the primary and secondary sides, enabling harmonic cancellation. The relation of phase angle before and after the transformer can be expressed as

$$\begin{aligned} \angle i'_{sn-m} &= \angle i_{sn-m} - \delta \quad \text{for positive-sequence harmonics} \\ \angle i'_{sn-m} &= \angle i_{sn-m} + \delta \quad \text{for negative-sequence harmonics} \end{aligned} \tag{3-4}$$

where $i_{sn-m}$ and $i'_{sn-m}$ refer to the *m*th-order harmonic currents before and after the transformer, respectively. The phase shift in the transformer can be realized by connecting the primary and secondary winding in different configurations. Different configurations, including wye (Y), delta (Δ), or zigzag (Z) arrangements, can be employed in the phase-shifting transformer to provide the desired phase shift angle.

Taking the two-CSI and three-CSI systems as examples of how phase-shifting transformers can be utilized. In the two-CSI system, the Y/Y configuration is employed in CSI#1, where no phase-shifting is provided. The Δ/Y configuration can be used in CSI#2 to provide the phase shifting angle of 30° between its primary and secondary winding current while keeping the primary and secondary voltages unchanged. The configuration diagram of a Δ/Y transformer is shown in Figure 3-3. The turn ratio of the transformer in the simulation is set to be 1:$\sqrt{3}$. For the three-CSI system, the configuration of Z/Δ can be used in CSI#2 and CSI#3 to provide the phase shifting angle of 20° and 40°, respectively. The configuration of a Z/Δ diagram is shown in Figure 3-4. The turn ratio can be calculated using the information provided in TABLE 3-2 [1]. The configuration and turn ratios of the transformer for more CSIs connected in series can be designed in the same manner.

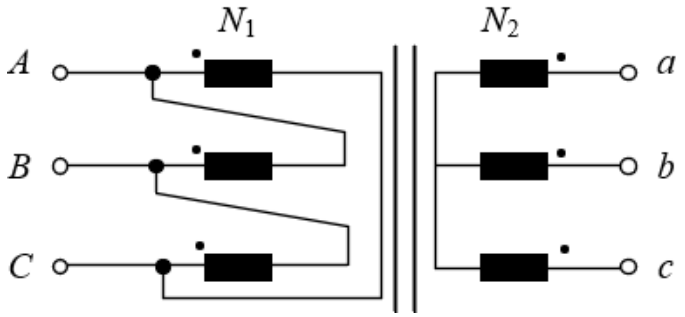


Figure 3-3 Δ/Y transformer.

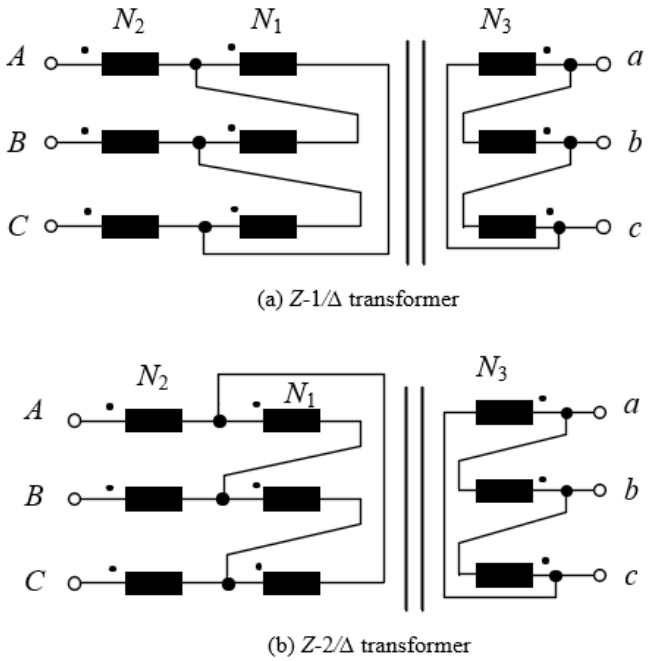


Figure 3-4 Z/Δ transformer.

It's worth noting that, compared to the multi-winding transformer used in conventional SC-CSIs, the phase-shifting transformer employed in the 60-Hz SC-CSIs maintains the same power and voltage rating but with more complex winding configurations. This complex configuration does not cause a high cost because the main factors affecting the cost of the transformer are power rating and insulation level [42].

TABLE 3-2 Turn ratios of *Z*/Δ transformer.

| **Transformer configuration** | **Phase-shifting angle** | $\frac{N_3}{N_2+N_3}$ | $\frac{N_1}{N_2+N_3}$ |
|---|---|---|---|
| Z-1/Δ | 0° | 0 | 1.0 |
| | 15° | 0.366 | 1.225 |
| | 20° | 0.532 | 1.347 |
| | 30° | 1.0 | 1.732 |
| Z-2/Δ | 40° | 0.532 | 1.347 |
| | 45° | 0.366 | 1.225 |
| | 60° | 0 | 1.0 |

## 3.4 Harmonic Elimination

The low-order harmonic current elimination of the grid current can be achieved by combining the phase-shifting modulation and phase-shifting transformers. For example, the grid current of a two-CSI system can be derived as

$$\begin{aligned} i_g &= i'_{s1} + i'_{s2} \\ &= \underbrace{\sum_{m=1,5,7...} I_m \sin(m\omega t)}_{i'_{s1}} + \underbrace{\sum_{m=1,7,13...} I_m \sin\left\{m(\omega t + 30^\circ) - 30^\circ\right\}}_{i'_{s2}\ \text{Positive sequence}} + \underbrace{\sum_{m=5,11,17...} I_m \sin\left\{m(\omega t + 30^\circ) + 30^\circ\right\}}_{i'_{s2}\ \text{Negative sequence}} \\ &= 2I_1 \sin(\omega t) + 2I_{11} \sin(11\omega t) + 2I_{13} \sin(13\omega t) + ... \end{aligned} \tag{3-5}$$

where $i'_{s1}$, and $i'_{s2}$ are the secondary winding currents of the transformer. The harmonic currents of 5th, 7th, 17th, 19th orders etc. in $i'_{s1}$ and $i'_{s2}$ are 180° out of phase. Since the load current $i_g$ is equal to the summation of $i'_{s1}$ and $i'_{s2}$, its harmonic currents at 5th 7th 17th 19th orders etc., are eliminated. Based on the Equation (3-5), the elimination of the specific harmonic currents for any 60-Hz SC-CSIs can be obtained. With more CSIs connected in series, the more low-order harmonic currents can be eliminated.

## 3.5 Switching Losses Investigation

The investigation of switching losses involves calculating the switching losses for the two-CSI, three-CSI, and five-CSI systems. This investigation considers both the switching frequency of 540 Hz and 60 Hz, with corresponding system power ratings of 4160 V/2 MVA and 4160 V/5 MVA, respectively. The spice parameters of the switches can be found in TABLE 2-1. The calculated switching losses of SC-CSIs with switching frequency of 540 Hz and 60 Hz are listed in TABLE 3-3. Compared to the conventional SC-CSIs, the switching losses in 60-Hz SC-CSIs reduced around 90%. This significant reduction of the switching losses highlights the advantages of using 60-Hz SC-CSIs, including improved efficiency and reduce the power dissipation.

TABLE 3-3 Calculated switching losses of SC-CSIs.

| Topology | Device Switching Losses (W) | | Total Switching Losses (W) | Percentage Reduction (%) |
|---|---|---|---|---|
| Two-CSI system $f_{sw}$= 540 Hz | IGBTs | 8768 | 22382 | 90 |
| | Diodes | 13614 | | |
| Two-CSI system $f_{sw}$= 60 Hz | IGBTs | 881 | 2250 | |
| | Diodes | 1369 | | |
| Three-CSI system $f_{sw}$= 540 Hz | IGBTs | 13152 | 33574 | 90 |
| | Diodes | 20422 | | |
| Three-CSI system $f_{sw}$= 60 Hz | IGBTs | 1322 | 3376 | |
| | Diodes | 2053 | | |
| Five-CSI system $f_{sw}$= 540 Hz | IGBTs | 21920 | 55957 | 90 |
| | Diodes | 34037 | | |
| Five-CSI system $f_{sw}$= 60 Hz | IGBTs | 2167 | 5532 | |
| | Diodes | 3365 | | |

## 3.6 Passive Components Investigation

### 3.6.1 DC Inductance

The DC inductance in 60-Hz SC-CSIs is reduced compared to the conventional SC-CSIs by implementing the phase shifting modulation to each CSI module. The DC inductance ($L_{dc}$) in a 60-Hz n-SC-CSI can be expressed as

$$L_{dc} = \frac{\left| V_{in} - \frac{1}{\Delta t}\int_{t}^{t+\Delta t} v_{dc}\,dt \right| \Delta t}{\Delta I_{dc}}$$
$$v_{dc} = v_1 + \underbrace{v_1(\theta + \frac{60}{\mathrm{n}})}_{v_2} + \ldots + \underbrace{v_1(\theta + \delta)}_{v_{\mathrm{n}}} \tag{3-6}$$

This modulation scheme introduces a phase-shifting angle (δ) in the input voltage of each CSI module. Consequently, the sum of the input voltages ($v_{dc}$) for each CSI module is calculated differently compared to conventional SC-CSIs. Taking a 60-Hz 2-SC-CSI as an example, the waveform of input voltage ($v_{in}$), and $v_{dc}$ for one fundamental cycle of inverter output currents ($i_{w1}$, $i_{w2}$) is shown in Figure 3-5. The DC inductance can be calculated as

$$
\begin{aligned}
L_{dc} &= \frac{\left| V_{in} - \frac{1}{\Delta t}\int_{t}^{t+\Delta t} v_1 + v_2 dt \right| \Delta t}{\Delta I_{dc}} \\
&= \frac{\left| V_{in} - \frac{1}{\Delta t}\int_{t}^{t+\Delta t} v_{ab} + v_{ab}(\theta + \frac{\pi}{6}) dt \right| \Delta t}{\Delta I_{dc}} \\
&= \frac{\left| V_{in} - \frac{1}{\Delta t}\int_{t}^{t+\Delta t} \sqrt{3} V_g \cos(\theta + \frac{\pi}{6}) dt + \sqrt{3} V_g \cos(\theta + \frac{\pi}{3}) dt \right| \Delta t}{\Delta I_{dc}}
\end{aligned}
\tag{3-7}
$$

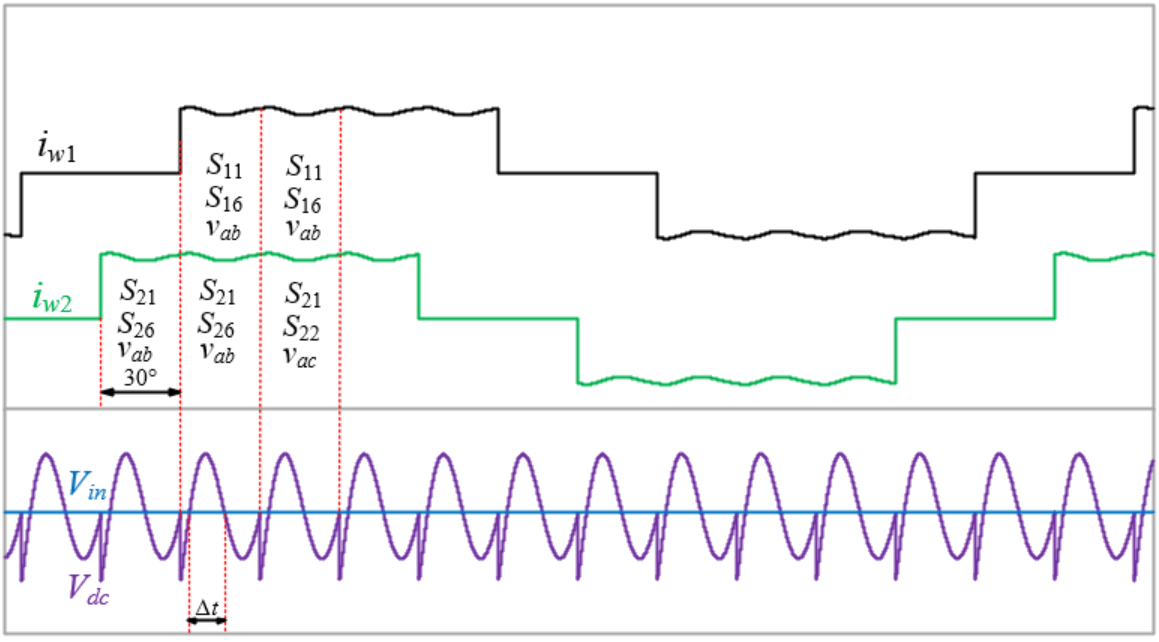


Figure 3-5 Waveforms of $V_{in}$ and $v_{dc}$ for a 60-Hz 2-SC-CSI.

TABLE 3-4 Calculated DC inductance for conventional and 60-Hz SC-CSIs.

| Topology | Power Rating | DC Current Ripple | DC Inductance | Percentage Reduction |
|---|---|---|---|---|
| Two-CSI system $f_{sw}$= 540 Hz | 4160 V/2 MVA | 12%$I_{dc}$ | 50 mH (2.1 pu) | 78% |
| Two-CSI system $f_{sw}$= 60 Hz | 4160 V/2 MVA | 12%$I_{dc}$ | 11 mH (0.5 pu) | |
| Three-CSI system $f_{sw}$= 540 Hz | 4160 V/3 MVA | 12%$I_{dc}$ | 75 mH (4.9 pu) | 78% |
| Three-CSI system $f_{sw}$= 60 Hz | 4160 V/3 MVA | 12%$I_{dc}$ | 16.5 mH (1.07 pu) | |
| Five-CSI system $f_{sw}$= 540 Hz | 4160 V/5 MVA | 12%$I_{dc}$ | 125 mH (13.5 pu) | 80% |
| Five-CSI system $f_{sw}$= 60 Hz | 4160 V/5 MVA | 12%$I_{dc}$ | 23 mH (2.5 pu) | |

TABLE 3-4 lists the calculated values of DC inductances for 60-Hz two-CSI, three-CSI, and five-CSI systems Additionally, the table includes a comparison in terms of percentage reduction with respect to the conventional SC-CSIs. It can be observed that the 60-Hz two-CSI, three-CSI, and five-CSI systems achieve approximately an 80% reduction in the DC link inductance compared to the conventional SC-CSIs.

## 3.6.2 Filter Capacitance

Unlike conventional SC-CSIs, which only rely on the LC filter to improve the harmonic performance, there are two components in 60-Hz SC-CSIs aimed at improving harmonic performance: LC filter and phase-shifting transformer. Since the phase-shifting transformer eliminates significant low-order harmonics, the required filter capacitance to meet grid code in 60-Hz SC-CSIs is reduced compared with conventional SC-CSIs. Considering the total grid-side inductance of 0.2 pu and grid-side resistance of 0.01 pu, the calculated filter capacitance for conventional SC-CSIs and 60-Hz SC-CSIs are listed in TABLE 3-

5. With more CSIs connected in series, the more low-order harmonic currents can be eliminated, resulting in the smaller filter capacitor size to comply with the harmonic limits from the grid code.

TABLE 3-5 Calculated filter capacitance for conventional SC-CSIs and 60-Hz SC-CSIs.

| Topology | Power Rating | Filter Capacitance | Percentage Reduction |
|---|---|---|---|
| Two-CSI system $f_{sw}$= 540 Hz | 4160 V/2 MVA | 70 µF (0.23 pu) | - |
| Two-CSI system $f_{sw}$= 60 Hz | 4160 V/2 MVA | 75 µF (0.24pu) | |
| Three-CSI system $f_{sw}$= 540 Hz | 4160 V/3 MVA | 110 µF (0.24 pu) | 66% |
| Three-CSI system $f_{sw}$= 60 Hz | 4160 V/3 MVA | 37 µF (0.08 pu) | |
| Five-CSI system $f_{sw}$= 540 Hz | 4160 V/5 MVA | 235 µF (0.3pu) | 94% |
| Five-CSI system $f_{sw}$= 60 Hz | 4160 V/5 MVA | 14 µF (0.018 pu) | |

## 3.7 Simulation Investigation

Simulation is conducted to analyze the performance of 60-Hz SC-CSIs and verify the calculated passive components. The simulation parameters are listed in TABLE 3-6. The simulated waveforms of the 60-Hz two-CSI, three-CSI, and five-CSI are shown in Figure 3-6, Figure 3-7, and Figure 3-8, respectively. The DC input current ($I_{dc}$) of each inverter contains a 12% current ripple. The output currents of each CSI ($i_{w1}$-$i_{wn}$) are identical but have a 30° phase shift between any adjacent currents in the two-CSI system, a 20° phase shift in the three-CSI system, and a 12° phase shift in the five-CSI system. The phase-shifting transformer provides desired phase shifts between its primary ($i_{s1}$-$i_{sn}$) and secondary ($i'_{s1}$-$i'_{sn}$) winding currents in the two-CSI, three-CSI and five CSI systems, respectively. The primary ($i_{s1}$-$i_{sn}$) and secondary ($i'_{s1}$-$i'_{sn}$) winding currents of the phase-shifting transformer experience significant low-order harmonics,

leading to high distortion in the current. The excellent harmonic performance of grid current is achieved in each inverter thanks to the low-order harmonic elimination of the phase-shifting transformer. Fig 3-9 shows the harmonic spectrums of the grid current ($i_g$) for each SC-CSI. Except for the fundamental frequency, the minimum harmonic frequency of $i_g$ can be identified at the 11th order in the two-CSI system, the 17th order in the three-CSI system, and the 29th order in the five-CSI system.

TABLE 3-6 Simulation parameters of 60-Hz SC-CSIs.

| **Topology** | Two-CSI System | Three-CSI System | Five-CSI System |
|---|---|---|---|
| **Switching Frequency** | 60 Hz | 60 Hz | 60 Hz |
| **Power Rating** | 4160 V/2 MVA | 4160 V/3 MVA | 4160 V/3 MVA |
| **DC Inductance** | 11 mH<br>(0.5 pu) | 16.5 mH<br>(1.07 pu) | 23 mH<br>(2.5 pu) |
| **Filter Capacitance** | 75 μF<br>(0.24pu) | 37 μF<br>(0.08pu) | 14 μF<br>(0.018pu) |
| **Grid-Side Inductance** | 4.6 mH<br>(0.2 pu) | 3.0 mH<br>(0.2 pu) | 1.8 mH<br>(0.2 pu) |
| **Grid-Side Resistance** | 0.09 Ω<br>(0.01 pu) | 0.06 Ω<br>(0.01 pu) | 0.04 Ω<br>(0.01 pu) |

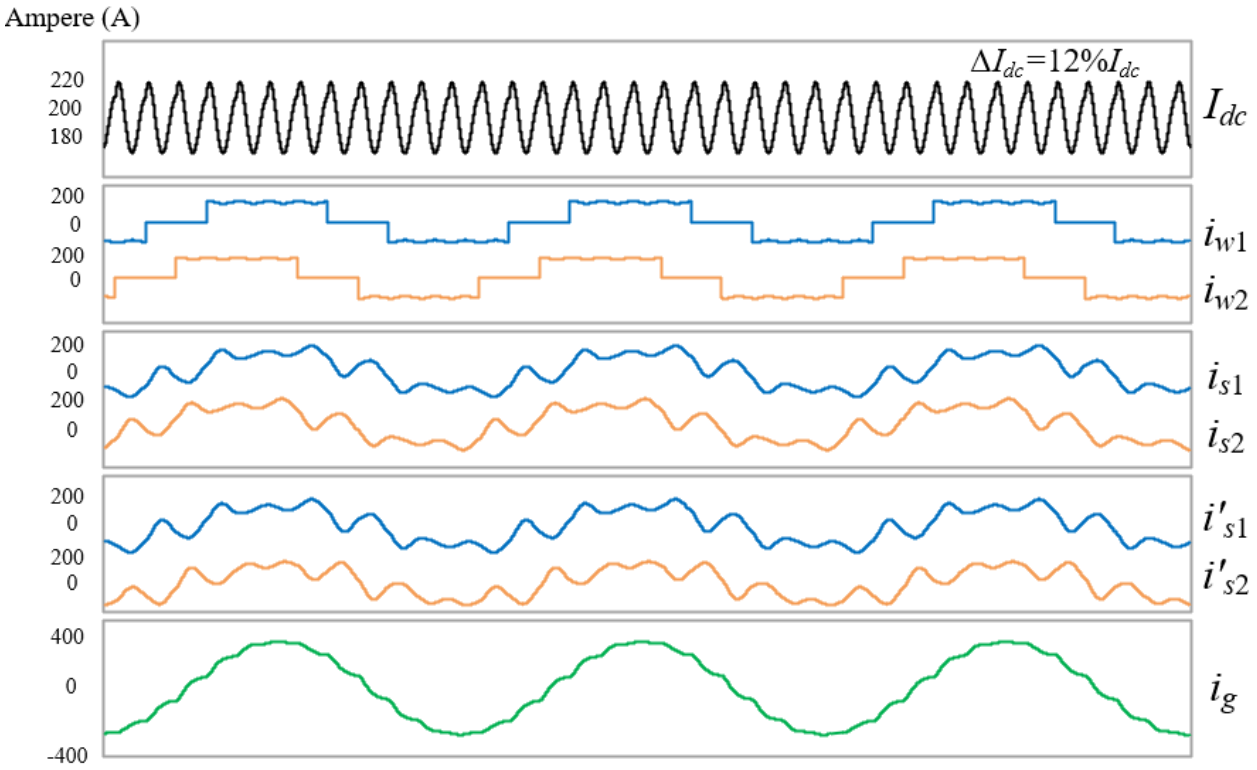


Figure 3-6 Simulated waveforms for a 60-Hz two-CSI.

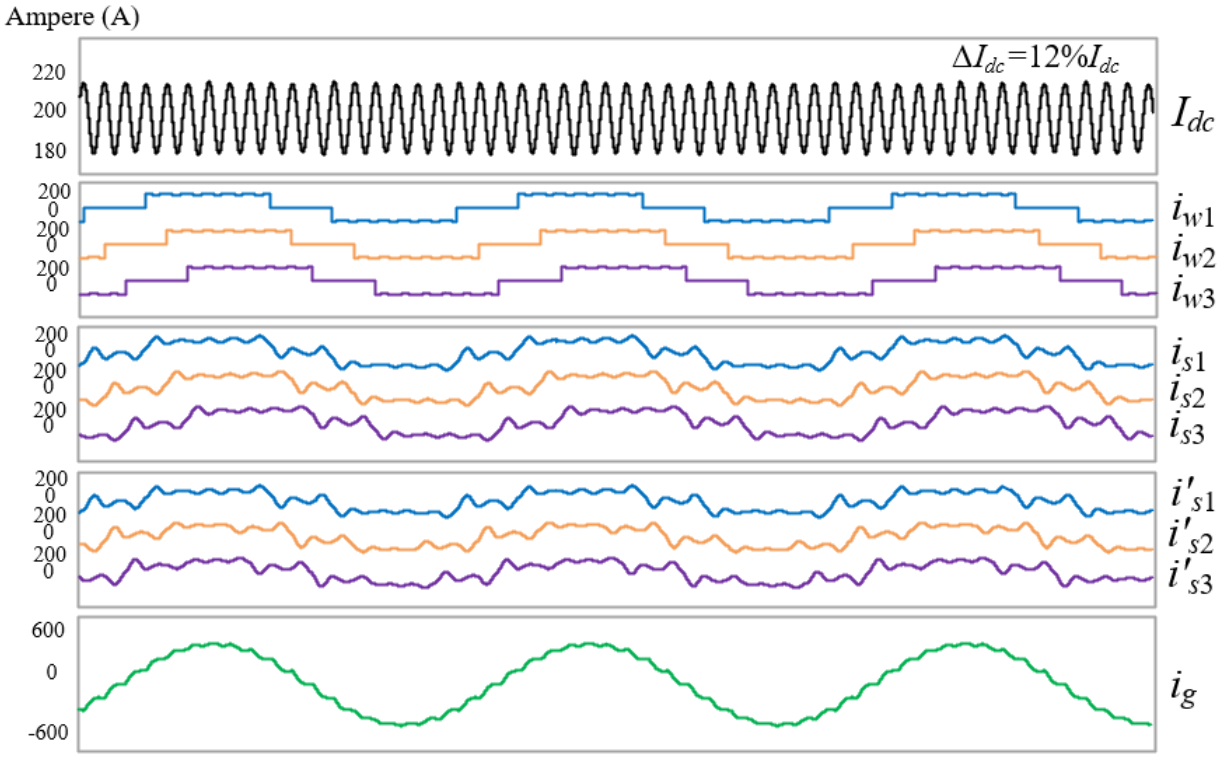


Figure 3-7 Simulated waveforms for a 60-Hz three-CSI.

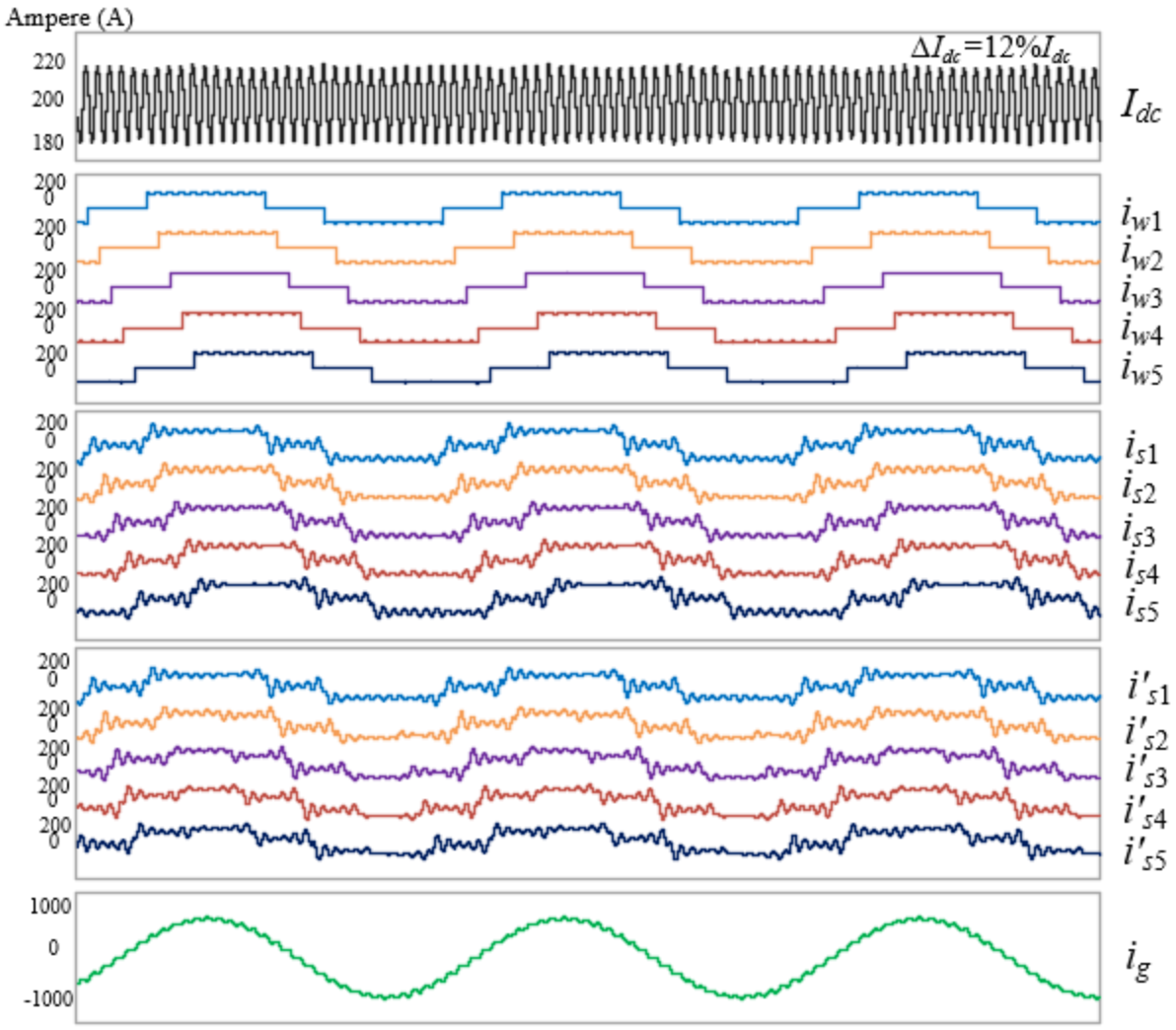


Figure 3-8 Simulated waveforms for a 60-Hz five-CSI.

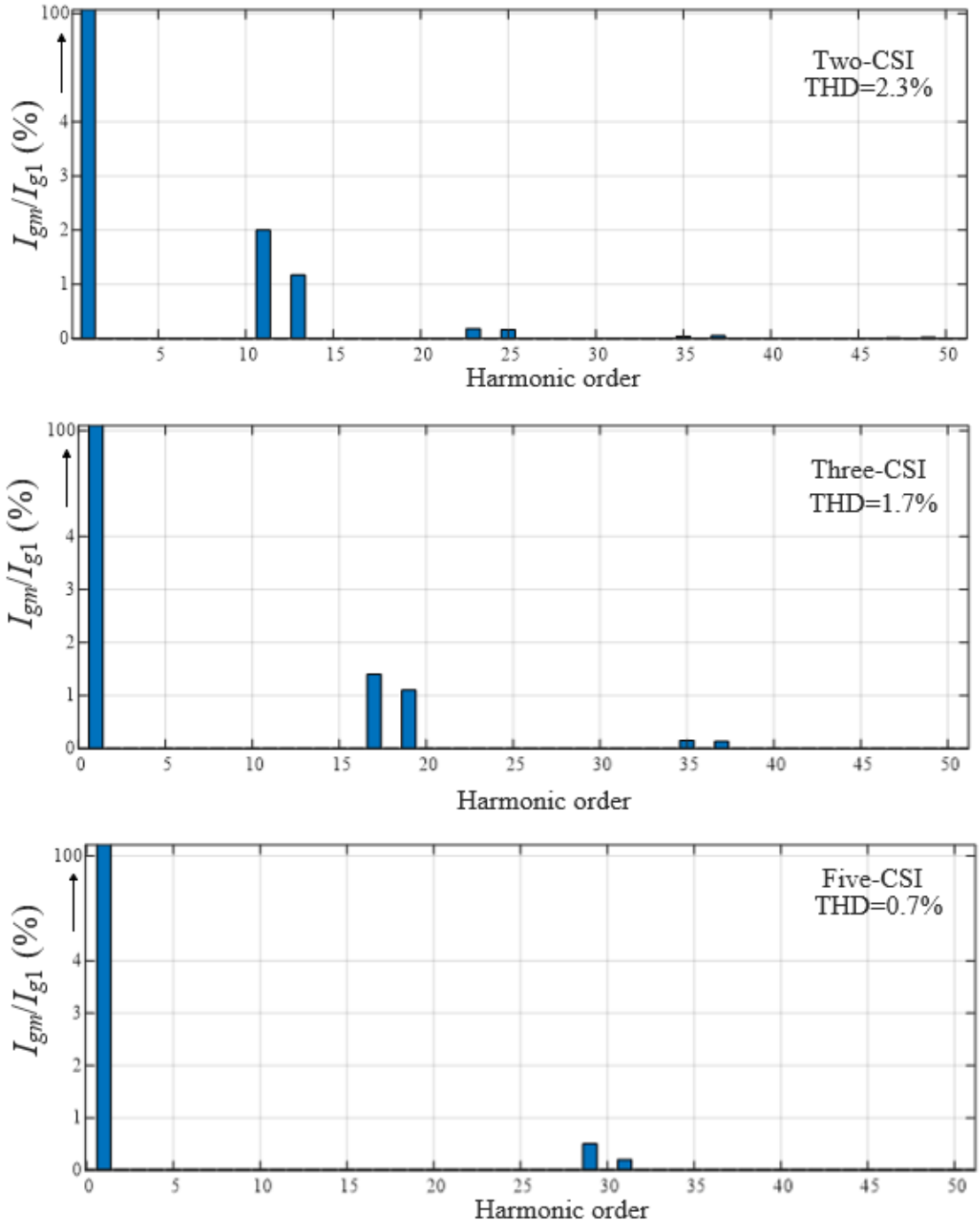


Figure 3-9 Harmonic spectrums of grid current $i_g$ in 60-Hz SC-CSIs.

## 3.8 Summary

This chapter employed series-connected connected current source inverters with a switching frequency of 60 Hz to further reduce the switching losses. Compared to the conventional SC-CSIs with a switching frequency of 540 Hz, this topology features lower switching losses, higher DC current utilization and reduced passive components. The switching losses and passive components for two-CSI, three-CSI and five-CSI systems are investigated. The results demonstrated that the 60-Hz SC-CSIs achieved a reduction of over 90% in switching losses compared to conventional SC-CSIs. Approximately 80% reduction of the DC inductance is achieved in 60-Hz two-CSI, three-CSI, and five-CSI systems. The reduction of filter capacitance depends on the number of CSI modules connected in series. As more modules are connected, the reduction of the capacitance to comply with the grid code can be further enhanced.

# Chapter 4

# Conclusions

## 4.1 Conclusions and Contributions

In conclusion, this thesis investigated methods to reduce the switching losses of SC-CSIs while mitigating the trade-off of increased passive components. Chapter 2 focused on reducing the switching frequency from 540 Hz to 360 Hz using SVM. The reduced switching frequency resulted in the efficient reduction of switching losses and increased the filter capacitance. The introduction of active damping control helped mitigate the increased filter capacitance. Chapter 3 introduced the 60-Hz SC-CSI topology with square wave operation, which achieved a significant reduction of over 90% in switching losses compared to conventional SC-CSIs. This topology also demonstrated the ability to effectively reduce the filter capacitance and DC inductance through phase-shifting modulation and phase-shifting transformers.

Overall, the 60-Hz SC-CSIs proved to be more competitive in reducing switching losses and passive components compared to conventional SC-CSIs and 360-Hz SC-CSIs. While reducing the switching frequency to 360 Hz showed promising results in reducing switching losses, it led to an increase in low-order harmonic components and subsequently larger filter capacitance requirements. The active damping control approach helped mitigate the capacitance increase, but the reduced capacitance still remained significantly larger than that of conventional SC-CSIs. On the other hand, 60-Hz SC-CSIs can further reduce switching losses and feature reduced passive components compared to conventional SC-CSIs.

In summary, this thesis highlighted the importance of carefully considering the trade-offs between switching losses and passive component sizes when designing SC-CSIs with reduced switching frequencies. The 60-Hz SC-CSI topology emerged as a more favorable solution for achieving significant switching losses and passive components reduction.

## 4.2 Future Work

The following studies and research are recommended for the future work.

1. Experimental Validation: Conduct experimental studies to validate the simulation results and performance of the proposed SC-CSI configurations. Build physical electric systems and conduct comprehensive experimental tests to verify the reduction in switching losses, passive component sizes, and the effectiveness of the active damping control approach.
2. Techniques to Reduce Filter Capacitance Size: Investigate and implement additional techniques to further reduce the size of the filter capacitor in 360 Hz-SC-CSIs.
3. Implement Active Damping into 60-Hz SC-CSIs: implement active damping control into 60-Hz SC-CSIs to see if the filter capacitance can be further reduced.

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